DSP

DATABOOK

1994

HARRIS

New Digital Signal Processing Products

HSP50016
DIGITAL DOWN CONVERTER

(Page 6-3)

- SINGLE CHIP NARROW BAND DOWN CONVERTER
- INPUT SAMPLE RATE = 52 MSPS
- OUTPUT SAMPLE RATE = 82Hz TO 459Hz
- TUNING RESOLUTION = 0.0012Hz

HSP43216
HALF BAND FILTER

(Page 3-43)

- UP/DOWN CONVERSION BY Fs/4
- INTERPOLATION/DECIMATION BY 2
- SHAPE FACTOR = 1.24
- PASSBAND RIPPLE < 0.0005dB
- STOPBAND ATTENUATION > 90dB

HSP50016-EV
DDC EVALUATION BOARD

(Page 8-10)

- PC BASED DATA AND CONTROL
- REAL TIME DATA AND CONTROL
- RAPID PROTOTYPING

HSP43124
SERIAL I/O FILTER

(Page 3-3)

- 24 BIT INPUT, 32 BIT OUTPUT DATA
- 256 TAP PROGRAMMABLE FIR FILTER
- 5 CASCADED HALF BAND FILTERS

HSP50110
DIGITAL QUADRATURE TUNER

(Page 6-25)

- FRONT END OF DEMODULATION CHIP SET
- DEMODULATES PSK, FSK, AM, FM
- PROVIDES TUNING, INITIAL FILTERING
- INPUT SAMPLE RATE = 60MSPS
- DATA BITS = 10

$5.00

HARRIS SEMICONDUCTOR

HARRIS SEMICONDUCTOR DSP PRODUCTS

This Digital Signal Processing databook represents the full line of Harris Semiconductor DSP products for commercial and military applications and supersedes previously published DSP material under the Harris, GE, RCA or Intersil names. For a complete listing of all Harris Semiconductor products, please refer to the Product Selection Guide (PSG-201S; ordering information below.)

For complete, current and detailed technical specifications on any Harris devices please contact the nearest Harris sales, representative or distributor office; or direct literature requests to:

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P.O. Box 883, MS CB1-28
Melbourne, FL 32901
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FAX: (407) 724-3937

See Section 12 for Data Sheets Available on AnswerFAX

See Technical Assistance Listing on Page vi

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HARRIS
SEMICONDUCTOR

DIGITAL SIGNAL PROCESSING

FOR COMMERCIAL AND MILITARY APPLICATIONS

TECHNICAL ASSISTANCE

For technical assistance on the Harris products listed in this databook, please contact the Field Applications Engineering staff available at one of the following Harris Sales Offices:

UNITED STATES		
CALIFORNIA	San Jose	408-985-7322
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FLORIDA	Melbourne	407-723-0501
GEORGIA	Duluth	404-476-2035
ILLINOIS	Schaumburg	708-240-3480
NEW JERSEY	Voorhees	609-751-3425
NEW YORK	Great Neck	516-829-9441
INTERNATIONAL		
FRANCE	Paris	33-1-346-54046
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DSP 1

GENERAL INFORMATION

ALPHA NUMERIC PRODUCT INDEX

NOTE: Bold Type Designates a New Product from Harris.

/883 Data Sheet Format - In the interests of conserving space, data sheets for /883 qualified products have been printed without the Pinouts, Pin Description, Waveforms, AC Test Load Circuit and Design Information sections. The information in these sections can be obtained from the corresponding portion of the commercial data sheets.

ALPHA NUMERIC PRODUCT INDEX (Continued)

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PRODUCT INDEX BY FAMILY

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PRODUCT INDEX BY FAMILY (Continued)

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DATA ACQUISITION PRODUCTS

A/D CONVERTERS - DISPLAY

CA3162	A/D Converter for 3-Digit Display
HI7131, HI7133	**$3^1/_2$ Digit Low Power, High CMRR LCD/LED Display Type A/D Converter**
ICL7106, ICL7107	$3^1/_2$ Digit LCD/LED Display A/D Converter
ICL7116, ICL7117	$3^1/_2$ Digit LCD/LED Display A/D Converter with Display Hold
ICL7126	$3^1/_2$ Digit Low Power Single-Chip A/D Converter (AnswerFAX Only) Document # 3084 See Section 12
ICL7129	$4^1/_2$ Digit LCD Single-Chip A/D Converter
ICL7136, ICL7137	$3^1/_2$ Digit LCD/LED Low Power Display A/D Converter with Overrange Recovery
ICL7139, ICL7149	$3^3/_4$ Digit Autoranging Multimeter
ICL8052/ICL71C03, ICL8068/ICL71C03	Precision $4\ ^1/_2$ Digit A/D Converter (AnswerFAX Only) Document # 3081 See Section 12

A/D CONVERTERS - FLASH

CA3304	CMOS Video Speed 4-Bit Flash A/D Converter
CA3306	CMOS Video Speed 6-Bit Flash A/D Converter
CA3318C	CMOS Video Speed 8-Bit Flash A/D Converter
HI1166	**8-Bit, 250MSPS Flash A/D Converter**
HI1276	**8-Bit, 500MSPS Flash A/D Converter**
HI1386	**8-Bit, 75MSPS Flash A/D Converter**
HI1396	**8-Bit, 125MSPS Flash A/D Converter**
HI-5700	8-Bit, 20MSPS Flash A/D Converter
HI-5701	**6-Bit, 30MSPS Flash A/D Converter**

A/D CONVERTERS - INTEGRATING

HI-7159A	Microprocessor Compatible $5^1/_2$ Digit A/D Converter
ICL7109	12-Bit Microprocessor Compatible A/D Converter
ICL7135	$4^1/_2$ Digit BCD Output A/D Converter
ICL8052/ICL7104, ICL8068/ICL7104	$^{14}/_{16}$-Bit μP-Compatible, 2-Chip A/D Converter (AnswerFAX Only) Document # 3091 See Section 12

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DATA ACQUISITION PRODUCTS (Continued)

A/D CONVERTERS - SAR

ADC0802, ADC0803, ADC0804	8-Bit μP Compatible A/D Converters
CA3310, CA3310A	CMOS 10-Bit A/D Converter with Internal Track and Hold
HI-574A, HI-674A, HI-774	Complete 12-Bit A/D Converter with Microprocessor Interface
HI5810	**CMOS 10μs 12-Bit Sampling A/D Converter with Internal Track and Hold**
HI5812	**CMOS 20μs 12-Bit Sampling A/D Converter with Internal Track and Hold**
HI5813	**CMOS 3.3V, 25μs 12-Bit Sampling A/D Converter with Internal Track and Hold**
HI7152	10-Bit High Speed A/D Converter with Track and Hold (AnswerFAX Only) Document # 3100 See Section 12
HI7151	10-Bit High Speed A/D Converter with Track and Hold (AnswerFAX Only) Document # 3099 See Section 12
ICL7112	12-Bit High-Speed CMOS μP-Compatible A/D Converter (AnswerFAX Only) Document # 3639 See Section 12
ICL7115	14-Bit High Speed CMOS μP-Compatible A/D Converter (AnswerFAX Only) Document # 3101 See Section 12

A/D CONVERTERS - SIGMA-DELTA

HI7190	**24-Bit High Precision Sigma-Delta A/D Converter**

A/D CONVERTERS - SUBRANGING

HI1175	**8-Bit, 20MSPS Flash A/D Converter**
HI1176	**8-Bit, 20MSPS Flash A/D Converter**
HI5800	**12-Bit, 3MSPS Sampling A/D Converter**
HI-7153	8 Channel, 10-Bit High Speed Sampling A/D Converter

COMMUNICATION INTERFACE

HIN230 thru HIN241	**+5V Powered RS-232 Transmitters/Receivers**
ICL232	+5V Powered Dual RS-232 Transmitter/Receiver

NOTE: Bold Type Designates a New Product from Harris.

DATA ACQUISITION PRODUCTS (Continued)

COUNTERS WITH DISPLAY DRIVERS/TIMEBASE GENERATORS

HA7210	**Low Power Crystal Oscillator**
ICM7213	One Second/One Minute Timebase Generator
ICM7216A, ICM7216B, ICM7216D	8-Digit Multi-Function Frequency Counter/Timer
ICM7217	4-Digit LED Display Programmable Up/Down Counter
ICM7224	$4^1/_2$ Digit LCD Display Counter
ICM7226A, ICM7226B	8-Digit Multi-Function Frequency Counter/Timers
ICM7249	$5^1/_2$ Digit LCD μ-Power Event/Hour Meter

D/A CONVERTERS

AD7520, AD7530, AD7521, AD7531	10-Bit, 12-Bit Multiplying D/A Converters
AD7523, AD7533	8-Bit Multiplying D/A Converters
AD7541	12-Bit Multiplying D/A Converter
AD7545	12-Bit Buffered Multiplying CMOS DAC
CA3338, CA3338A	**CMOS Video Speed 8-Bit R2R D/A Converter**
HI-562A	12-Bit High Speed Monolithic D/A Converter (AnswerFAX Only) Document # 3580 See Section 12
HI-565A	High Speed Monolithic D/A Converter with Reference
HI-DAC80V, HI-DAC85V	12-Bit, Low Cost, Monolithic D/A Converter
HI1171	**8-Bit, 40MSPS High Speed D/A Converter**
HI20201, HI20203	**10/8-Bit, 160MSPS Ultra High Speed D/A Converter**
ICL7121	16-Bit Multiplying Microprocessor-Compatible D/A Converter (AnswerFAX Only) Document # 3112 See Section 12
ICL7134	14-Bit Multiplying μP-Compatible D/A Converter AnswerFAX Only) Document # 3113 See Section 12

DISPLAY DRIVERS

CA3161	BCD to Seven Segment Decoder/Driver
ICM7211, ICM7212	4-Digit ICM7211 (LCD) and ICM7212 (LED) Display Drive
ICM7228	8-Digit μP Compatible LED Display Decoder Driver
ICM7231, ICM7232	Numeric/Alphanumeric Triplexed LCD Display Driver
ICM7243	8-Character μP-Compatible LED Display Decoder Driver

NOTE: Bold Type Designates a New Product from Harris.

LINEAR AND TELECOM PRODUCTS

COMPARATORS DATA SHEETS

CA139, CA239, CA339, LM339	Quad Voltage Comparators for Industrial, Commercial and Military Applications
CA3098	Programmable Schmitt Trigger - with Memory Dual Input Precision Level Detectors
CA3290	BiMOS Dual Voltage Comparator with MOSFET Input, Bipolar Output
HA-4900, HA-4902, HA-4905	Precision Quad Comparator
HFA-0003, HFA-0003L	**Ultra High Speed Comparator**

DIFFERENTIAL AMPLIFIERS DATA SHEETS

CA3028, CA3053	Differential/Cascode Amplifiers for Commercial and Industrial Equipment from DC to 120MHz
CA3049, CA3102	Dual High Frequency Differential Amplifiers For Low Power Applications Up 500MHz
CA3054	Transistor Array - Dual Independent Differential Amp for Low Power Applications from DC to 120MHz

OPERATIONAL AMPLIFIERS DATA SHEETS

CA124, CA224, CA324, LM324*, LM2902*	Quad Operational Amplifiers for Commercial, Industrial, and Military Applications
CA158, CA258, CA358, CA2904, LM358*, LM2904*	Dual Operational Amplifiers for Commercial Industrial, and Military Applications
CA741, CA1458, CA1558, LM741*, LM1458*, LM1558*	High Gain Single and Dual Operational Amplifiers for Military, Industrial and Commercial Applications
CA3020	Multipurpose Wide-Band Power Amps Military, Industrial and Commercial Equipment at Frequency Up to 8MHz
CA3060	Operational Transconductance Amplifier Arrays
CA3078	Micropower Operational Amplifier
CA3080	Operational Transconductance Amplifier (OTA)
CA3094	Programmable Power Switch/Amplifier for Control and General Purpose Applications
CA3100	Wideband Operational Amplifier
CA3130	BiMOS Operational Amplifier with MOSFET Input/CMOS Output
CA3140	BiMOS Operational Amplifier with MOSFET Input/Bipolar Output
CA3160	BiMOS Operational Amplifiers with MOSFET Input/CMOS Output
CA3193	BiCMOS Precision Operational Amplifiers
CA3240	Dual BiMOS Operational Amplifier with MOSFET Input/Bipolar Output
CA3260	BiMOS Operational Amplifier with MOSFET Input/CMOS Output
CA3280	Dual Variable Operational Amplifier

NOTE: Bold Type Designates a New Product from Harris.

OPERATIONAL AMPLIFIERS DATA SHEETS (Continued)

CA3420	Low Supply Voltage, Low Input Current BiMOS Operational Amplifiers
CA3440	Nanopower BiMOS Operational Amplifier
CA3450	Video Line Driver, High Speed Operational Amplifier
CA5130	BiMOS Microprocessor Operational Amplifier with MOSFET Input/CMOS Output
CA5160	BiMOS Microprocessor Operational Amplifiers with MOSFET Input/CMOS Output
CA5260	BiMOS Microprocessor Operational Amplifiers with MOSFET Input/CMOS Output
CA5420	Low Supply Voltage, Low Input Current BiMOS Operational Amplifier
CA5470	Quad Microprocessor BiMOS-E Operational Amplifiers with MOSFET Input/Bipolar Output
HA-2400, HA-2404, HA-2405	PRAM Four Channel Programmable Amplifiers
HA-2406	Digitally Selectable Four Channel Operational Amplifier
HA-2444	**Selectable, Four Channel Video Operational Amplifier**
HA-2500, HA-2502, HA-2505	Precision High Slew Rate Operational Amplifiers
HA-2510, HA-2512, HA-2515	High Slew Rate Operational Amplifiers
HA-2520, HA-2522, HA-2525	Uncompensated High Slew Rate Operational Amplifiers
HA-2529	Uncompensated, High Slew Rate High Output Current, Operational Amplifier
HA-2539	Very High Slew Rate Wideband Operational Amplifier
HA-2540	Wideband, Fast Settling Operational Amplifier
HA-2541	Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier
HA-2542	Wideband, High Slew Rate, High Output Current Operational Amplifier
HA-2544	Video Operational Amplifier
HA-2548	Precision, High Slew Rate, Wideband Operational Amplifier
HA-2600, HA-2602, HA-2605	Wideband, High Impedance Operational Amplifiers
HA-2620, HA-2622, HA-2625	Very Wideband, Uncompensated Operational Amplifiers
HA-2640, HA-2645	High Voltage Operational Amplifiers
HA-2705	Low Power, High Performance Operational Amplifier
HA-2839	**Very High Slew Rate Wideband Operational Amplifier**
HA-2840	**Very High Slew Rate Wideband Operational Amplifier**
HA-2841	**Wideband, Fast Settling, Unity Gain Stable, Video Operational Amplifier**
HA-2842	**Wideband, High Slew Rate, High Output Current, Video Operational Amplifier**
HA-2850	**Low Power, High Slew Rate Wideband Operational Amplifier**

NOTE: Bold Type Designates a New Product from Harris.

TELECOMMUNICATIONS DATA SHEETS (Continued)

CD22204	5V Low Power Subscriber DTMF Receiver
CD22301	Monolithic Pan Repeater
CD22354A, CD22357A	CMOS Single-Chip, Full-Feature PCM CODEC
CD22M3493	**12 x 8 x 1 BiMOS-E Crosspoint Switch**
CD22M3494	**16 x 8 x 1 BiMOS-E Crosspoint Switch**
CD22859	Monolithic Silicon COS/MOS Dual-Tone Multifrequency Tone Generator
CD74HC22106, CD74HCT22106	QMOS 8 x 8 x 1 Crosspoint Switch with Memory Control
HC-5502B	**SLIC Subscriber Line Interface Circuit**
HC-5504B	**SLIC Subscriber Line Interface Circuit**
HC-5504DLC	SLIC Subscriber Line Interface Circuit
HC-5509A1	**SLIC Subscriber Line Interface Circuit**
HC-5509B	**SLIC Subscriber Line Interface Circuit**
HC-5524	SLIC Subscriber Line Interface Circuit
HC-5560	PCM Transcoder
HC-55536	Continuous Variable Slope Delta-Demodulator (CVSD)
HC-55564	Continuously Variable Slope Delta-Modulator (CVSD)

TRANSISTOR ARRAY DATA SHEETS

CA3018	General Purpose Transistor Arrays
CA3039	Diode Array
CA3045, CA3046	General Purpose N-P-N Transistor Arrays
CA3081, CA3082	General Purpose High Current N-P-N Transistor Arrays
CA3083	General Purpose High Current N-P-N Transistor Array
CA3086	General Purpose N-P-N Transistor Array
CA3096	N-P-N/P-N-P Transistor Array
CA3127	High Frequency N-P-N Transistor Array
CA3141	High-Voltage Diode Array For Commercial, Industrial & Military Applications
CA3146, CA3183	High-Voltage Transistor Arrays
CA3227, CA3246	High-Frequency N-P-N Transistor Arrays For Low-Power Applications at Frequencies Up to 1.5GHz
HFA3046, HFA3096, HFA3127, HFA3128	**Ultra High Frequency Transistor Array**

NOTE: Bold Type Designates a New Product from Harris.

DSP 2

MULTIPLIERS

HMA510

16 x 16-Bit CMOS Parallel Multiplier Accumulator

January 1994

Features

- 16 x 16-bit Parallel Multiplication with Accumulation to a 35-Bit Result
- High-Speed (45ns) Multiply Accumulate Time
- Low Power CMOS Operation:
  - I_{CCSB} = 500μA Maximum
  - I_{CCOP} = 7.0mA Maximum at 1.0MHz
- HMA510 is Compatible with the CY7C510 and the IDT7210
- Supports Two's Complement or Unsigned Magnitude Operations
- TTL Compatible Inputs/Outputs
- Three-State Outputs

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HMA510JC-45	0°C to +70°C	68 Lead PLCC
HMA510JC-55	0°C to +70°C	68 Lead PLCC
HMA510GC-55	0°C to +70°C	68 Lead PGA

Description

The HMA510 is a high speed, low power CMOS 16 x 16-bit parallel multiplier accumulator capable of operating at 45ns clocked multiply-accumulate cycles. The 16-bit X and Y operands may be specified as either two's complement or unsigned magnitude format. Additional inputs are provided for the accumulator functions which include: loading the accumulator with the current product, adding or subtracting the accumulator contents and the current product, and pre-loading the accumulator registers from the external inputs.

All inputs and outputs are registered. The registers are all positive edge triggered, and are latched on the rising edge of the associated clock signal. The 35-bit accumulator output register is broken into three parts. The 16-bit least significant product (LSP), the 16-bit most significant product (MSP), and the 3-bit extended product (XTP) registers. The XTP and MSP registers have dedicated output ports, while the LSP register shares the Y-inputs in a multiplexed fashion. The entire 35-bit accumulator output register may be pre-loaded at any time through the use of the bidirectional output ports and the preloaded control.

Block Diagram

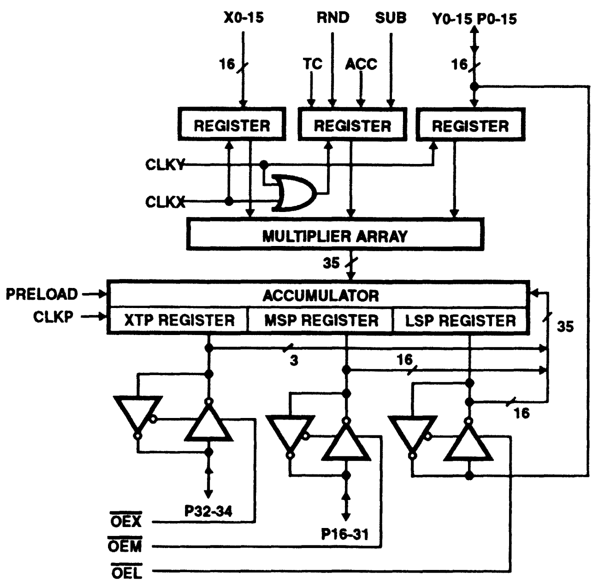


TABLE 2. HMA510/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	-55 MIN	-55 MAX	-65 MIN	-65 MAX	-75 MIN	-75 MAX	UNITS
Multiply Accumulate Time	T_{MA}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	55	-	65	-	75	ns
Input Setup Time	T_S		9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	25	-	25	-	ns
Clock HIGH Pulse Width	T_{PWH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	25	-	25	-	ns
Clock LOW Pulse Width	T_{PWL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	25	-	25	-	ns
Output Delay	T_D		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	30	-	35	-	35	ns
3-State Enable Time	T_{ENA}	(Note 2)	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	30	-	30	-	35	ns

NOTES:

1. AC Testing as follows: V_{CC} = 4.5V and 5.5V. Input levels 0V and 3.0V (0V and 3.2V for clock inputs). Timing reference levels = 1.5V, Output load per test load circuit, with V_1 = 2.4V, R_1 = 500Ω and C_L = 40pF.
2. Transition is measured at ±200mV from steady state voltage, Output loading per test load circuit, with V_1 = 1.5V, R_1 = 500Ω and C_L = 40pF.

TABLE 3. HMA510/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	-55 MIN	-55 MAX	-65 MIN	-65 MAX	-75 MIN	-75 MAX	UNITS
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	10	-	10	-	10	pF
Output Capacitance	C_{OUT}		1	$T_A = +25^oC$	-	10	-	10	-	10	pF
I/O Capacitance	$C_{I/O}$		1	$T_A = +25^oC$	-	15	-	15	-	15	pF
Input Hold Time	T_H		1	$-55^oC \le T_A \le +125^oC$	3	-	3	-	3	-	ns
3-State Disable Time	T_{DIS}		1	$-55^oC \le T_A \le +125^oC$	-	30	-	30	-	30	ns
Output Rise Time	T_R	From 0.8V to 2.0V	1	$-55^oC \le T_A \le +125^oC$	-	10	-	10	-	10	ns
Output Fall Time	T_F	From 2.0V to 0.8V	1	$-55^oC \le T_A \le +125^oC$	-	10	-	10	-	10	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Burn-In Circuit

68 LEAD PIN GRID ARRAY TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L
11		N/C	X15	RND	ACC	CLKY	TC	PREL	CLKP	P33	
10	X13	X14	$\overline{OEL}$	SUB	CLKX	V_{CC}	$\overline{OEX}$	$\overline{OEM}$	P34	P32	N/C
9	X11	X12								P30	P31
8	X9	X10								P28	P29
7	X7	X8								P26	P27
6	X5	X6								P24	P25
5	X3	X4								P22	P23
4	X1	X2								P20	P21
3	Y0/P0	X0								P18	P19
2	N/C	Y1/P1	Y3/P3	Y5/P5	Y7/P7	Y8/P8	Y10/P10	Y12/P12	Y14/P14	P16	P17
1		Y2/P2	Y4/P4	Y6/P6	GND	Y9/P9	Y11/P11	Y13/P13	Y15/P15	N/C	

PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
B6	X6	F1	F1	Y9/P9	F2	K7	P26	$V_{CC}/2$	E11	ACC	F1
A6	X5	F2	G2	Y10/P10	F3	L7	P27	$V_{CC}/2$	D10	SUB	F2
B5	X4	F3	G1	Y11/P11	F5	K8	P28	$V_{CC}/2$	D11	RND	F3
A5	X3	F4	H2	Y12/P12	F4	L8	P29	$V_{CC}/2$	C10	$\overline{OEL}$	V_{CC}
B4	X2	F5	H1	Y13/P13	F4	K9	P30	$V_{CC}/2$	C11	X15	F8
A4	X1	F6	J2	Y14/P14	F8	L9	P31	$V_{CC}/2$	B10	X14	F9
B3	X0	F7	J1	Y15/P15	F9	K10	P32	$V_{CC}/2$	A10	X13	F10
A3	Y0/P0	F8	K2	P16	$V_{CC}/2$	K11	P33	$V_{CC}/2$	B9	X12	F11
B2	Y1/P1	F9	L2	P17	$V_{CC}/2$	J10	P34	$V_{CC}/2$	A9	X11	F12
B1	Y2/P2	F10	K3	P18	$V_{CC}/2$	J11	CLKP	F0	B8	X10	F13
C2	Y3/P3	F11	L3	P19	$V_{CC}/2$	H10	$\overline{OEM}$	GND	A8	X9	F14
C1	Y4/P4	F12	K4	P20	$V_{CC}/2$	H11	PREL	F6	B7	X8	F15
D2	Y5/P5	F13	L4	P21	$V_{CC}/2$	G10	$\overline{OEX}$	GND	A7	X7	F7
D1	Y6/P6	F14	K5	P22	$V_{CC}/2$	G11	TC	F5	A2	N.C.	N.C.
E2	Y7/P7	F15	L5	P23	$V_{CC}/2$	F10	V_{CC}	V_{CC}	K1	N.C.	N.C.
E1	GND	GND	K6	P24	$V_{CC}/2$	F11	CLKY	F0	L10	N.C.	N.C.
F2	Y8/P8	F1	L6	P25	$V_{CC}/2$	E10	CLKX	F0	B11	N.C.	N.C.

NOTES:

1. V_{CC} = 5.5V +0.5V/-0.0V with 0.1μF decoupling capacitor to GND
2. F0 = 100kHz, F1 = F0/2, F2 = F1/2, ..., 10%
3. $V_{IH} = V_{CC}$ - 1V ± 0.5V (Min), V_{IL} = 0.8V (Max)
4. 47kΩ load resistors used on all pins except V_{CC} and GND (Pin-Grid identifiers F10, G10, G11 and H11)

Die Characteristics

DIE DIMENSIONS:
184 x 176 x 19 ± 1mils

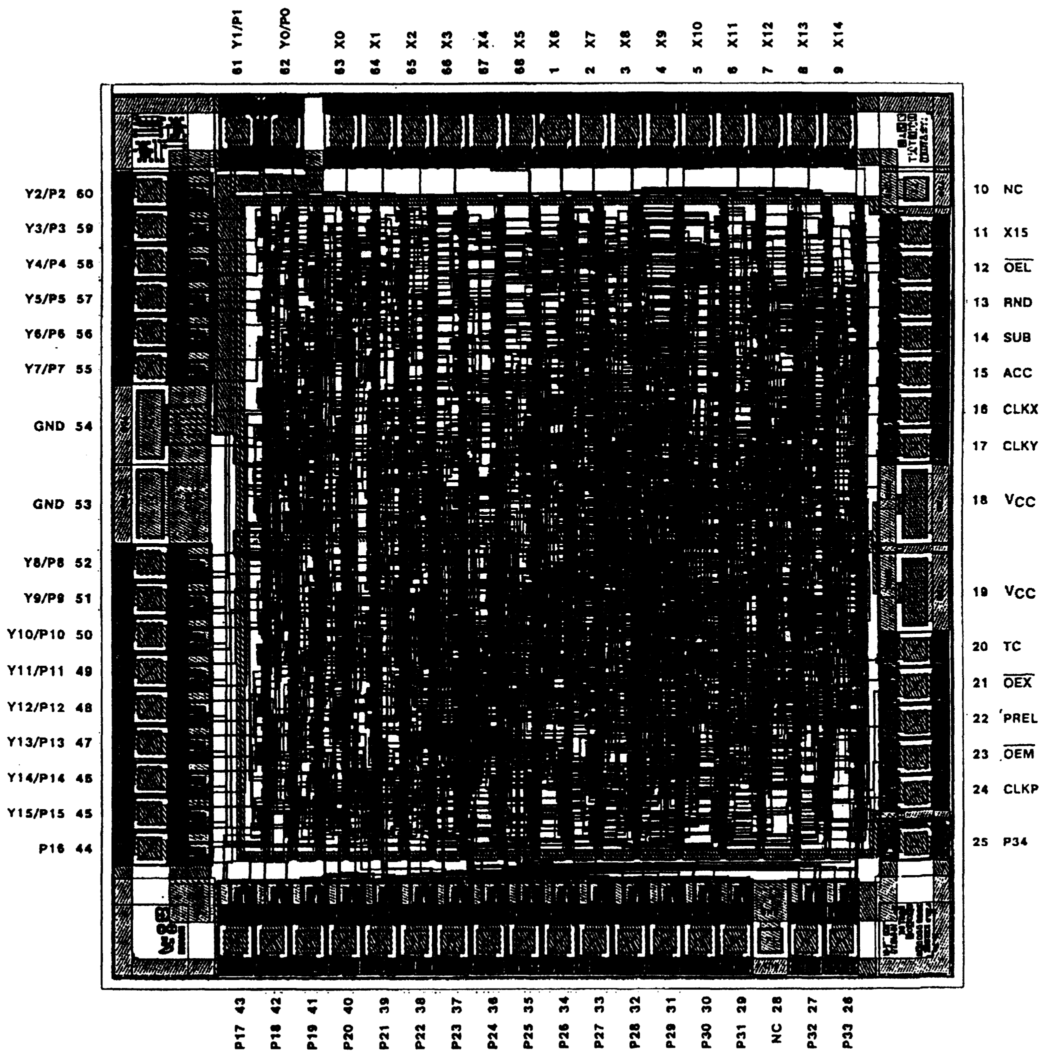
METALLIZATION:
Type: Si - Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY: $0.9 \times 10^5 A/cm^2$

Metallization Mask Layout

HMA510/883



HARRIS SEMICONDUCTOR

HMU16, HMU17

January 1994

16 x 16-Bit CMOS Parallel Multipliers

Features

- **16 x 16-Bit Parallel Multiplier with Full 32-Bit Product**
- **High-Speed (35ns) Clocked Multiply Time**
- **Low Power Operation:**
  - **I_{CCSB} = 500μA Maximum**
  - **I_{CCOP} = 7.0mA Maximum at 1MHz**
- **Supports Two's Complement, Unsigned Magnitude and Mixed Mode Multiplication**
- **HMU16 is Compatible with the AM29516, LMU16, IDT7216 and the CY7C516**
- **HMU17 is Compatible with the AM29517, LMU17, IDT7217 and the CY7C517**
- **TTL Compatible Inputs/Outputs**
- **Three-State Outputs**

Applications

- **Fast Fourier Transform Analysis**
- **Digital Filtering**
- **Graphic Display Systems**
- **Image Processing**
- **Radar and Sonar**
- **Speech Synthesis and Recognition**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HMU16JC-35	0°C to +70°C	68 Lead PLCC
HMU16JC-45	0°C to +70°C	68 Lead PLCC
HMU16GC-35	0°C to +70°C	68 Lead PGA
HMU16GC-45	0°C to +70°C	68 Lead PGA
HMU17JC-35	0°C to +70°C	68 Lead PLCC
HMU17JC-45	0°C to +70°C	68 Lead PLCC
HMU17GC-35	0°C to +70°C	68 Lead PGA
HMU17GC-45	0°C to +70°C	68 Lead PGA

Description

The HMU16 and HMU17 are high speed, low power CMOS 16 x 16-bit multipliers ideal for fast, real time digital signal processing applications.

The X and Y operands along with their mode controls (TCX and TCY) have 17-bit input registers. The mode controls independently specify the operands as either two's complement or unsigned magnitude format, thereby allowing mixed mode multiplication operations.

Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP). For asynchronous output these registers may be made transparent through the use of the feedthrough control (FT).

Additional inputs are provided for format adjustment and rounding. The format adjust control (FA) allows the user to select either a left shifted 31-bit product or a full 32-bit product, whereas the round control (RND) provides the capability of rounding the most significant portion of the result.

The HMU16 has independent clocks (CLKX, CLKY, CLKL, CLKM) associated with each of these registers to maximize throughput and simplify bus interfacing. The HMU17 has only a single clock input (CLK), but makes use of three register enables ($\overline{ENX}$, $\overline{ENY}$ and $\overline{ENP}$). The $\overline{ENX}$ and $\overline{ENY}$ inputs control the X and Y input registers, while $\overline{ENP}$ controls both the MSP and LSP output registers. This configuration facilitates the use of the HMU17 for microprogrammed systems.

The two halves of the product may be routed to a single 16-bit three-state output port via a multiplexer, and in addition, the LSP is connected to the Y-input port through a separate three-state buffer.

All outputs of the HMU16 and HMU17 multipliers also offer three-state control for multiplexing results onto multiuse busses.

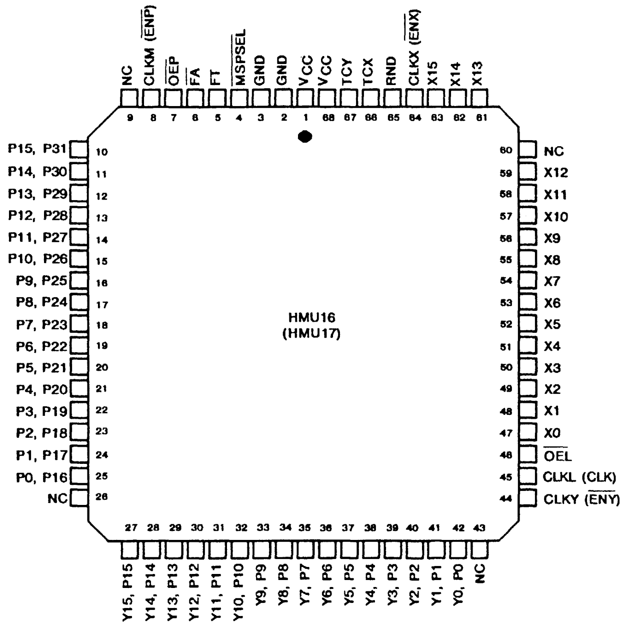
Package Pinouts

CERAMIC 68 PIN GRID ARRAY (PGA)
TOP VIEW

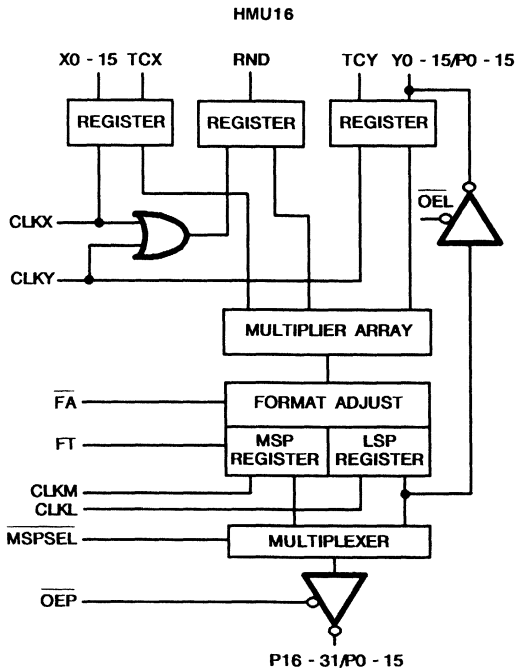
	A	B	C	D	E	F	G	H	J	K	L
11		N/C	X13	X15	RND	TCY	V_{CC}	GND	FT	$\overline{OEP}$	
10	X11	X12	X14	CLKX ($\overline{ENX}$)	TCX	V_{CC}	GND	$\overline{MSPSEL}$	$\overline{FA}$	CLKM ($\overline{ENP}$)	N/C
9	X9	X10								P30/ P14	P31/ P15
8	X7	X8								P28/ P12	P29/ P13
7	X5	X6								P26/ P10	P27/ P11
6	X3	X4								P24/ P8	P25/ P9
5	X1	X2								P22/ P6	P23/ P7
4	$\overline{OEL}$	X0								P20/ P4	P21/ P5
3	CLKY ($\overline{ENY}$)	CLKL (CLK)								P18/ P2	P19/ P3
2	N/C	Y0/ P0	Y2/ P2	Y4/ P4	Y6/ P6	Y8/ P8	Y10/ P10	Y12/ P12	Y14/ P14	P16/ P0	P17/ P1
1		Y1/ P1	Y3/ P3	Y5/ P5	Y7/ P7	Y9/ P9	Y11/ P11	Y13/ P13	Y15/ P15	N/C	

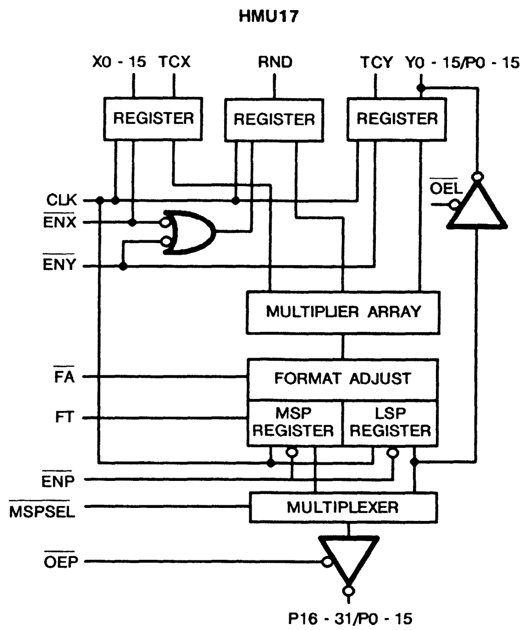
68 LEAD
PIN GRID ARRAY
TOP VIEW

68 PIN PLASTIC LEADED CHIP CARRIER (PLCC)
TOP VIEW



Functional Block Diagram





2
MULTIPLIERS

Pin Description

SYMBOL	PLCC PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	1, 68		V_{CC}. The +5V power supply pins. A 0.1µF capacitor between the V_{CC} and GND pins is recommended.
GND	2, 3		GND. The device ground.
X0-X15	47-59, 61-63	I	X-Input Data. These 16 data inputs provide the multiplicand which may be in two's complement or unsigned magnitude format.
Y0-Y15/ P0-P15	27-42	I/O	Y-Input/LSP Output Data. This 16-Bit port is used to provide the multiplier which may be in two's complement or unsigned magnitude format. It may also be used for output of the Least Significant Product (LSP).
P16-P31/ P0-P15	10-25	O	Output Data. This 16-Bit port may provide either the MSP (P16-31) or the LSP (P0-15).
TCY, TCX	66, 67	I	Two's Complement Control. Input data is interpreted as two's complement when this control is HIGH. A LOW indicates the data is to be interpreted as unsigned magnitude format.
FT	5	I	Feedthrough Control. When this control is HIGH, both the MSP and LSP registers are transparent. When LOW, the registers are latched by their associated clock signals.
FA	6	I	Format Adjust Control. A full 32-bit product is selected when this control line is HIGH. A LOW on this control line selects a left shifted 31-bit product with the sign bit replicated in the LSP. This control is normally HIGH except for certain two's complement integer and fractional applications.
RND	65	I	Round Control. When this control is HIGH, a one is added to the Most Significant Bit (MSB) of the LSP. This position is dependent on the FA control; FA = HIGH indicates RND adds to the 2-15 bit (P15), and FA = LOW indicates RND adds to the 2^{-16} bit (P14).
$\overline{\text{MSPSEL}}$	4	I	Output Multiplexer Control. When this control is LOW, the MSP is available for output at the dedicated output port, and the LSP is available at the Y-input/LSP output port. When $\overline{\text{MSPSEL}}$ is HIGH, the LSP is available at both ports and the MSP is not available for output.
$\overline{\text{OEL}}$	46	I	Y-In/P0-15 Output Port Three-state Control. When $\overline{\text{OEL}}$ is HIGH, the output drivers are in the high impedance state. This state is required for Y-data input. When $\overline{\text{OEL}}$ is LOW, the port is enabled for LSP output.
$\overline{\text{OEP}}$	7	I	P16-31/P0-15 Output Port Three-state Control. A LOW on this control line enables the output port. When $\overline{\text{OEP}}$ is HIGH, the output drivers are in the high impedance state.
The following Pin Descriptions apply to the HMU16 only.			
CLKX	64	I	X-Register Clock. The rising edge of this clock loads the X-data input register along with the TCX and RND registers.
CLKY	44	I	Y-Register Clock. The rising edge of this clock loads the Y-data input register along with the TCY and RND registers.
CLKM	8	I	MSP Register Clock. The rising edge of CLKM loads the most significant product (MSP) register.
CLKL	45	I	LSP Register Clock. The rising edge of CLKL loads the least significant product (LSP) register.
The following Pin Descriptions apply to the HMU17 only.			
CLK	45	I	Clock. The rising edge of this clock will load all enabled registers.
$\overline{\text{ENX}}$	64	I	X-Register Enable. When $\overline{\text{ENX}}$ is LOW, the X-register is enabled; X-input data and TCX will be latched at the rising edge of CLK. When $\overline{\text{ENX}}$ is high, the X-register is in a hold mode.
$\overline{\text{ENY}}$	44	I	Y-Register Enable. $\overline{\text{ENY}}$ enables the Y-register. (See $\overline{\text{ENX}}$).
$\overline{\text{ENP}}$	8	I	Product Register Enable. $\overline{\text{ENP}}$ enables the product register. Both the MSP and LSP sections are enabled by $\overline{\text{ENP}}$. (See $\overline{\text{ENX}}$).

Functional Description

The HMU16/HMU17 are high speed 16 X 16-bit multipliers designed to perform very fast multiplication of two 16-bit binary numbers. The two 16-bit operands (X and Y) may be independently specified as either two's complement or unsigned magnitude format by the two's complement controls (TCX and TCY). When either of these control lines is LOW, the respective operand is treated as an unsigned 16-bit value; and when it is HIGH, the operand is treated as a signed value represented in two's complement format. The operands along with their respective controls are latched at the rising edge of the associated clock signal. The HMU16 accomplishes this through the use of independent clock inputs for each of the input registers (CLKX and CLKY), while the HMU17 utilizes a single clock signal (CLK) along with the X and Y register enable inputs ($\overline{\text{ENX}}$ and $\overline{\text{ENY}}$).

Input controls are also provided for rounding and format adjustment of the 32-bit product. The Round input (RND) is provided to accomodate rounding of the most significant portion of the product by adding one to the Most Significant Bit (MSB) of the LSP register. The position of the MSB is dependent on the state of the Format Adjust Control (See Pin Descriptions and Multiplier Input/Output Format Tables). The Round input is latched into the RND register whenever either of the input registers is clocked. The Format Adjust control ($\overline{\text{FA}}$) allows the product output to be formatted. When the $\overline{\text{FA}}$ control is HIGH, a full 32-bit product is output; and when $\overline{\text{FA}}$ is LOW, a left-shifted 31-bit product is output with the sign bit replicated in bit position 15 of the LSP. The $\overline{\text{FA}}$ control must be HIGH for unsigned magnitude, and mixed mode multiplication operations. It may be LOW for certain two's complement integer and fractional operations only (See Multiplier Input/Output Formats Table).

The HMU16/HMU17 multipliers are equipped with two 16-bit output registers (MSP and LSP) which are provided to hold the most and least significant portions of the resultant product respectively. The HMU16 uses independent clocks (CLKM and CLKL) for latching the two output registers, while the HMU17 uses a single clock input (CLK) along with the Product Latch Enable ($\overline{\text{ENP}}$). The MSP and LSP registers may also be made transparent for asynchronous output through the use of the Feedthrough control (FT).

There are two output configurations which may be selected when using the HMU16/HMU17 multipliers. The first configuration allows the simultaneous access of the most and least significant halves of the product. When the $\overline{\text{MSPSEL}}$ input is LOW, the Most Significant Product will be available at the dedicated output port (P16-31/P0-15). The Least Significant Product is simultaneously available at the bi-directional port shared with the Y-inputs (Y0-15/P0-15) through the use of the LSP output enable ($\overline{\text{OEL}}$). The other output configuration involves multiplexing the MSP and LSP registers onto the dedicated output port through the use of the $\overline{\text{MSPSEL}}$ control. When the $\overline{\text{MSPSEL}}$ control is LOW, the Most Significant Product will be available at the dedicated output port; and when $\overline{\text{MSPSEL}}$ is HIGH, the Least Significant Product will be available at this port. This configuration allows access of the entire 32-bit product by a 16-bit wide system bus.

Multiplier Input/Output Formats Table

FRACTIONAL TWO'S COMPLEMENT NOTATION

BINARY POINT

SIGNAL	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
DIGIT VALUE	-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

x

SIGNAL	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
DIGIT VALUE	-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

* =

SIGNAL	P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
DIGIT VALUE (FA = 0)	-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	-2^0	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}
	MSP																LSP															

=

SIGNAL	P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
DIGIT VALUE (FA = 1)	-2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}
	MSP																LSP															

* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000 . . . 0 with 1,000 . . . 0 yielding an erroneous product of −1 in the fraction case and -2^{30} in the integer case.

FRACTIONAL UNSIGNED MAGNITUDE NOTATION

BINARY POINT

SIGNAL	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
DIGIT VALUE	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

x

SIGNAL	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
DIGIT VALUE	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

=

SIGNAL	P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
DIGIT VALUE (FA = 1 MANDATORY)	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}	2^{-32}
	MSB																LSP															

FRACTIONAL MIXED MODE NOTATION

BINARY POINT

SIGNAL (TWO'S COMPLEMENT)	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
DIGIT VALUE	-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

x

SIGNAL (UNSIGNED MAGNITUDE)	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
DIGIT VALUE	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

=

SIGNAL	P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
DIGIT VALUE (FA = 1 MANDATORY)	-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}
	MSB																LSP															

Multiplier Input/Output Formats Table (Continued)

INTEGER TWO'S COMPLEMENT NOTATION

BINARY POINT

SIGNAL	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
DIGIT VALUE	-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

x

SIGNAL	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
DIGIT VALUE	-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

* =

SIGNAL	P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
DIGIT VALUE	-2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	-2^{30}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSP | LSP — FA = 0

=

SIGNAL	P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
DIGIT VALUE	-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSP | LSP — FA = 1

* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000 . . . 0 with 1,000 . . . 0 yielding an erroneous product of −1 in the fraction case and -2^{30} in the integer case.

INTEGER UNSIGNED MAGNITUDE NOTATION

BINARY POINT

SIGNAL	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
DIGIT VALUE	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

x

SIGNAL	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
DIGIT VALUE	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

=

SIGNAL	P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
DIGIT VALUE	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSP | LSP — FA = 1 MANDATORY

INTEGER MIXED MODE NOTATION

BINARY POINT

SIGNAL (TWO'S COMPLEMENT)	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
DIGIT VALUE	-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

x

SIGNAL (UNSIGNED MAGNITUDE)	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
DIGIT VALUE	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

=

SIGNAL	P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
DIGIT VALUE	-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSP | LSP — FA = 1 MANDATORY

Absolute Maximum Ratings

Supply Voltage	+8.0 Volts
Input, Output or I/O Voltage Applied	GND−0.5V to V_{CC}+0.5V
Storage Temperature Range	−65°C to +150°C
Gate Count	4500 Gates
θ_{ja}	43.2°C/W (PLCC), 42.69°C/W (PGA)
θ_{jc}	15.1°C/W (PLCC), 10.0°C/W (PGA)
Maximum Package Power Dissipation at 70°C	1.7W (PLCC), 2.46 (PGA)
Junction Temperature	+150°C (PLCC), +175°C (PGA)
Lead Temperature (Soldering, Ten Seconds)	+300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating, and operation at these or any other conditions above those indicated in the operations sections of this specification is not implied.

Operating Conditions

Operating Voltage Range	+4.75V to +5.25V
Operating Temperature Range	0°C to +70°C

D.C. Electrical Specifications (V_{CC} = 5.0V + 5%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0	-	V	V_{CC} = 5.25V
V_{IL}	Logical Zero Input Voltage	-	0.8	V	V_{CC} = 4.75V
V_{OH}	Output High Voltage	2.6	-	V	I_{OH} = −400μA, V_{CC} = 4.75V
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = +4.0mA, V_{CC} = 4.75V
I_I	Input Leakage Current	-10	10	μA	V_I = V_{CC} or GND, V_{CC} = 5.25V
I_O	Output or I/O Leakage Current	-10	10	μA	V_O = V_{CC} or GND, V_{CC} = 5.25V
I_{CCSB}	Standby Power Supply Current	-	500	μA	V_I = V_{CC} or GND, V_{CC} = 5.25V Outputs Open
I_{CCOP}	Operating Power Supply Current	-	7.0	mA	V_I = V_{CC} or GND, V_{CC} = 5.25V f = 1MHz (Note 1)

Capacitance (T_A = +25°C, Note 2)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	15	pF	Frequency = 1MHz. All measurements referenced to device Ground.
C_{OUT}	Output Capacitance	10	pF	
$C_{I/O}$	I/O Capacitance	10	pF	

NOTES:

1. Operating Supply Current is proportional to frequency, Typical rating is 5mA/MHz.
2. Not tested, but characterized at initial design and at major process/ design changes.

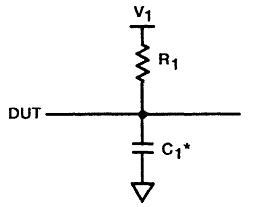
A.C. Electrical Specifications (V_{CC} = 5.0V + 5%, T_A = 0°C to +70°C, Note 3)

SYMBOL	PARAMETER	HMU16/HMU17-35		HMU16/HMU17-45		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
T_{MUC}	Unclocked Multiply Time	-	55	-	70	ns	
T_{MC}	Clocked Multiply Time	-	35	-	45	ns	
T_S	X, Y, RND Setup Time	15	-	18	-	ns	
T_H	X, Y, RND Hold Time	2	-	2	-	ns	
T_{PWH}	Clock Pulse Width High	10	-	15	-	ns	
T_{PWL}	Clock Pulse Width Low	10	-	15	-	ns	
T_{PDSEL}	$\overline{\text{MSPSEL}}$ to Product Out	-	22	-	25	ns	
T_{PDP}	Output Clock to P	-	22	-	25	ns	
T_{PDY}	Output Clock to Y	-	22	-	25	ns	
T_{ENA}	3-State Enable Time	-	22	-	25	ns	Note 1
T_{DIS}	3-State Disable Time	-	22	-	25	ns	
T_{SE}	Clock Enable Setup Time (HMU17 only)	15	-	15	-	ns	
T_{HE}	Clock Enable Hold Time (HMU17 only)	2	-	2	-	ns	
T_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (HMU16 only)	0	-	0	-	ns	Note 2
T_R	Output Rise Time	-	8	-	8	ns	From 0.8V to 2.0V
T_F	Output Fall Time	-	8	-	8	ns	From 2.0V to 0.8V

NOTES:

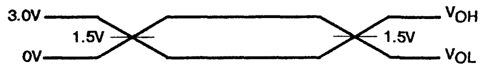
1. Transition is measured at ±200mV from steady state voltage with loading specified in A.C. Test Circuit, V_1 = 1.5V, R_1 = 500Ω and C_1 = 40pF
2. To ensure the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.
3. Refer to A.C. Test Circuit, with V_1 = 2.4V, R_1 = 500Ω and C_1 = 40pF

A.C. Test Circuit



* Includes Stray and Jig Capacitance

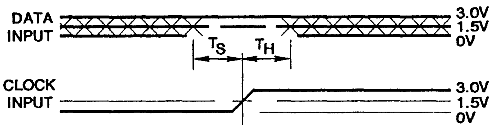
A.C. Testing Input, Output Waveforms



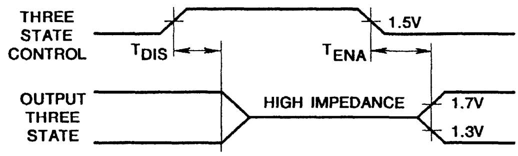
A.C. Testing: All parameters tested as per test circuit. Input rise and fall times are driven at 1ns/V.

Timing Diagram

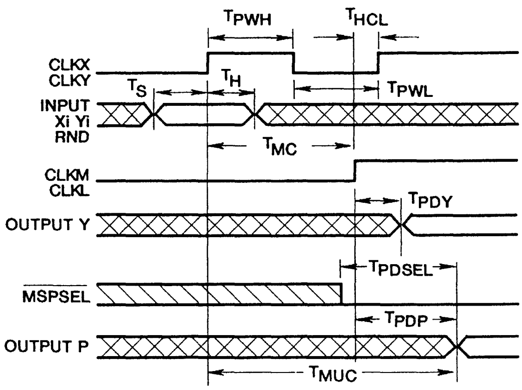
SET-UP AND HOLD TIME



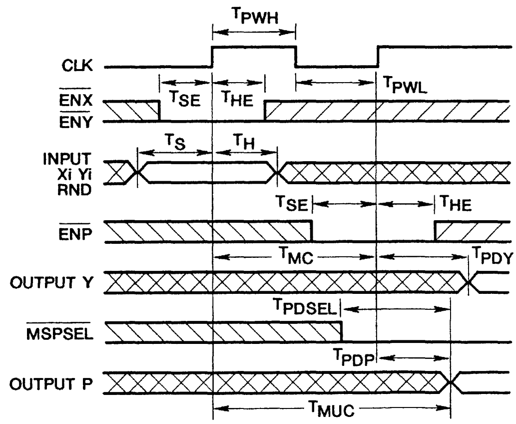
THREE STATE CONTROL



HMU16 TIMING DIAGRAM



HMU17 TIMING DIAGRAM



HARRIS SEMICONDUCTOR

HMU16/883

January 1994

16 x 16-Bit CMOS Parallel Multiplier

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- 16 x 16-Bit Parallel Multiplier with Full 32-Bit Product
- High-Speed (45ns) Clocked Multiply Time
- Low Power CMOS Operation
  - I_{CCSB} = 500μA Maximum
  - I_{CCOP} = 7.0mA Maximum at 1MHz
- HMU16/883 is Compatible with the AM29516, LMU16, IDT7216, and the CY7C516
- Supports Two's Complement, Unsigned Magnitude and Mixed Mode Multiplication
- TTL Compatible Inputs/Outputs
- Three-State Outputs

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HMU16GM-45/883	-55°C to +125°C	68 Lead PGA
HMU16GM-60/883	-55°C to +125°C	68 Lead PGA

Description

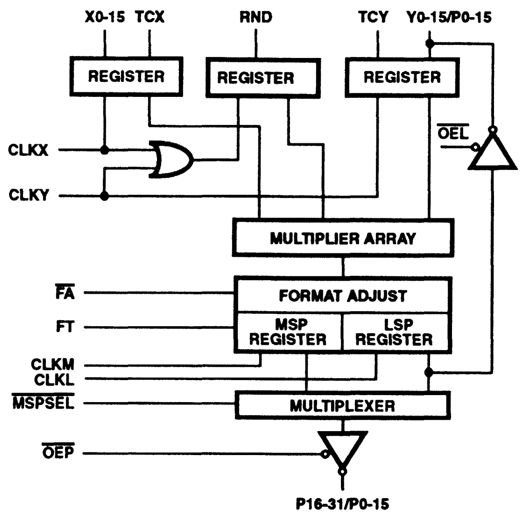
The HMU16/883 is a high speed, low power CMOS 16 x 16-bit parallel multiplier ideal for fast, real time digital signal processing applications. The 16-bit X and Y operands may be independently specified as either two's complement or unsigned magnitude format, thereby allowing mixed mode multiplication operations.

Additional inputs are provided to accommodate format adjustment and rounding of the 32-bit product. The Format Adjust control allows the user to select a 31-bit product with the sign bit replicated in the LSP. The Round control provides for rounding the most significant portion of the result by adding one to the most significant bit of the LSP.

Two 16-bit output registers (MSP and LSP) are provided to hold the most and least significant portions of the result, respectively. These registers may be made transparent for asynchronous operation through the use of the feedthrough control (FT). The two halves of the product may be routed to a single 16-bit three-state output port via the output multiplexer control, and in addition, the LSP is connected to the Y-input port through a separate three-state buffer.

The HMU16/883 utilizes independent clock signals (CLKX, CLKY, CLKL, CLKM) to latch the input operands and output product registers. This configuration maximizes throughput and simplifies bus interfacing. All outputs of the HMU16/883 also offer three-state control for multiplexing onto multiuse system busses.

Functional Diagram



2 MULTIPLIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2804.2

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input or Output Voltage Applied .... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering 10 sec) .... 300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic PGA Package	42.69°C/W	10.0°C/W

Maximum Package Power Dissipation at +125°C
Ceramic PGA Package .... 1.17 Watt
Gate Count .... 4500 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range .... -55°C to +125°C

TABLE 1. HMU16/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400μA V_{CC} = 4.5V (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +4.0mA V_{CC} = 4.5V (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-10	+10	μA
Output or I/O Leakage Current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-10	+10	μA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	500	μA
Operating Power Supply Current	I_{CCOP}	f = 1.0MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.5V (Note 2)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	7.0	mA
Functional Test	FT	(Note 3)	7, 8	$-55°C \leq T_A \leq +125°C$	-	-	

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 5mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH} (Clock Inputs) = 3.0, V_{IH} (All other inputs) = 2.6, V_{IL} = 0.4, $V_{OH} \geq$ 1.5V, and $V_{OL} \leq$ 1.5V.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. HMU16/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	-45 MIN	-45 MAX	-60 MIN	-60 MAX	UNITS
Unclocked Multiply Time	T_{MUC}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	70	-	90	ns
Clocked Multiply Time	T_{MC}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	45	-	60	ns
X, Y, RND Setup Time	T_S		9, 10, 11	$-55^oC \le T_A \le +125^oC$	18	-	20	-	ns
Clock HIGH Pulse Width	T_{PWH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	20	-	ns
Clock LOW Pulse Width	T_{PWL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	20	-	ns
MSPSEL to Product Out	T_{PDSEL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	25	-	30	ns
Output Clock to P	T_{PDP}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	25	-	30	ns
Output Clock to Y	T_{PDY}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	25	-	30	ns
3-State Enable Time	T_{ENA}	(Note 2)	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	25	-	30	ns
Clock Low Hold Time CLKXY Relative to CLKML	T_{HCL}	(Note 3)	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns

NOTES:

1. AC Testing as follows: V_{CC} = 4.5V and 5.5V. Input levels 0V and 3.0V, Timing reference levels = 1.5V, Output load per test load circuit, with V_1 = 2.4V, R_1 = 500Ω and C_L = 40pF.
2. Transition is measured at ± 200 mV from steady state voltage, Output loading per test load circuit, with V_1 = 1.5V, R_1 = 500Ω and C_L = 40pF.
3. To ensure the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.

TABLE 3. HMU16/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	-45		-60		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz All Measurements are referenced to device GND.	1	$T_A = +25^oC$	-	15	-	15	pF
Output Capacitance	C_{OUT}		1	$T_A = +25^oC$	-	10	-	10	pF
I/O Capacitance	$C_{I/O}$		1	$T_A = +25^oC$	-	10	-	10	pF
X, Y, RND Hold Time	T_H		1, 2	$-55^oC \leq T_A \leq +125^oC$	3	-	3	-	ns
3-State Disable Time	T_{DIS}		1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	25	-	30	ns
Output Rise Time	T_R	From 0.8V to 2.0V	1, 2, 4	$-55^oC \leq T_A \leq +125^oC$	-	10	-	10	ns
Output Fall Time	T_F	From 2.0V to 0.8V	1, 2, 4	$-55^oC \leq T_A \leq +125^oC$	-	10	-	10	ns

NOTES:
1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Guaranteed, but not 100% tested.
3. Transition is measured at ±200mV from steady state voltage, Output loading per test load circuit, with V_1 = 1.5V, R_1 = 500Ω and C_L = 40pF.
4. Loading is as specified in the test load circuit, with V_1 = 2.4V, R_1 = 500Ω and C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Burn-In Circuit

	A	B	C	D	E	F	G	H	J	K	L
11		N/C	X13	X15	RND	TCY	V_{CC}	GND	FT	$\overline{OEP}$	
10	X11	X12	X14	CLKX	TCX	V_{CC}	GND	$\overline{MSPSEL}$	$\overline{FA}$	CLKM	N/C
9	X9	X10								P30/ P14	P31/ P15
8	X7	X8								P28/ P12	P29/ P13
7	X5	X6								P26/ P10	P27/ P11
6	X3	X4				68 LEAD PIN GRID ARRAY TOP VIEW				P24/ P8	P25/ P9
5	X1	X2								P22/ P6	P23/ P7
4	$\overline{OEL}$	X0								P20/ P4	P21/ P5
3	CLKY	CLKL								P18/ P2	P19/ P3
2	N/C	Y0/ P0	Y2/ P2	Y4/ P4	Y6/ P6	Y8/ P8	Y10/ P10	Y12/ P12	Y14/ P14	P16/ P0	P17/ P1
1		Y1/ P1	Y3/ P3	Y5/ P5	Y7/ P7	Y9/ P9	Y11/ P11	Y13/ P13	Y15/ P15	N/C	

PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
B6	X4	F6	F1	Y9/P9	F11	K7	P10/P26	$V_{CC}/2$	E11	RND	F1
A6	X3	F5	G2	Y10/P10	F12	L7	P11/P27	$V_{CC}/2$	D10	CLKX	F0
B5	X2	F4	G1	Y11/P11	F13	K8	P12/P28	$V_{CC}/2$	D11	X15	F3
A5	X1	F3	H2	Y12/P12	F14	L8	P13/P29	$V_{CC}/2$	C10	X14	F2
B4	X0	F2	H1	Y13/P13	F15	K9	P14/P30	$V_{CC}/2$	C11	X13	F15
A4	OEL	V_{CC}	J2	Y14/P14	F4	L9	P15/P31	$V_{CC}/2$	B10	X12	F14
B3	CLKL	F0	J1	Y15/P15	F5	K10	CLKM	F0	A10	X11	F13
A3	CLKY	F0	K2	P0/P16	$V_{CC}/2$	K11	$\overline{OEP}$	F1	B9	X10	F12
B2	Y0/P0	F2	L2	P1/P17	$V_{CC}/2$	J10	$\overline{FA}$	F14	A9	X9	F11
B1	Y1/P1	F3	K3	P2/P18	$V_{CC}/2$	J11	FT	F15	B8	X8	F10
C2	Y2/P2	F4	L3	P3/P19	$V_{CC}/2$	H10	$\overline{MSPSEL}$	F14	A8	X7	F9
C1	Y3/P3	F5	K4	P4/P20	$V_{CC}/2$	H11	GND	GND	B7	X6	F8
D2	Y4/P4	F6	L4	P5/P21	$V_{CC}/2$	G10	GND	GND	A7	X5	F7
D1	Y5/P5	F7	K5	P6/P22	$V_{CC}/2$	G11	V_{CC}	V_{CC}	A2	N.C.	NONE
E2	Y6/P6	F8	L5	P7/P23	$V_{CC}/2$	F10	V_{CC}	V_{CC}	K1	N.C.	NONE
E1	Y7/P7	F9	K6	P8/P24	$V_{CC}/2$	F11	TCY	F15	L10	N.C.	NONE
F2	Y8/P8	F10	L6	P9/P25	$V_{CC}/2$	E10	TCX	F15	B11	N.C.	NONE

NOTES:

1. V_{CC} = 5.0V +0.5V/-0.0V with 0.1μF decoupling capacitor to GND.
2. F0 = 100kHz, F1 = F0/2, F2 = F1/2, ...
3. V_{IH} = V_{CC} - 1V ± 0.5V (Min), V_{IL} = 0.8V (Max)
4. 47kΩ load resistors used on all pins except V_{CC} and GND (Pin-Grid identifiers F10, G10, G11 and H11).

Die Characteristics

DIE DIMENSIONS:
179 x 169 x 19 ± 1mils

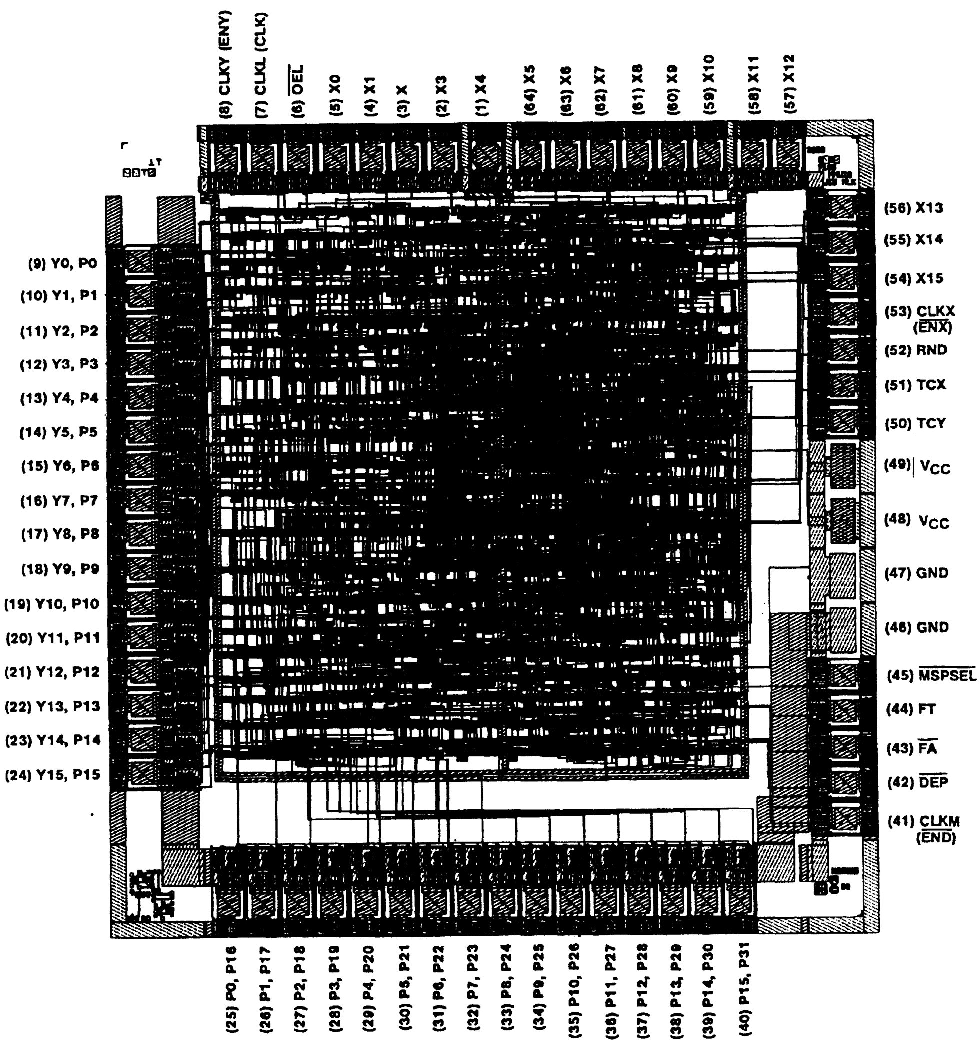
METALLIZATION:
Type: Si - Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY: $1.2 \times 10^5 A/cm^2$

Metallization Mask Layout

HMU16/883



HARRIS SEMICONDUCTOR

HMU17/883

January 1994

16 x 16-Bit CMOS Parallel Multiplier

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **16 x 16-Bit Parallel Multiplier with Full 32-Bit Product**
- **High-Speed (45ns) Clocked Multiply Time**
- **Low Power CMOS Operation:**
  - **I_{CCSB} = 500µA Maximum**
  - **I_{CCOP} = 7.0mA Maximum at 1MHz**
- **HMU17/883 is Compatible with the AM29517, LMU17, IDT7217, and the CY7C517**
- **Supports Two's Complement, Unsigned Magnitude and Mixed Mode Multiplication**
- **TTL Compatible Inputs/Outputs**
- **Three-State Outputs**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HMU17GM-45/883	-55°C to +125°C	68 Lead PGA
HMU17GM-60/883	-55°C to +125°C	68 Lead PGA

Description

The HMU17/883 is a high speed, low power CMOS 16 x 16-bit parallel multiplier ideal for fast, real time digital signal processing applications. The 16-bit X and Y operands may be independently specified as either two's complement or unsigned magnitude format, thereby allowing mixed mode multiplication operations.

Additional inputs are provided to accommodate format adjustment and rounding of the 32-bit product. The Format Adjust control allows the user the option of selecting a 31-bit product with the sign bit replicated LSP. The Round control is provided to accommodate rounding of the most significant portion of the result. This is accomplished by adding one to the most significant bit of the LSP.

Two 16-bit output registers (MSP and LSP) are provided to hold the most and least significant portions of the result, respectively. These registers may be made transparent for asynchronous operation through the use of the feedthrough control (FT). The two halves of the product may be routed to a single 16-bit three-state output port via the output multiplexer control, and in addition, the LSP is connected to the Y-input port through a separate three-state buffer.

The HMU17/883 utilizes a single clock signal (CLK) along with three register enables ($\overline{ENX}$, $\overline{ENY}$, and $\overline{ENP}$) to latch the input operands and the output product registers. The $\overline{ENX}$ and $\overline{ENY}$ inputs enable the X and Y input registers, while $\overline{ENP}$ enables both the LSP and MSP output registers. This configuration facilitates the use of the HMU17/883 for micro-programmed systems.

All outputs of the HMU17/883 also offer three-state control for multiplexing onto multiuse system busses.

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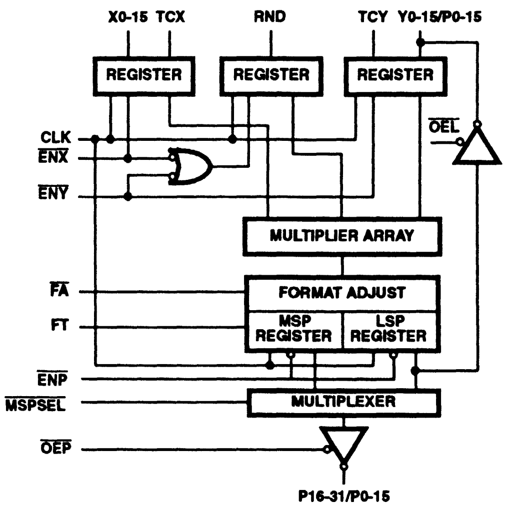
MULTIPLIERS

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2805.2**

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input or Output Voltage Applied .... GND-0.5V to V_{CC} +0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering 10 sec) .... 300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
Ceramic PGA Package .... 42.69°C/W 10.0°C/W
Maximum Package Power Dissipation at +125°C
Ceramic PGA Package .... 1.17 Watt
Gate Count .... 4500 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range .... -55°C to +125°C

TABLE 1. HMU16/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400μA V_{CC} = 4.5V (Note 1)	1, 2, 3	$-55^oC \le T_A \le +125^oC$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +4.0mA V_{CC} = 4.5V (Note 1)	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-10	+10	μA
Output or I/O Leakage Current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-10	+10	μA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	500	μA
Operating Power Supply Current	I_{CCOP}	f = 1.0MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.5V (Note 2)	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	7.0	mA
Functional Test	FT	(Note 3)	7, 8	$-55^oC \le T_A \le +125^oC$	-	-	

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 5mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH} (Clock Inputs) = 3.0, V_{IH} (All other inputs) = 2.6, V_{IL} = 0.4, $V_{OH} \ge$ 1.5V, and $V_{OL} \le$ 1.5V.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. HMU17/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	-45		-60		UNITS
					MIN	MAX	MIN	MAX	
Unclocked Multiply Time	T_{MUC}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	70	-	90	ns
Clocked Multiply Time	T_{MC}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	45	-	60	ns
X, Y, RND Setup Time	T_S		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	18	-	20	-	ns
Clock HIGH Pulse Width	T_{PWH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	20	-	ns
Clock LOW Pulse Width	T_{PWL}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	20	-	ns
MSPSEL to Product Out	T_{PDSEL}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	25	-	30	ns
Output Clock to P	T_{PDP}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	25	-	30	ns
Output Clock to Y	T_{PDY}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	25	-	30	ns
3-State Enable Time	T_{ENA}	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	25	-	30	ns
Clock Enable Setup	T_{SE}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	15	-	ns

NOTES:

1. AC Testing as follows: V_{CC} = 4.5V and 5.5V. Input levels 0V and 3.0V, Timing reference levels = 1.5V, Output load per test load circuit, with V_1 = 2.4V, R_1 = 500Ω and C_L = 40pF.
2. Transition is measured at ± 200mV from steady state voltage, Output loading per test load circuit, with V_1 = 1.5V, R_1 = 500Ω and C_L = 40pF.

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MULTIPLIERS

TABLE 3. HMU17/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	-45		-60		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz All Measurements are referenced to device GND.	1	$T_A = +25^oC$	-	15	-	15	pF
Output Capacitance	C_{OUT}		1	$T_A = +25^oC$	-	10	-	10	pF
I/O Capacitance	$C_{I/O}$		1	$T_A = +25^oC$	-	10	-	10	pF
X, Y, RND Hold Time	T_H		1, 2	$-55^oC \leq T_A \leq +125^oC$	3	-	3	-	ns
3-State Disable Time	T_{DIS}		1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	25	-	30	ns
Clock Enable Hold Time	T_{HE}		1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	3	-	3	-	ns
Output Rise Time	T_R	From 0.8V to 2.0V	1, 2, 4	$-55^oC \leq T_A \leq +125^oC$	-	10	-	10	ns
Output Fall Time	T_F	From 2.0V to 0.8V	1, 2, 4	$-55^oC \leq T_A \leq +125^oC$	-	10	-	10	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Guaranteed, but not 100% tested.
3. Transition is measured at ±200mV from steady state voltage, Output loading per test load circuit, with V_1 = 1.5V, R_1 = 500Ω and C_L = 40pF.
4. Loading is as specified in the test load circuit, with V_1 = 2.4V, R_1 = 500Ω and C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Burn-In Circuit

	A	B	C	D	E	F	G	H	J	K	L
11		N/C	X13	X15	RND	TCY	V_{CC}	GND	FT	$\overline{OEP}$	
10	X11	X12	X14	$\overline{ENX}$	TCX	V_{CC}	GND	$\overline{MSPSEL}$	$\overline{FA}$	$\overline{ENP}$	N/C
9	X9	X10								P30/ P14	P31/ P15
8	X7	X8								P28/ P12	P29/ P13
7	X5	X6								P26/ P10	P27/ P11
6	X3	X4				68 LEAD PIN GRID ARRAY TOP VIEW				P24/ P8	P25/ P9
5	X1	X2								P22/ P6	P23/ P7
4	$\overline{OEL}$	X0								P20/ P4	P21/ P5
3	$\overline{ENY}$	CLK								P18/ P2	P19/ P3
2	N/C	Y0/ P0	Y2/ P2	Y4/ P4	Y6/ P6	Y8/ P8	Y10/ P10	Y12/ P12	Y14/ P14	P16/ P0	P17/ P1
1		Y1/ P1	Y3/ P3	Y5/ P5	Y7/ P7	Y9/ P9	Y11/ P11	Y13/ P13	Y15/ P15	N/C	

PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
B6	X4	F6	F1	Y9/P9	F11	K7	P10/P26	$V_{CC}/2$	E11	RND	F1
A6	X3	F5	G2	Y10/P10	F12	L7	P11/P27	$V_{CC}/2$	D10	ENX	F0
B5	X2	F4	G1	Y11/P11	F13	K8	P12/P28	$V_{CC}/2$	D11	X15	F3
A5	X1	F3	H2	Y12/P12	F14	L8	P13/P29	$V_{CC}/2$	C10	X14	F2
B4	X0	F2	H1	Y13/P13	F15	K9	P14/P30	$V_{CC}/2$	C11	X13	F15
A4	$\overline{OEL}$	V_{CC}	J2	Y14/P14	F4	L9	P15/P31	$V_{CC}/2$	B10	X12	F14
B3	CLK	F0	J1	Y15/P15	F5	K10	$\overline{ENP}$	F0	A10	X11	F13
A3	$\overline{ENY}$	F0	K2	P0/P16	$V_{CC}/2$	K11	$\overline{OEP}$	F1	B9	X10	F12
B2	Y0/P0	F2	L2	P1/P17	$V_{CC}/2$	J10	$\overline{FA}$	F14	A9	X9	F11
B1	Y1/P1	F3	K3	P2/P18	$V_{CC}/2$	J11	FT	F15	B8	X8	F10
C2	Y2/P2	F4	L3	P3/P19	$V_{CC}/2$	H10	$\overline{MSPSEL}$	F14	A8	X7	F9
C1	Y3/P3	F5	K4	P4/P20	$V_{CC}/2$	H11	GND	GND	B7	X6	F8
D2	Y4/P4	F6	L4	P5/P21	$V_{CC}/2$	G10	GND	GND	A7	X5	F7
D1	Y5/P5	F7	K5	P6/P22	$V_{CC}/2$	G11	V_{CC}	V_{CC}	A2	N.C.	NONE
E2	Y6/P6	F8	L5	P7/P23	$V_{CC}/2$	F10	V_{CC}	V_{CC}	K1	N.C.	NONE
E1	Y7/P7	F9	K6	P8/P24	$V_{CC}/2$	F11	TCY	F15	L10	N.C.	NONE
F2	Y8/P8	F10	L6	P9/P25	$V_{CC}/2$	E10	TCX	F15	B11	N.C.	NONE

NOTES:

1. V_{CC} = 5.0V +0.5V/-0.0V with 0.1μF decoupling capacitor to GND.
2. F0 = 100kHz, F1 = F0/2, F2 = F1/2, ...
3. $V_{IH} = V_{CC}$ - 1V ± 0.5V (Min), V_{IL} = 0.8V (Max).
4. 47kΩ load resistors used on all pins except V_{CC} and GND (Pin-Grid identifiers F10, G10, G11 and H11).

Die Characteristics

DIE DIMENSIONS:
179 x 169 x 19 ± 1mils

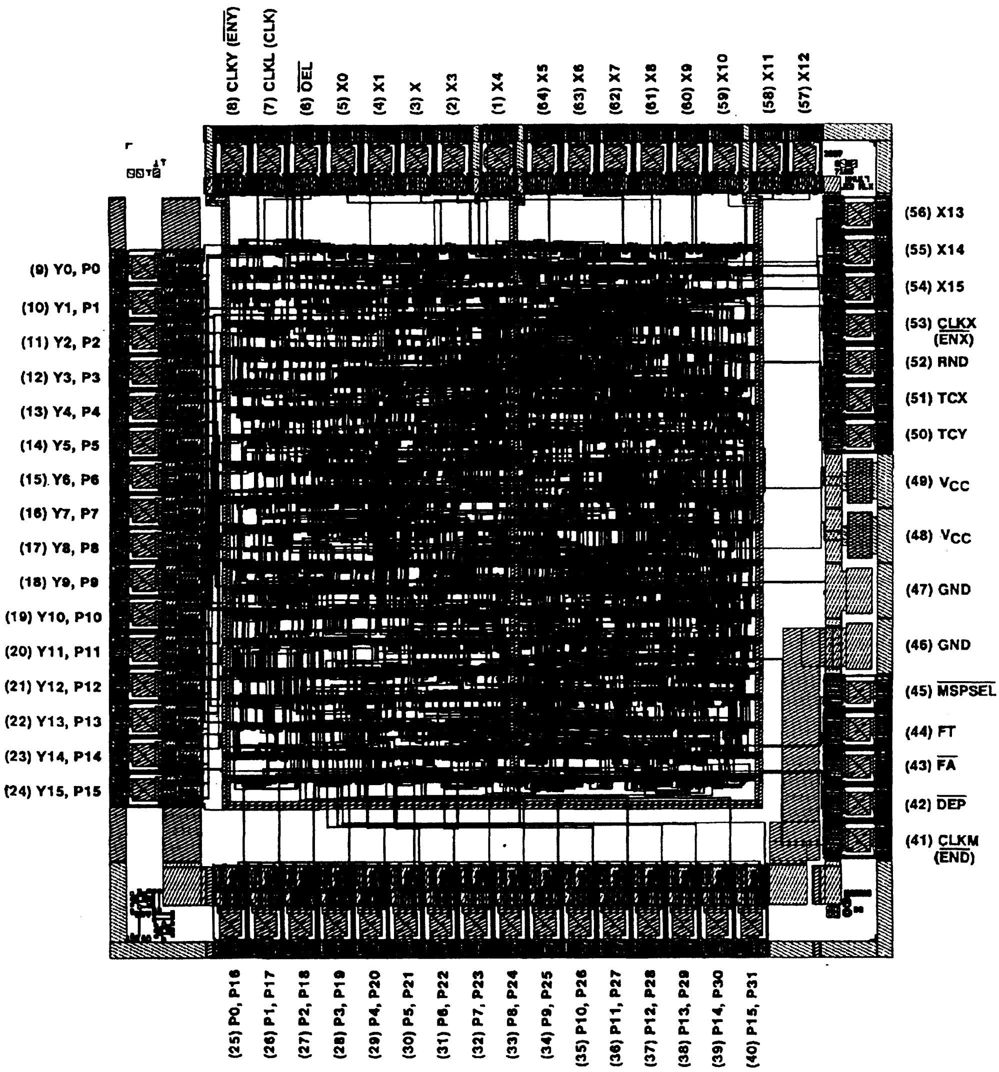
METALLIZATION:
Type: Si-Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY: $1.2 \times 10^5 A/cm^2$

Metallization Mask Layout

HMU17/883



DSP 3

ONE DIMENSIONAL FILTERS

PAGE

ONE DIMENSION FILTER DATA SHEETS

NOTE: Bold Type Designates a New Product from Harris.

HARRIS SEMICONDUCTOR

HSP43124

PRELIMINARY

January 1994

Serial I/O Filter

Features

- 45MHz Clock Rate
- 256 Tap Programmable FIR Filter
- 24-Bit Data, 32-Bit Coefficients
- Cascade of up to 5 Half Band Filters
- Decimation from 1 to 256
- Two Pin Interface for Down Conversion by $F_S/4$
- Multiplier for Mixing or Scaling Input with an External Source
- Serial I/O Compatible with Most DSP Microprocessors

Applications

- Low Cost FIR Filter
- Filter Co-Processor
- Digital Tuner

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
HSP43124PC-45	0°C to +70°C	28 Lead Plastic DIP
HSP43124SC-45	0°C to +70°C	28 Lead SOIC

Description

The Serial I/O Filter is a high performance filter engine that is ideal for off loading the burden of filter processing from a DSP microprocessor. It supports a variety of multistage filter configurations based on a user programmable filter and fixed coefficient halfband filters. These configurations include a programmable FIR filter of up to 256 taps, a cascade of from one to five halfband filters, or a cascade of halfband filters followed by a programmable FIR. The half band filters each decimate by a factor of two, and the FIR filter decimates from one to eight. When all six filters are selected, a maximum decimation of 256 is provided.

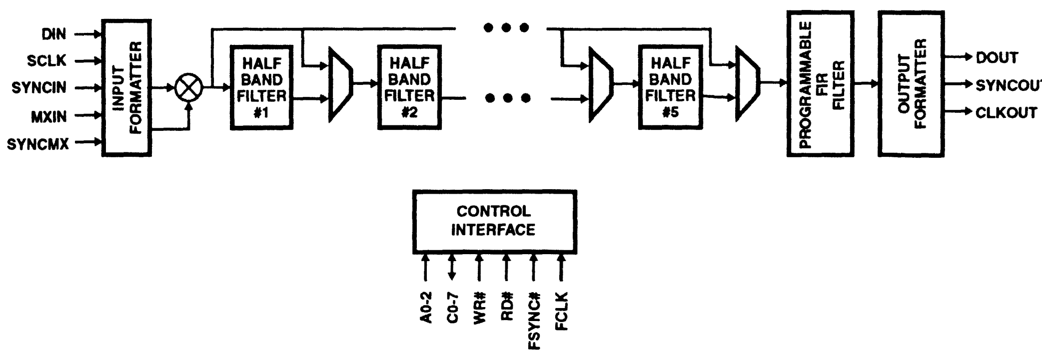
For digital tuning applications, a separate multiplier is provided which allows the incoming data stream to be multiplied, or mixed, by a user supplied mix factor. A two pin interface is provided for serially loading the mix factor from an external source or selecting the mix factor from an on-board ROM. The on-board ROM contains samples of a sinusoid capable of spectrally shifting the input data by one quarter of the sample rate, $F_S/4$. This allows the chip to function as a digital down converter when the filter stages are configured as a low-pass filter.

The serial interface for input and output data is compatible with the serial ports of common DSP microprocessors. Coefficients and configuration data are loaded over a bidirectional eight bit interface. This product is available in 28 pin DIP and SOIC packages.

3

1D FILTERS

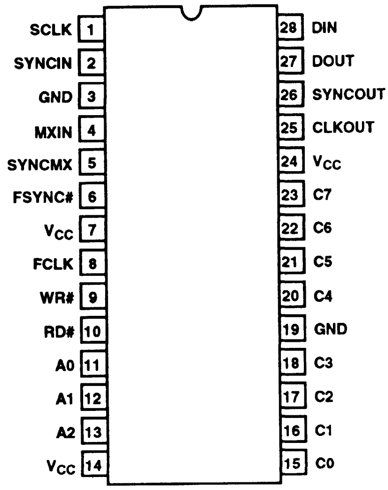
Block Diagram



File Number 3555.1

Pinout

28 LEAD PLASTIC DIP, SOIC
TOP VIEW



Pin Description

NAME	PDIP, SOIC PIN	TYPE	DESCRIPTION
V_{CC}	7, 14, 24	-	+5V Power Supply
GND	3, 19	-	Ground
DIN	28	I	Serial Data Input. The bit value present on this input is sampled on the rising edge of SCLK. A "HIGH" on this input represents a "1", and a low on this input represents "0". The word format and operation of serial interface are contained in the Data Input Section.
SYNCIN	2	I	Data Sync. The HSP43124 is synchronized to the beginning of a new data word on DIN when SCLK samples SYNCIN "HIGH" one SCLK before the first bit of the new word. Note: SYNCIN should not maintain a "HIGH" state for longer than one SCLK cycle.
SCLK	1	I	Serial Input CLK. The rising edge of SCLK clocks data on DIN and MXIN into the part. The following signals are synchronous to this clock: DIN, SYNCIN, MXIN, SYNCMX.
MXIN	4	I	Mix Factor Input. MXIN is the serial input for the mix factor. It is sampled on the rising edge of SCLK. A "HIGH" on this input represents a "1", and a low on this input represents "0". Also used to specify the Weaver Modulator ROM output. Details on word format and operation are contained in the Mix Factor Section.
SYNCMX	5	I	Mix Factor Sync. The HSP43124 is synchronized to the beginning of a serially input mix factor when SCLK samples SYNCMX "HIGH" one SCLK before the first bit of the new mix factor. Note: SYNCMX should only pulse "HIGH" for one SCLK cycle. Also used to specify Weaver Modulator ROM output.
FCLK	8	I	Filter Clock. The filter clock determines the processing speed of the Filter Compute Engine. Clock rate requirements on FCLK for particular filter configurations is discussed in the Filter Compute Engine Section. This clock may be asynchronous to the serial input clock (SCLK). FSYNC# is synchronous to this clock.
FSYNC#	6	I	Filter Sync. This input, when sampled low by the rising edge of FCLK, resets the filter compute engine so that the data sample following the next SYNCIN cycle is the first data sample into the filter structure. If a data stream is currently being input, the data is "canceled" and the DIN pin is ignored until the next SYNCIN cycle occurs.
WR#	9	I	Write. The falling edge of WR# loads data present on C0-7 into the configuration or coefficient register specified by the address on A0-2. The WR# signal is asynchronous to all other clocks. Note: WR# should not be low when RD# is low.
RD#	10	I	Read. The falling edge of RD# accesses the control registers or coefficient RAM addressed by A0-2 and places the contents of that memory location on C0-7. When RD# returns "HIGH" the C0-7 bus functions as an input bus.The RD# pin is asynchronous to all other clocks. Note: RD# should not be low when WR# is low.
A0-2	11, 12, 13	I	Address Bus. The A0-2 inputs are decoded on the falling edge of both RD# and WR#. Table 1 shows the address map for the control registers.
C0-7	15, 16, 17, 18, 20, 21, 22, 23	I/O	Control and Coefficient bus. This bi-directional bus is used to access the control registers and coefficient RAM.
CLKOUT	25	O	Output Clock. Programmable bit clock for serial output. Note: assertion of FILTSYNC# initializes OCLK to a high state.
SYNCOUT	26	O	Output Data Sync. SYNYOUT is asserted HIGH for one OCLK cycle before the first bit of a new output sample is available on DOUT.
DOUT	27	O	Serial Data Output. The bit stream is synchronous to the rising edge of OCLK. See the Serial Output Formatter section for additional details.

If the mix factor is generated by the Weaver Modulator ROM, the mix factor must be specified on MXIN and SYNCMX one SYNCIN before that which precedes the target data word (see Figure 9).

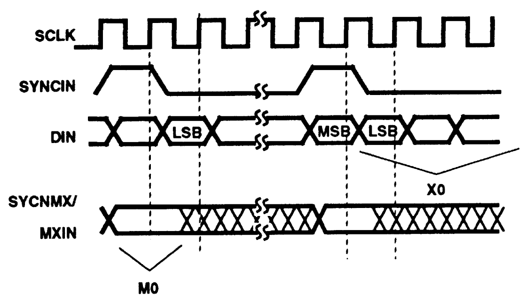


FIGURE 9. DATA/MIX FACTOR SYNCHRONIZATION WEAVER MODULATOR MIX FACTORS

NOTE: Figure 9 shows the specification of a ROM based mix factor, M0, so that it will be multiplied with the target data sample designated by X0.

Filter Compute Engine

The Filter Compute Engine centers around a multiply accumulator which is used to perform the sum-of-products required for a variety of filtering configurations. These configurations include a cascade of up to 5 halfband filters, a single symmetric filter of up to 256 taps, a single asymmetric filter of up to 128 taps, or a cascade of halfband filters followed by a programmable filter. The filter configuration is specified by programming the Filter Configuration Register (see Table 1).

The cascade of up to five halfband filters is an efficient decimating filter structure. Each fixed coefficient filter in the chain introduces a decimation of two, and the aggregate decimation rate of the entire halfband filtering stage is given by

$$DEC_{HB} = 2^{(\text{NUMBER OF HALFBAND FILTERS SELECTED})}.$$

Thus, a cascade of 3 halfband filters would decimate the input sample stream by a factor of 8.

The frequency responses of the five filters is presented graphically in Figure 10 and in tabular form in Table 3. The transition band for the fifth halfband filter, HB5, is the narrowest while that for the first halfband filter, HB1, is the widest. The cascade of the halfband filters always terminates with HB5 and is preceded by filters in order of increasing transition bandwidth. For example, if the HSP43124 is configured to operate with three halfbands, the chain of filters would consist of HB3 followed by HB4 and terminated with HB5. If only one halfband is selected, HB5 is used.

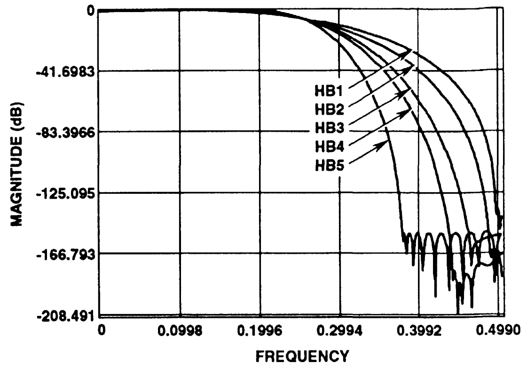


FIGURE 10. COMPOSITE RESPONSE OF FIXED COEFFICIENT HALFBAND FILTERS

The coefficients for each of the halfband filters is given in Table 4. These values are the 32-bit, two's complement, integer representation of the filter coefficients. Scaling these values by 2^{-31} yields the fractional two's complement coefficients used to achieve unity gain in the Filter Processor.

If a specific frequency response is desired, a programmable filter may be activated. The filter compute engine takes advantage of symmetry in FIR coefficients is by summing data samples sharing a common coefficient prior to multiplication. In this manner, two filter taps are calculated per multiply accumulate cycle. If an asymmetric filter is specified, only one tap per multiply accumulate cycle is calculated.

The processing rate of the Filter Compute Engine is proportional to FCLK. As a result, the frequency of FCLK must exceed a minimum value to insure that a filter calculation is complete before the result is required for output. In configurations which do not use decimation, one input sample period is available for filter calculation before an output is required. For configurations which employ decimation, up to 256 input sample periods may be available for filter calculation. The following equation specifies the minimum FCLK rate required for configurations which use the programmable filter as an FIR filter.

$$\text{Min FCLK} = (F_S/DEC_{HB})(TAPS/(2^*DEC_{FIR}) + HB_{CLKS} + 1)$$

In this equation F_S is the sample rate, TAPS is the number of taps in the FIR filter (0 to 256), DEC_{FIR} is the decimation rate of the programmable FIR (1 to 8), and HB_{CLKS} is a compute clock factor based on the number of halfband filters in the configuration (see Table 5). The term DEC_{HB} is the aggregate decimation rate for the cascade of halfband filters (see Table 5). For example, if the input sample rate is 800kHz, a 128 tap FIR filter with no decimation is selected, and a cascade of 2 halfband filters is used, a minimum FCLK rate of 19.6MHz would be required. Note: for configurations in which the halfband filters are used, the FCLK rate must exceed $14F_S$.

TABLE 3. FREQUENCY RESPONSE OF HALFBAND FILTERS

NORMALIZED FREQUENCY	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
0.000000	-0.000000	0.000000	0.000000	-0.000000	-0.000000
0.007812	0.000000	-0.000000	-0.000000	-0.000000	-0.000000
0.015625	-0.000113	-0.000000	-0.000000	-0.000000	-0.000000
0.023438	-0.000677	-0.000006	-0.000000	-0.000000	-0.000000
0.031250	-0.002243	-0.000052	-0.000000	-0.000000	-0.000000
0.039062	-0.005569	-0.000227	-0.000000	-0.000000	0.000000
0.046875	-0.011596	-0.000719	-0.000001	0.000000	-0.000000
0.054688	-0.021433	-0.001859	-0.000009	-0.000000	-0.000000
0.062500	-0.036333	-0.004165	-0.000041	-0.000000	-0.000000
0.070312	-0.057670	-0.008391	-0.000149	-0.000001	-0.000000
0.078125	-0.086916	-0.015557	-0.000448	-0.000012	-0.000000
0.085938	-0.125619	-0.026983	-0.001175	-0.000066	-0.000000
0.093750	-0.175382	-0.044301	-0.002767	-0.000258	-0.000000
0.101562	-0.237843	-0.069457	-0.005963	-0.000815	-0.000000
0.109375	-0.314663	-0.104701	-0.011924	-0.002208	-0.000000
0.117188	-0.407509	-0.152566	-0.022368	-0.005313	-0.000000
0.125000	-0.518045	-0.215834	-0.039695	-0.011613	-0.000000
0.132812	-0.647925	-0.297499	-0.067100	-0.023435	-0.000031
0.140625	-0.798791	-0.400727	-0.108640	-0.044186	-0.000287
0.148438	-0.972266	-0.528809	-0.169262	-0.078552	-0.001468
0.156250	-1.169959	-0.685131	-0.254777	-0.132639	-0.005427
0.164062	-1.393465	-0.873129	-0.371785	-0.214009	-0.016180
0.171875	-1.644372	-1.096269	-0.527552	-0.331613	-0.041152
0.179688	-1.924262	-1.358019	-0.729872	-0.495620	-0.092409
0.187500	-2.234728	-1.661842	-0.986908	-0.717181	-0.187497
0.195312	-2.577375	-2.011181	-1.307047	-1.008144	-0.349593
0.203125	-2.953834	-2.409468	-1.698769	-1.380771	-0.606862
0.210938	-3.365774	-2.860128	-2.170548	-1.847495	-0.991193
0.218750	-3.814917	-3.366593	-2.730783	-2.420719	-1.536664
0.226562	-4.303048	-3.932319	-3.387764	-3.112694	-2.278126
0.234375	-4.832037	-4.560817	-4.149669	-3.935463	-3.250174
0.242188	-5.403856	-5.255675	-5.024594	-4.900864	-4.486639
0.250000	-6.020599	-6.020600	-6.020600	-6.020600	-6.020600
0.257812	-6.684504	-6.859450	-7.145791	-7.306352	-7.884833
0.265625	-7.397981	-7.776287	-8.408404	-8.769932	-10.112627
0.273438	-8.163642	-8.775419	-9.816921	-10.423476	-12.738912
0.281250	-8.984339	-9.861469	-11.380193	-12.279667	-15.801714
0.289062	-9.863195	-11.039433	-13.107586	-14.352002	-19.344007

TABLE 3. FREQUENCY RESPONSE OF HALFBAND FILTERS (Continued)

NORMALIZED FREQUENCY	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
0.296875	-10.803663	-12.314765	-15.009147	-16.655094	-23.416153
0.304688	-11.809574	-13.693460	-17.095793	-19.205034	-28.079247
0.312500	-12.885208	-15.182171	-19.379534	-22.019831	-33.409992
0.320312	-14.035372	-16.788332	-21.873730	-25.119940	-39.508194
0.328125	-15.265501	-18.520315	-24.593418	-28.528942	-46.509052
0.335938	-16.581776	-20.387625	-27.555685	-32.274414	-54.604954
0.343750	-17.991278	-22.401131	-30.780161	-36.389088	-64.087959
0.351562	-19.502172	-24.573368	-34.289623	-40.912403	-75.444221
0.359375	-21.123947	-26.918915	-38.110786	-45.892738	-89.610390
0.367188	-22.867725	-29.454887	-42.275345	-51.390583	-108.973686
0.375000	-24.746664	-32.201569	-46.821358	-57.483341	-152.503693
0.382812	-26.776485	-35.183285	-51.795181	-64.272881	-153.443375
0.390625	-28.976198	-38.429543	-57.254162	-71.898048	-158.914017
0.398438	-31.369083	-41.976673	-63.270584	-80.556969	-156.960175
0.406250	-33.984089	-45.870125	-69.937607	-90.550629	-153.317627
0.414062	-36.857830	-50.167850	-77.378593	-102.379677	-161.115540
0.421875	-40.037594	-54.945438	-85.762718	-117.007339	-153.504684
0.429688	-43.585945	-60.304272	-95.332924	-136.890198	-158.650345
0.437500	-47.588165	-66.385063	-106.462181	-185.130432	-154.637756
0.445312	-52.164894	-73.392075	-119.793030	-187.297241	-153.870453
0.453125	-57.495132	-81.640152	-136.802948	-182.300125	-161.882385
0.460938	-63.861992	-91.658478	-175.030167	-203.460876	-152.278915
0.468750	-71.755898	-104.468010	-158.939362	-174.691895	-164.329758
0.476562	-82.156616	-122.641861	-157.095886	-174.737076	-153.535690
0.484375	-97.627930	-166.537369	-155.613434	-175.108841	-153.507477
0.492188	-139.751450	-165.699081	-154.708450	-169.966568	-167.665482

TABLE 4. HALFBAND FILTER COEFFICIENTS (32-BITS, UN-NORMALIZED)

COEFFICIENT	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
C0	-67230275	12724188	624169	-197705	23964
C1	0	0	0	0	0
C2	604101076	-105279784	-6983862	2303514	-242570
C3	1073741823	0	0	0	0
C4	604101076	629426509	38140187	-13225905	1306852
C5	0	1073741827	0	0	0
C6	-67230275	629426509	-145867861	51077176	-4942818
C7		0	0	0	0
C8		-105279784	650958284	-161054660	14717750

TABLE 4. HALFBAND FILTER COEFFICIENTS (32-BITS, UN-NORMALIZED) (Continued)

COEFFICIENT	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
C9		0	1073741793	0	0
C10		12724188	650958284	657968488	-37027884
C11			0	1073741825	0
C12			-145867861	657968488	84032070
C13			0	0	0
C14			38140187	-161054660	-191585682
C15			0	0	0
C16			-6983862	51077176	670589251
C17			0	0	1073741824
C18			624169	-13225905	670589251
C19				0	0
C20				2303514	-191585682
C21				0	0
C22				-197705	84032070
C23					0
C24					-37027884
C25					0
C26					14717750
C27					0
C28					-4942818
C29					0
C30					1306852
C31					0
C32					-242570
C33					0
C34					23964

TABLE 5. PERFORMANCE ENVELOPE PARAMETERS

NUMBER OF HALFBANDS	HB_{CLKS}	DEC_{HB}
0	0	1
1	13	2
2	33	4
3	69	8
4	125	16
5	221	32

The longest length FIR filter realizable for a particular configuration is determined by solving the above equation for TAPS. The resulting expression is given below.

Max TAPS = $2DEC_{FIR}((FCLK/F_S)DEC_{HB} - HB_{CLKS} - 1)$

The maximum throughput sample rate may be specified by solving the above equation for F_S. The resulting equation is

Max $F_S = FCLK*DEC_{HB}/(TAPS/(2*DEC_{FIR}) + HB_{CLKS} + 1)$.

NOTE: for configurations using filters with asymmetric coefficients, the term TAPS in the above equations should be multiplied by two in order to determine the correct FCLK.

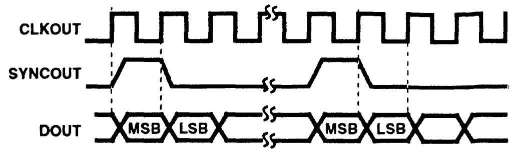
The Filter Compute Engine is synchronized with an incoming data stream by asserting the FYSNC# input. When this input is sample low by the rising edge of FCLK, the Compute Engine is reset, and the data word following the next assertion of SYNCIN is recognized as the first data sample input to the filter structure.

Serial Output Formatter

The Output Formatter serializes the parallel output of the filter compute engine while generating the timing and synchronization signals required to support a serial interface. The Formatter produces serial data words with programmable lengths from 8 to 32-bits. The data words may be organized with either most or least significant bit first. Also, the data word may be rounded or truncated to the desired length and the format of the output data may be specified as either two's complement or offset binary. To simplify applications where the Serial I/O Filter is used as a down converter, the output formatter can be configured to scale the output by a factor of 2. The above options are programmed via the Output Format and Output Timing Registers given in Table 1.

The HSP43124 outputs a bit stream through DOUT which is synchronous to a programmable clock signal output on CLKOUT. The output clock, CLKOUT, is derived from FCLK and has a programmable rate from 1 to $^1/_{32}$ times FCLK. The duty cycle of CLKOUT is 50% for rates that have an even number of FCLK's per CLKOUT. For rates that have and odd number of FCLK's per OCLK the high portion of the CLKOUT waveform spans (n+1)/2 FCLK's and the low portion spans (n-1)/2 FCLK's where n is the number of FCLK's.

External devices synchronize to the beginning of an output data word by monitoring SYNCOUT. This output is asserted "high" one CLKOUT prior to the first bit of the next data word as shown in Figure 11.



NOTE: Assumes data is being output LSB first.

FIGURE 11. SERIAL OUTPUT TIMING

Input and Output Data Formats

The data formats for the input, output and coefficients are fractional two's complement. The bit weighting's in the data words are given in Figure 12. Input or output data words programmed to have less than 24-bits, map to the most significant bit positions of the 24-bit word. For example, an input word defined to be 8-bits wide would map to the bit positions with weightings from -2^0 to 2^{-7}.

FRACTIONAL TWO'S COMPLEMENT FORMAT FOR 24-BIT INPUT AND OUTPUT

24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
-2^0.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

FRACTIONAL TWO'S COMPLEMENT FORMAT FOR 32-BIT COEFFICIENTS

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
-2^0.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}

FIGURE 12. DATA FORMATS

Absolute Maximum Ratings

Supply Voltage .... +7.0V
Input, Output Voltage .... GND -0.5V to V_{CC} +0.5V
Storage Temperature .... -65°C to +150°C
ESD .... Class 1
Junction Temperature.................... +150°C (SOIC,PDIP)
Lead Temperature (Soldering 10s).................... +300°C

Thermal Resistance	θ_{JA}	θ_{JC}
SOIC Package	65°C/W	TBD°C/W
Plastic DIP Package	45°C/W	TBD°C/W

Maximum Package Power Dissipation
SOIC Package 1.23W
Plastic DIP Package 1.78W
Gate Count 40,304

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range (Commercial)........... 4.75V to 5.25V
Operating Temperature Range (Commercial)....... 0°C to +70°C

DC Electrical Specifications (V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Power Supply Current	I_{CCOP}	-	203	mA	V_{CC} = Max, FCLK = SCLK = 45Mhz Notes 1, 2
Standby Power Supply Current	I_{CCSB}	-	500	uA	V_{CC} = Max, Outputs Not Loaded
Input Leakage Current	I_I	-10	10	uA	V_{CC} = Max, Input = 0V or V_{CC}
Output Leakage Current	I_O	-10	10	V	V_{CC} = Max, Input = 0V or V_{CC}
Clock Input High	V_{IHC}	3.0	-	V	V_{CC} = Max, FCLK and SCLK
Clock Input Low	V_{ILC}	-	0.8	V	V_{CC} = Min, FCLK and SCLK
Logical One Input Voltage	V_{IH}	2.0	-	V	V_{CC} = Max
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = Min
Logical One Output Voltage	V_{OH}	2.6	-	V	I_{OH} = -5mA, V_{CC} = Min
Logical Zero Output Voltage	V_{OL}	-	0.4	V	I_{OL} = 5mA, V_{CC} = Min
Input Capacitance	C_{IN}	-	10	pF	FCLK = SCLK = 1MHz All Measurements Referenced to GND. T_A = +25°C, Note 3
Output Capacitance	C_{OUT}	-	10	pF	

NOTES:

1. Power supply current is proportional to frequency. Typical rating is 4.5mA/MHz.
2. Output load per test circuit and C_L = 40pF.
3. Not tested, but characterized at initial design and at major process/design changes.

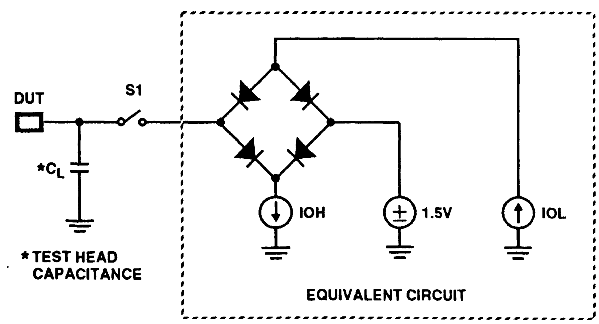
AC Electrical Specifications (Note 1) (V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C)

PARAMETER	SYMBOL	45MHz MIN	45MHz MAX	COMMENTS
FCLK, SCLK Period	T_{CP}	22	-	ns
FCLK, SCLK High	T_{CH}	8	-	ns
FCLK, SCLK Low	T_{CL}	8	-	ns
Setup Time DIN, MXIN, SYNCIN, SYNCMX to SCLK	T_{DS}	8	-	ns
Hold Time DIN, MXIN, SYNCIN, SYNCMX from SCLK	T_{DH}	0	-	ns
Setup Time FSYNC to FCLK	TSS	8	-	ns
Hold Time FSYNC from FCLK	TSH	0	-	ns
Setup Time C0-7, A0-2 to Falling Edge of WR#	T_{WS}	10	-	ns
Hold Time C0-7, A0-2 from Falling Edge of WR#	T_{WH}	3	-	ns
Setup Time A0-2 to Falling Edge of RD#	T_{RS}	10	-	ns
Hold Time A0-2 from Rising Edge of RD#	T_{RH}	0	-	ns
WR# High	T_{WRH}	10	-	ns
WR# Low	T_{WRL}	10	-	ns
RD# High	T_{RDH}	10	-	ns
RD# Low to Data Valid	T_{RDO}	-	25	ns
RD# High to Output Disable	T_{OD}	-	6	ns
FCLK to CLKOUT	T_{FOC}	-	12	ns
CLKOUT to SYNCOUT, DOUT	T_{DO}	-	8	ns
Output Rise, Fall Time	T_{RF}	-	3	ns, Note 2

NOTES:

1. AC tests performed with C_L = 40pF, I_{OL} = 5mA, and I_{OH} = -5mA. Input reference level for FCLK and SCLK is 2.0V, all other inputs 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V.
2. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.

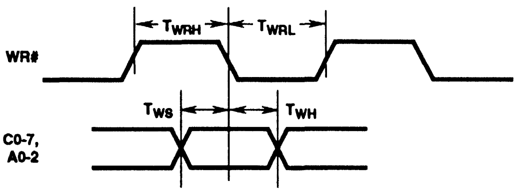
AC Test Load Circuit



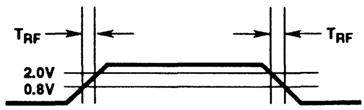
SWITCH S1 OPEN FOR I_{CCSB} AND I_{CCOP}

Waveforms

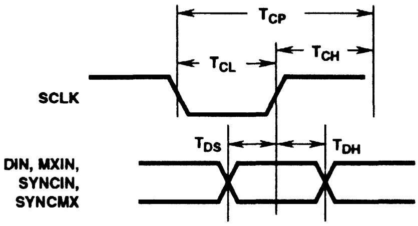
TIMING RELATIVE TO WR#



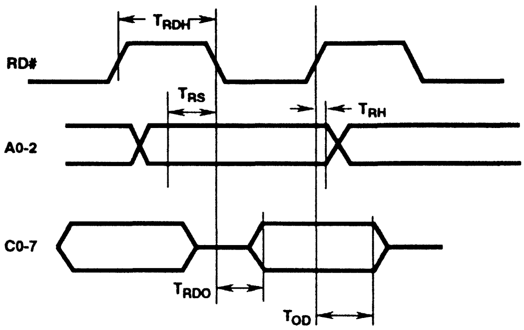
OUTPUT RISE AND FALL TIMES



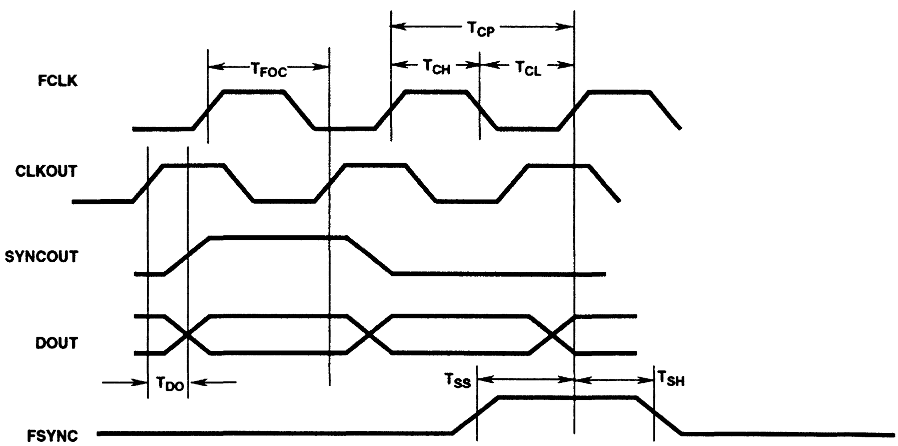
INPUT DATA TIMING



TIMING RELATIVE TO READ



TIMING RELATIVE TO FLCK AND CLKOUT



3

1D FILTERS

HARRIS SEMICONDUCTOR

HSP43168

January 1994

Dual FIR Filter

Features

- Two Independent 8-Tap FIR Filters Configurable as a Single 16-Tap FIR
- 10-Bit Data & Coefficients
- On-Board Storage for 32 Programmable Coefficient Sets
- Up To: 256 FIR Taps, 16 x 16 2-D Kernels, or 10 x 19-Bit Data and Coefficients
- Programmable Decimation to 16
- Programmable Rounding on Output
- Standard Microprocessor Interface

Applications

- Quadrature, Complex Filtering
- Image Processing
- PolyPhase Filtering
- Adaptive Filtering

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43168VC-33	0°C to +70°C	100 Lead MQFP
HSP43168VC-45	0°C to +70°C	100 Lead MQFP
HSP43168JC-33	0°C to +70°C	84 Lead PLCC
HSP43168JC-45	0°C to +70°C	84 Lead PLCC
HSP43168GC-33	0°C to +70°C	84 Lead PGA
HSP43168GC-45	0°C to +70°C	84 Lead PGA

Description

The HSP43168 Dual FIR Filter consists of two independent 8-tap FIR filters. Each filter supports decimation from 1 to 16 and provides on-board storage for 32 sets of coefficients. The Block Diagram shows two FIR cells each fed by a separate coefficient bank and one of two separate inputs. The outputs of the FIR cells are either summed or multiplexed by the MUX/Adder. The compute power in the FIR Cells can be configured to provide quadrature filtering, complex filtering, 2-D convolution, 1-D/2-D correlations, and interpolating/decimating filters.

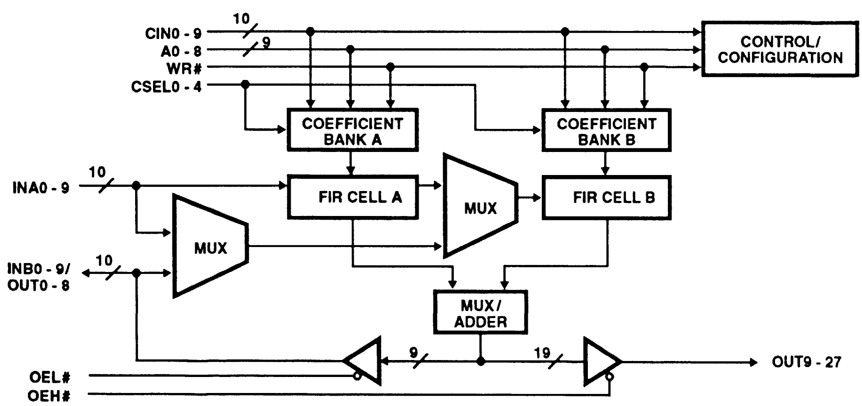
The FIR cells take advantage of symmetry in FIR coefficients by pre-adding data samples prior to multiplication. This allows an 8-tap FIR to be implemented using only 4 multipliers per filter cell. These cells can be configured as either a single 16-tap FIR filter or dual 8-tap FIR filters. Asymmetric filtering is also supported.

Decimation of up to 16 is provided to boost the effective number of filter taps from 2 to 16 times. Further, the decimation registers provide the delay necessary for fractional data conversion and 2-D filtering with kernels to 16x16.

The flexibility of the Dual is further enhanced by 32 sets of user programmable coefficients. Coefficient selection may be changed asynchronously from clock to clock. The ability to toggle between coefficient sets further simplifies applications such as polyphase or adaptive filtering.

The HSP43168 is a low power fully static design implemented in an advanced CMOS process. The configuration of the device is controlled through a standard microprocessor interface.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2808.3

Pinouts

84 PIN PGA BOTTOM VIEW

	11	10	9	8	7	6	5	4	3	2	1
A	RVRS #	WR #	GND	A1	A4	A7	A8	CSEL1	CSEL3	CSEL4	CIN8
B	SHFTEN #	MUX0	MUX1	A0	A3	A2	V_{CC}	CSEL2	CIN9	CIN7	CIN5
C	TXFR #	FWRD #			A5	A6	CSEL0			CIN6	CIN4
D	V_{CC}	ACCEN								GND	CIN3
E	OEH #	GND	CLK						CIN2	CIN1	CIN0
F	OUT27	OUT22	OUT26						INA8	INA9	V_{CC}
G	OUT24	OUT23	OUT25						INA7	INA5	INA6
H	OUT21	OUT20								INA3	INA4
J	OUT19	OUT17			OUT9	OEL #	INB3			INA0	INA2
K	OUT18	V_{CC}	OUT16	OUT13	V_{CC}	INB0	INB2	GND	INB7	INB8	INA1
L	GND	OUT15	OUT14	OUT12	OUT10	OUT11	INB1	INB4	INB5	INB6	INB9

PIN 'A1' ID

HSP43168 BOTTOM VIEW

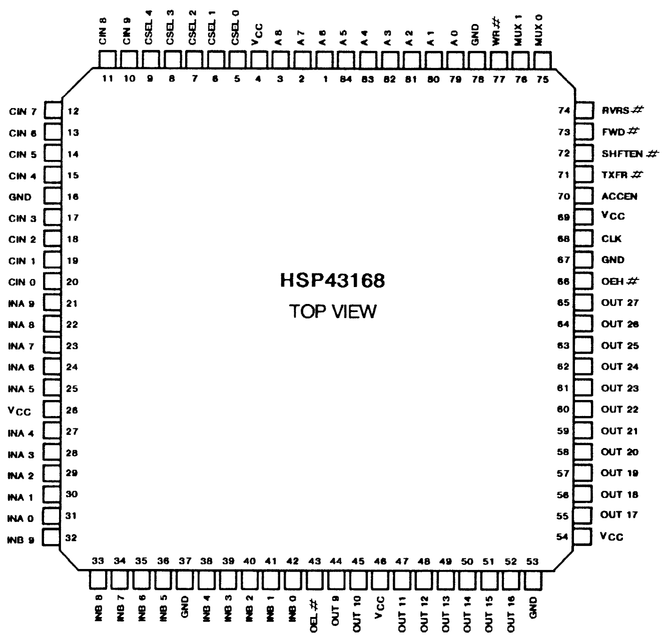
84 PIN PGA TOP VIEW

	11	10	9	8	7	6	5	4	3	2	1
L	GND	OUT15	OUT14	OUT12	OUT10	OUT11	INB1	INB4	INB5	INB6	INB9
K	OUT18	V_{CC}	OUT16	OUT13	V_{CC}	INB0	INB2	GND	INB7	INB8	INA1
J	OUT19	OUT17			OUT9	OEL #	INB3			INA0	INA2
H	OUT21	OUT20								INA3	INA4
G	OUT24	OUT23	OUT25						INA7	INA5	INA6
F	OUT27	OUT22	OUT26						INA8	INA9	V_{CC}
E	OEH #	GND	CLK						CIN2	CIN1	CIN0
D	V_{CC}	ACCEN								GND	CIN3
C	TXFR #	FWRD #			A5	A6	CSEL0			CIN6	CIN4
B	SHFTEN #	MUX0	MUX1	A0	A3	A2	V_{CC}	CSEL2	CIN9	CIN7	CIN5
A	RVRS #	WR #	GND	A1	A4	A7	A8	CSEL1	CSEL3	CSEL4	CIN8

PIN 'A1' ID

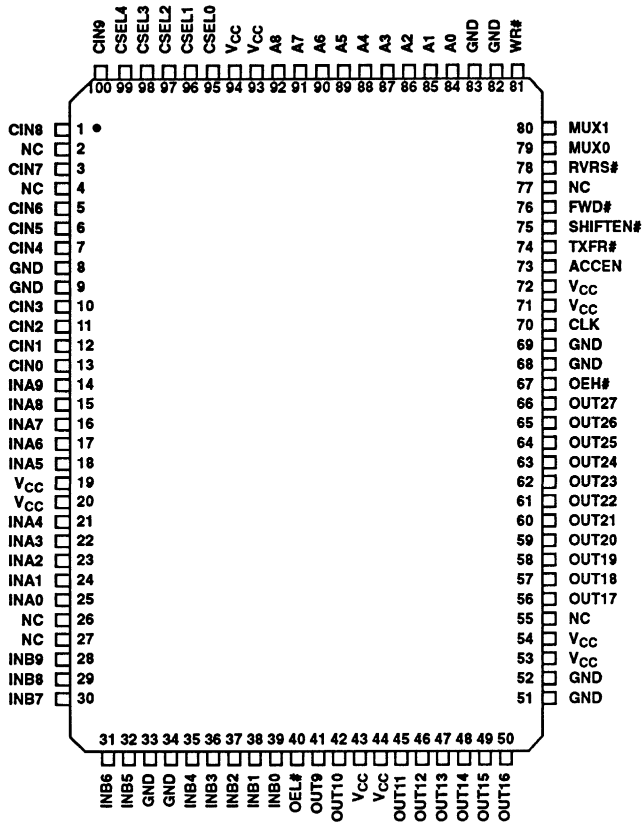
HSP43168 TOP VIEW

84 PIN PLCC TOP VIEW



Pinouts (Continued)

100 LEAD MQFP
TOP VIEW



Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
VCC	B5, D11, K10 K7, F1		VCC: +5V power supply pin.
GND	A9, E10, L11 K4, D2		Ground.
CIN0-9	E1-3, D1, C1-2, B1-3, A1	I	Control/Coefficient Data Bus. Processor interface for loading control data and coefficients. CIN0 is the LSB.
A0-8	A5-8, B6-8, C6-7	I	Control/Coefficient Address Bus. Processor interface for addressing control and coefficient registers. A0 is the LSB.
WR#	A10	I	Control/Coefficient Write Clock. Data is latched into the control and coefficient registers on the rising edge of WR#.
CSEL0-4	A2-4, B4, C5	I	Coefficient Select. This input determines which of the 32 coefficient sets are to be used by FIR A and B. This input is registered and CSEL0 is the LSB.
INA0-9	K1, J1-2, H1-2, G1-3, F2-3	I	Input to FIR A. INA0 is the LSB
INB0-9	L1-5, K2-3 K5-6, J5	I/O	Bidirectional Input for FIR B. INB0 is the LSB and is input only. When used as output, INB1-9 are the LSB's of the output bus, and INB9 is the MSB of these bits.
OUT9-27	F9-11, G9-11, H10-11, J10-11 J7, K11, K8-9, L6-10	O	19 MSB's of Output Bus. Data format is either unsigned or two's complement depending on configuration. OUT27 is the MSB.
SHFTEN#	B11	I	Shift Enable. This active low input enables clocking of data into the part and shifting of data through the decimation registers.
FWRD#	C10	I	Forward ALU Input Enable. When active low, data from the forward decimation path is input to the ALU's through the "a" input. When high, the "a" inputs to the ALUs are zeroed.
RVRS#	A11	I	Reverse ALU Input Enable. When active low, data from the reverse decimation path is input to the ALU's through the "b" input. When high, the "b" inputs to the ALUs are zeroed.
TXFR#	C11	I	Data Transfer Control. This active low input switches the LIFO being read into the reverse decimation path with the LIFO being written from the forward decimation path (see Figure 1).
MUX0-1	B9-10	I	Adder/Mux Control. This input controls data flow through the output Adder/Mux. Table 3.0 lists the various configurations.
CLK	E9	I	Clock. All inputs except those associated with the processor interface (CIN0-9, A0-8, WR#) and the output enables (OEL#, OEH#)are registered by the rising edge of CLK.
OEL#	J6	I	Output Enable Low. This tristate control enables the LSB's of the output bus to INB1-9 when OEL# is low.
OEH#	E11	I	Output Enable High. This tristate control enables OUT9-27 when OEH# is low.
ACCEN	D10	I	Accumulate Enable. This active high input allows accumulation in the FIR Cell Accumulator. A low on this input latches the FIR Accumulator contents into the Output Holding Registers while zeroing the feedback path in the Accumulator.

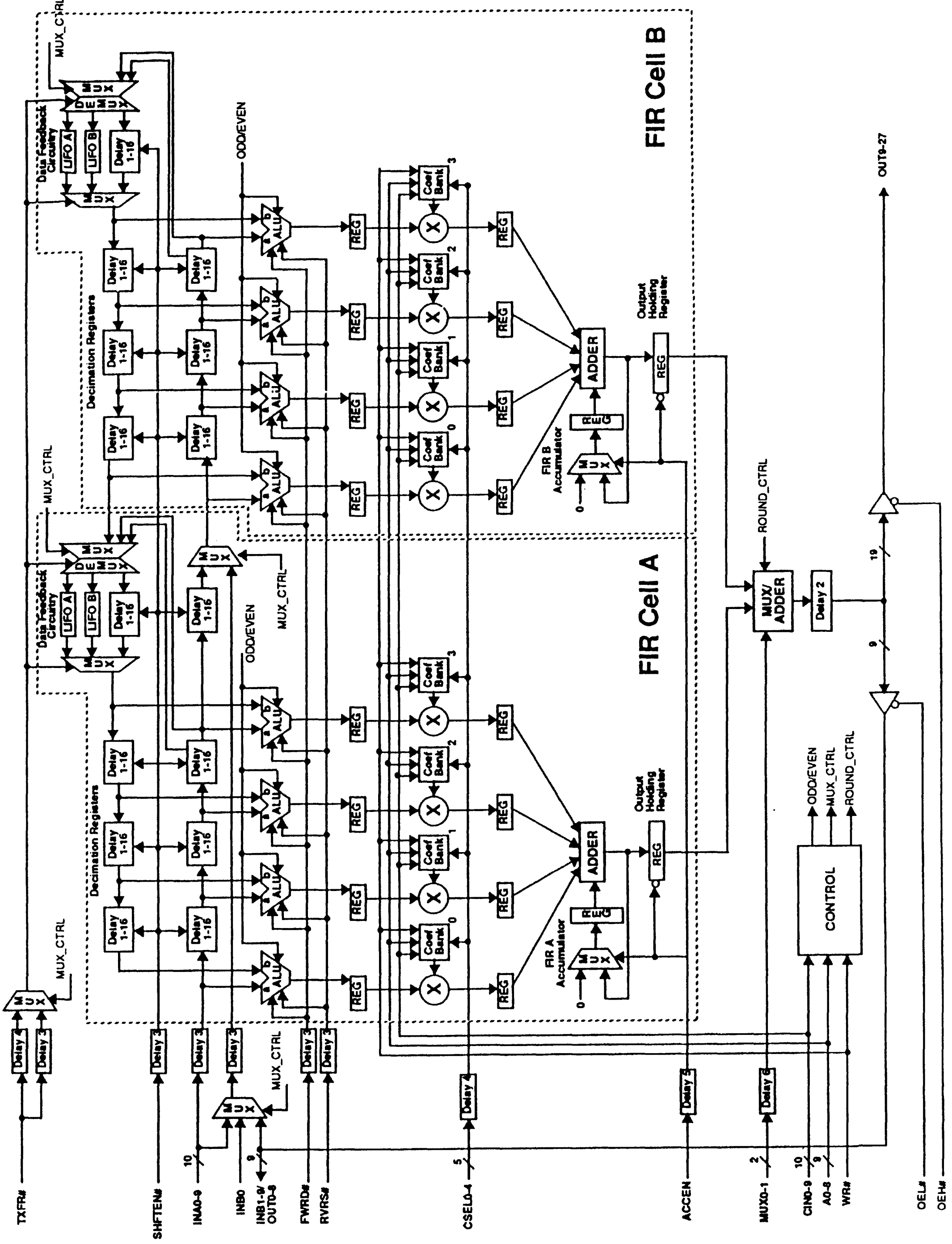


FIGURE 1. DUAL FIR FILTER

Functional Description

As shown in Figure 1.0, the HSP43168 consists of two 4-multiplier FIR filter cells which process 10 bit data and coefficients. The FIR cells can operate as two independent 8-tap FIR filters or two 4-tap asymmetric filters at maximum I/O rates. A single filter mode is provided which allows the FIR cells to operate as one 16-tap FIR filter or one 8-tap asymmetric filter. On board coefficient storage for up to 32 sets of 8 coefficients is provided. The coefficient sets are user selectable and are programmed through a microprocessor interface. Programmable decimation to 16 is also provided. By utilizing decimation registers together with the coefficient sets, polyphase filters are realizable which allow the user to trade data rate for filter taps. The MUX/ Adder can be configured to either add or multiplex the outputs of the filter cells depending upon whether the cells are operating in single or dual filter mode. In addition, a shifter in the MUX/Adder is provided for implementation of filters with 10 bit data and 20 bit coefficients or vice versa.

Microprocessor Interface

The Dual has a 20 pin write only microprocessor interface for loading data into the Control Block and Coefficient Bank. The interface consists of a 10-bit data bus (CIN0-9), a 9 bit address bus (A0-8), and a write input (WR#) to latch the data into the on-board registers. The control and coefficient data can be loaded asynchronously to CLK.

Control Block

The Dual FIR is configured by writing to the registers within the Control Block. These registers are memory mapped to address 000H (H = Hexadecimal) and 001H on A0-8. The format of these registers is shown in Table 1 and Table 2. Writing the Control/Configuration registers causes a reset which lasts for 6 CLK cycles following the assertion of WR#. The reset caused by writing registers in the Control Block will not clear the contents of the Coefficient Bank.

TABLE 1

CONTROL ADDRESS 000H		
BITS	**FUNCTION**	**DESCRIPTION**
3-0	Decimation Factor	0000=No Decimation 1111=Decimation by 16
4	Mode Select	0 = Single Filter Mode 1 = Dual Filter Mode
5	Odd/Even Symmetry	0 = Even symmetric coefficients 1 = Odd symmetric coefficients
6	FIR A odd/even taps	0 = Odd number of taps in filter 1 = Even number of taps in filter
7	FIR B odd/even taps	(Defined same as FIR A above)
8	FIR B Input Source	0 = Input from INA0-9 1 = Input from INB0-9
9	Not Used	Set to 0 for proper operation

The 4 LSBs of the control word loaded at address 000H are used to select the decimation factor. For example, if the 4 LSBs are programmed with a value of 0010, the forward and reverse shifting decimation registers are each configured with a delay of 3. Bit 4 is used to select whether the FIR cells operate as two independent filters or one extended length filter. Coefficient symmetry is selected by bit 5. Bits 6 and 7 are programmed to configure the FIR cells for odd or even filter lengths. Bit 8 selects the FIR B input source when the FIR cells are configured for independent operation. Bit 9 must be programmed to 0.

The 4 LSB's of the control word loaded at address 001H are used to configure the format of the FIR cell's data and coefficients. Bit 4 is programmed to enable or disable the reversal of data sample order prior to entering the backward shifting decimation registers. Bits 5-9 are used to support programmable rounding on the output.

TABLE 2

CONTROL ADDRESS 001H		
BITS	**FUNCTION**	**DESCRIPTION**
0	FIR A Input Format	0 = Unsigned 1 = Two's Complement
1	FIR A Coefficient Format	(Defined same as FIR A input)
2	FIR B Input Format	(Defined same as FIR A input)
3	FIR B Coefficient	(Defined same as FIR A input)
4	Data Reversal Enable	0 = Enabled 1 = Disabled
8-5	Round Position	0000 = 2^{-10} 1011 = 2^{1}
9	Round Enable	0 = Enabled 1 = Disabled

NOTE: Address locations 002H to 0ffH are reserved, and writing to these locations will have unpredictable effects on part configuration.

FIR Filter Cells

Each FIR filter cell is based on an array of four 11x10 bit two's complement multipliers. The multipliers get one input from the ALUs which combine data shifting through the forward and backward decimation registers. The second input comes from the user programmable coefficient bank. The multiplier outputs feed an accumulator whose result is passed to the output section where it is multiplexed or added.

Decimation Registers

The forward and backward shifting registers are configurable for decimation by 1 to 16 (see Table 1). The backward shifting registers are used to take advantage of symmetry in linear phase filters by aligning data at the ALU's for pre-addition prior to multiplication by the common coefficient. When the FIR cells are configured in single filter mode, the decimation registers in each cell are cascaded. This lengthened delay path allows computation of a filter which is twice the size of that capable in a single cell. The decimation registers also provide data storage for poly-phase or 2-D filtering applications (See Applications Examples section).

3

1D FILTERS

The Data Feedback Circuitry in each FIR cell is responsible for transferring data from the forward to the backward shifting decimation registers. This circuitry feeds blocks of samples into the backward shifting decimation path in either reversed or non-reversed sample order. The MUX/DEMUX structure at the input to the Feedback Circuitry routes data to the LIFO's or the delay stage depending on configuration. The MUX on the Feedback Circuitry Output selects the storage element which feeds the backward shifting decimation registers.

In applications requiring reversal of sample order, such as FIR filtering with decimation, the FIR cells are configured with data reversal enabled (see Table 2). In this mode, data is transferred from the forward to the backward shifting registers through a ping-ponged LIFO structure. While one LIFO is being read into the backward shifting path, the other is written with data samples. The MUX/DEMUX controls which LIFO is being written, and the MUX on the Feedback Circuitry output controls which LIFO is being read. A low on TXFR# and SHIFTEN#, switches the LIFO's being read and written, which causes the block of data read from the structure to be reversed in sample order (See Example 4 in the Application Examples section).

The frequency with which TXFR# is asserted determines size of the data blocks in which sample order is reversed. For example, if TXFR# is asserted once every three CLK's, blocks of 3 data samples with order reversed, would be fed into the backward decimation registers. Note: altering the frequency or phase of TXFR# assertion once a filtering operation has been started will cause unknown results.

In applications which do not require sample order reversal, the FIR cells must be configured with data reversal disabled (see Table 2). In addition, TXFR# must be asserted to ensure proper data flow. In this configuration, data to the backward shifting decimation path is routed though a delay stage instead of the ping-pong LIFO's. The number of registers in the delay stage is based on the programmed decimation factor. Note: data reversal must be disabled and TXFR# must be asserted for filtering applications which do not use decimation.

The shifting of data through the forward and reverse decimation registers is enabled by asserting the SHFTEN# input. When SHFTEN# transitions high, data shifting is disabled, and the data sample latched into the part on the previous clock is the last input to the forward decimation path. When SHFTEN# is asserted, shifting of data through the decimation paths is enabled. The data sample at the part input when SHFTEN# is asserted will be the next data sample into the forward decimation path.

When operating the FIR cells as two independent filters, FIR A receives input data via INA0-9 and FIR B receives data from either INA0-9 or INB0-9 depending on the configuration (Table 1). When the FIR cells are configured as a single extended length filter, the forward and backward decimation paths are cascaded. In this mode, data is transferred from the forward decimation path to the backward decimation path by the Data Feedback Circuitry in FIR B. Thus, the manner in which data is read into the backward shifting decimation path is determined by FIR B's configuration.

When the decimation paths are cascaded, data is routed through the delay stage in FIR A's Data Feedback Circuitry.

The configuration of the FIR cells as even or odd length filters determines the point in the forward decimation path from which data is multiplexed to the Data Feedback Circuitry. For example, if the FIR cell is configured as an odd length filter, data prior to the last register in the third forward decimation stage is routed to the Feedback Circuitry. If the FIR cell is configured as an even length filter, data output from the third forward decimation stage is multiplexed to the Feedback Circuitry. This is required to insure proper data alignment with symmetric filter coefficients (See Application Examples).

ALUs

Data shifting through the forward and reverse decimation path feeds the "a" and "b" inputs of the ALUs respectively. The ALU's perform an "b+a" operation if the FIR cell is configured for even symmetric coefficients or an "b-a" operation if configured for odd symmetric coefficients.

For applications in which a pre-add or subtract is not required, the "a" or "b" input can be zeroed by disabling FWRD# or RVRS# respectively. This has the effect of producing an ALU output which is either "a","-a", or "b" depending on the filter symmetry chosen. For example, if the FIR cell is configured for an even symmetric filter with FWRD# low and RVRS# high, the data shifting through the forward decimation registers would appear on the ALU output.

Coefficient Bank

The output of the ALU is multiplied by a coefficient from one of 32 user programmable coefficient sets. Each set consists of 8 coefficients (4 coefficients for FIR A and 4 for FIR B). The active coefficient set is selected using CSEL0-4. The coefficient set may be switched every clock to support polyphase filtering operations.

The coefficients are loaded into on-board registers using the microprocessor interface, CIN0-9, A0-8, and WR#. Each multiplier within the FIR Cells is driven by a coefficient bank with one of 32 coefficients. These coefficients are addressed as shown in Table 3. The inputs A0-1 specify the Coefficient Bank for one of the four multipliers in each FIR Cell; A2 specifies FIR Cell A or B; Bits A7-3 specify one of 32 sets in which the coefficient is to be stored. For example, an address of 10dH would access the coefficient for the second multiplier in FIR B in the second coefficient set.

TABLE 3

A8	A7-3	A2	A1-0	FIR	BANK
1	xxxxx	0	00	A	0
1	xxxxx	0	01	A	1
1	xxxxx	0	10	A	2
1	xxxxx	0	11	A	3
1	xxxxx	1	00	B	0
1	xxxxx	1	01	B	1
1	xxxxx	1	10	B	2
1	xxxxx	1	11	B	3

FIR Cell Accumulator

The registered outputs from the multipliers in each FIR cell feed the FIR cell's accumulator. The ACCEN input controls each accumulator's running sum and the latching of data from the accumulator into the Output Holding Registers. When ACCEN is low, feedback from the accumulator adder is zeroed which disables accumulation. Also, output from the accumulator is latched into the Output Holding Registers. When ACCEN is asserted, accumulation is enabled and the contents of the Output Holding Registers remain unchanged.

Output MUX/Adder

The contents of each FIR Cell's Output Holding Register is summed or multiplexed in the Mux/Adder. The operation of the Mux/Adder is controlled by the MUX1-0 inputs as shown in Table 4. Applications requiring 10 bit data and 20 bit coefficients or 20 bit data and 10 bit coefficients are made possible by configuring the MUX/Adder to scale FIR B's output by 2^{-10} prior to summing with FIR A. When the Dual FIR is configured as two independent filters, the MUX1-0 inputs would be used to multiplex the filter outputs of each cell. For applications in which FIR A and B are configured as a single filter, the MUX/Adder is configured to sum the output of each FIR cell.

TABLE 4

MUX1-0 DECODING	
MUX1-0	**OUT0-27**
00	FIRA + FIRB (FIR B Scaled by 2^{-10})
01	FIRA + FIRB
10	FIRA
11	FIRB

Input/Output Formats

The Dual FIR supports mixed mode arithmetic with both unsigned and two's complement data and coefficients. The input and output formats for both data types is shown below. If the Dual FIR is configured as an even symmetric filter with unsigned data and coefficients, the output will be unsigned. Otherwise, the output will be two's complement.

INPUT DATA FORMAT INA0-9, INB0-9
FRACTIONAL TWO'S COMPLEMENT

9	8	7	6	5	4	3	2	1	0
-2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT9-27
FRACTIONAL TWO'S COMPLEMENT

27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9
-2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT0-8
FRACTIONAL TWO'S COMPLEMENT

8	7	6	5	4	3	2	1	0
2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}

INPUT DATA FORMAT INA0-9, INB0-9
FRACTIONAL UNSIGNED

9	8	7	6	5	4	3	2	1	0
2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT9-27
FRACTIONAL UNSIGNED

27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9
2^{9}	2^{8}	2^{7}	2^{6}	2^{4}	2^{5}	2^{3}	2^{2}	2^{1}	2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT0-8
FRACTIONAL UNSIGNED

8	7	6	5	4	3	2	1	0
2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}

The MUX/Adder can be configured to implement programmable rounding at bit locations 2^{-10} through 2^{1}. The round is implemented by adding a 1 to the specified location (see Table 2.0). For example, to configure the part such that the output is rounded to the 10 MSBs, OUT18-27, the round position would be chosen to be 2^{-1}.

Application Examples

In this section a number of examples which show even, odd, symmetric, asymmetric and decimating filters are presented. These examples are intended to show different operational modes of the HSP43168. The examples are all based on a dual filter configuration. However, the same principles apply when the part is configured with both FIR cells operating as a single filter.

Example 1. Even-Tap Symmetric Filter Example

The HSP43168 may be configured as two independent 8-tap symmetric filters as shown by the block diagram in Figure 2. Each of the FIR cells takes advantage of symmetric filter coefficients by pre-adding data samples common to a given coefficient. As a result, each FIR cell can implement an 8-tap symmetric filter using only four multipliers. Similarly, when the HSP43168 is configured in single filter mode a 16-tap symmetric filter is possible by using the multipliers in both cells.

The operation of the FIR cell is better understood by comparing the data and coefficient alignment for a given filter output, Figure 3, with the data flow through the FIR cell, as shown in Figure 4. The block diagrams in Figure 4 are a simplification of the FIR cell shown in Figure 1. For simplicity, the ALU's and FIR Cell Accumulators were replaced by adders, and the pipeline delay registers were omitted.

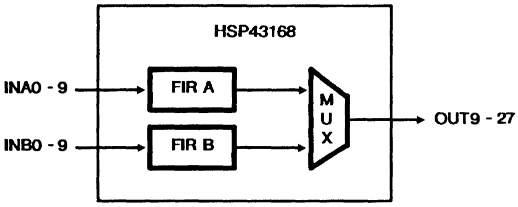


FIGURE 2. USING HSP43168 AS TWO INDEPENDENT FILTERS

In Figure 4, the order of the data samples within the filter cell is shown by the numbers in the forward and backward shifting decimation paths. The output of the filter cell is given by the equation at the bottom of each block diagram. Figure 4a shows the data sample alignment at the pre-adders for the data/coefficient alignment shown in Figure 3.

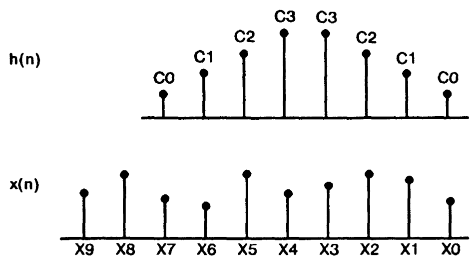
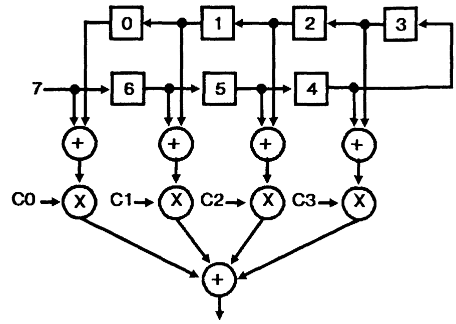


FIGURE 3. DATA/COEFFICIENT ALIGNMENT FOR 8-TAP EVEN SYMMETRIC FILTER

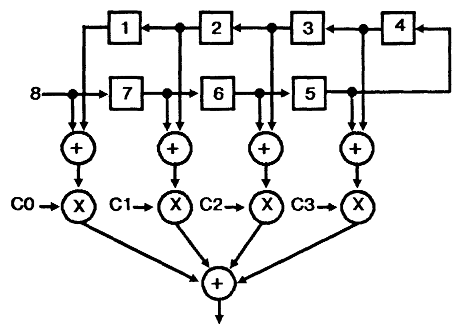
The dual filter application is configured by writing 1d0H to address 000H via the microprocessor interface, CIN0-9, A0-8, and WR#. Since this application does not use decimation, the 4th bit of the control register at address 001H must be set to disable data reversal (see Table 2). Failure to disable data reversal will produce erroneous results.

A. DATA FLOW AS DATA SAMPLE 7 IS CLOCKED INTO THE FEED FORWARD STAGE.



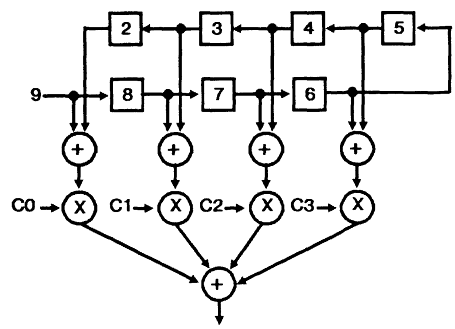
(X7+ X0)C0+ (X6+ X1)C1+ (X5+ X2)C2+ (X4+ X3)C3

B. DATA FLOW AS DATA SAMPLE 8 IS CLOCKED INTO THE FEED FORWARD STAGE.



(X8+ X1)C0+ (X7+ X2)C1+ (X6+ X3)C2+ (X5+ X4)C3

C. DATA FLOW AS DATA SAMPLE 9 IS CLOCKED INTO THE FEED FORWARD STAGE.



(X9+ X2)C0+ (X8+ X3)C1+ (X7+ X4)C2+ (X6+ X5)C3

FIGURE 4. DATA FLOW DIAGRAMS FOR 8-TAP SYMMETRIC FILTER

Using this architecture, only the unique coefficients need to be stored in the Coefficient Bank. For example, the above filter would be stored in the first coefficient set for FIR A by writing C0, C1, C2, and C3 to address 100H, 101H, 102H, and 103H respectively. To write the same filter to the first coefficient set for FIR B, the address sequence would change to 104H, 105H, 106H, and 107H.

To operate the HSP43168 in this mode, TXFR# is tied low to ensure proper data flow; both FWRD# and RVRS# are tied low to enable data samples from the forward and reverse data paths to the ALU's for pre-adding; ACCEN is tied low to prevent accumulation over multiple CLK's; SHFTEN# is tied low to allow shifting of data through the decimation registers; MUX0-1 is programmed to multiplex the output the of either FIR A or FIR B; CSEL0-4 is programmable to access the stored coefficient set, in this example CSEL = 00000.

Example 2. Odd-Tap Symmetric Filter Example

The HSP43168 may be configured as two independent 7-tap symmetric filters with a functional block diagram resembling Figure 2. As in the 8-tap filter example, the HSP43168 implements the filtering operation by summing data samples sharing a common coefficient prior to multiplication by that coefficient. However, for odd length filters the pre-addition requires that the center coefficient be scaled by 1/2.

The operation of the FIR cell for odd length filters is better understood by comparing the data/coefficient alignment in Figure 5 with the data flow diagrams in Figure 6. The block diagrams in Figure 6 are a simplification of the FIR cell shown in Figure 1.

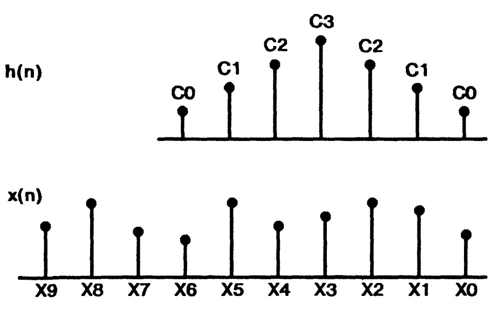
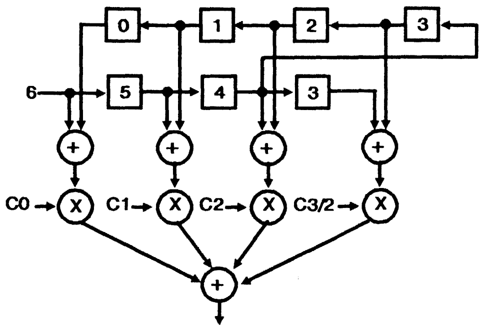


FIGURE 5. DATA/COEFFICIENT ALIGNMENT FOR 7-TAP SYMMETRIC FILTER

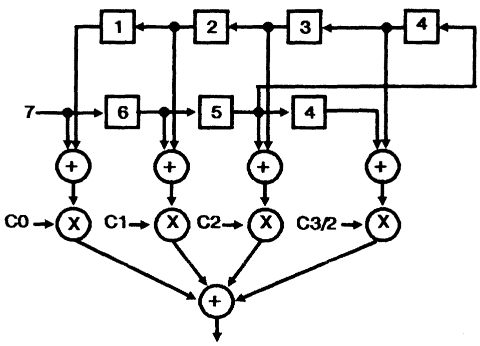
For odd length filters, proper data/coefficient alignment is ensured by routing data entering the last register in the third forward decimation stage to the backward shifting registers. In this configuration, the center coefficient must be scaled by 1/2 to compensate for the summation of the same data sample from both the forward and backward shifting registers.

A. DATA FLOW AS DATA SAMPLE 6 IS CLOCKED INTO THE FEED FORWARD STAGE.



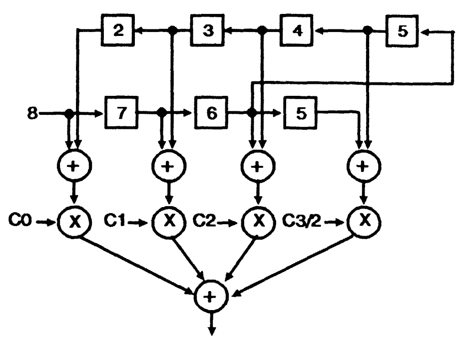
(X6+ X0)C0+ (X5+ X1)C1+ (X4+ X2)C2+ (X3+ X3)C3/2

B. DATA FLOW AS DATA SAMPLE 7 IS CLOCKED INTO THE FEED FORWARD STAGE.



(X7+ X1)C0+ (X6+ X2)C1+ (X5+ X3)C2+ (X4+ X4)C3/2

C. DATA FLOW AS DATA SAMPLE 8 IS CLOCKED INTO THE FEED FORWARD STAGE.



(X8+ X2)C0+ (X7+ X3)C1+ (X6+ X4)C2+ (X5+ X5)C3/2

FIGURE 6. DATA FLOW DIAGRAMS FOR 7-TAP SYMMETRIC FILTER.

In the data flow diagrams of Figure 6, the order of the data samples input in to the filter cell is shown by the numbers in the forward and backward shifting decimation paths. The output of the filter cell is given by the equation at the bottom of the block. The diagram in Figure 6a shows data sample alignment at the pre-adders for the data/coefficient alignment shown in Figure 5.

This dual filter application is configured by writing 110H to address 000H via the microprocessor interface, CIN0-9, A0-8, and WR#. Also, data reversal must be disabled by setting bit 4 of the control register at address 0001H. As in the 8-tap example, only the unique coefficients need to be stored in the Coefficient Bank. These coefficients are stored in the first coefficient set for FIR A by writing C0, C1, C2, and C3 to address 100H, 101H, 102H, and 103H respectively. To write the same filter to the first coefficient set for FIR B, the address sequence would change to 104H, 105H, 106H, and 107H. The control signals TXFR#, FWRD#, RVRS#, ACCEN, SHFTEN#, and CSEL0-4 are controlled as described in Example 1.

Example 3. Asymmetric Filter Example

The FIR cells within the HSP43168 can each calculate 4 asymmetric taps on each clock. Thus, a single FIR cell can implement an 8-tap asymmetric filter if the HSP43168 is clocked at twice the input data rate. Similarly, if the Dual is configured as a single filter, a 16- tap asymmetric filter is realizable.

For this example, the FIR cells are configured as two 8- tap asymmetric filters which are clocked at twice the input data rate. New data is shifted into the forward and backward decimation paths every other CLK by the assertion of SHFTEN#. The filter output is computed by passing data from each decimation path to the multipliers on alternating clocks. Two sets of coefficients are required, one for data on the forward decimation path, and one for data on the reverse path. The filter output is generated by accumulating the multiplier outputs for two CLKs.

The operation of this configuration is better understood by comparing the data/coefficient alignment in Figure 7 with the data flow diagrams in Figure 8. The ALU's have been omitted from the FIR cell diagrams because data is fed to the multipliers directly from the forward and reverse decimation paths. The data samples within the FIR cell are shown by the numbers in the decimation paths.

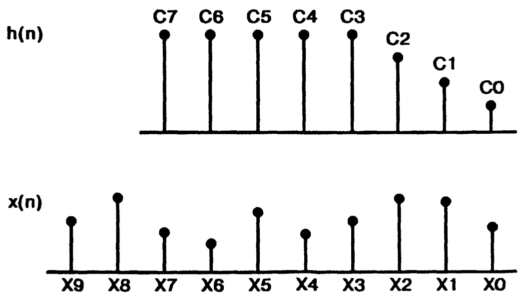
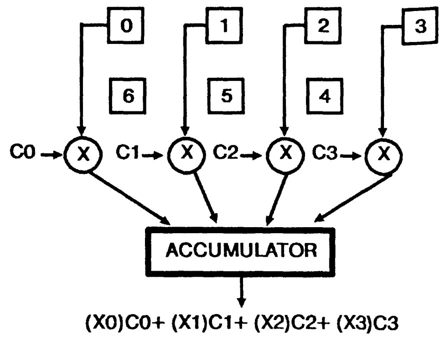
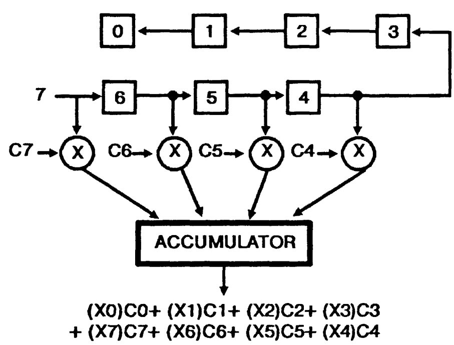


FIGURE 7. DATA/COEFFICIENT ALIGNMENT FOR 8-TAP ASYMMETRIC FILTER

A. DATA SHIFTING DISABLED, BACKWARD SHIFTING DECIMATION REGISTERS FEEDING MULTIPLIERS.



B. SHIFTING OF DATA SAMPLE 7 INTO FIR CELL ENABLED, FORWARD SHIFTING REGISTERS FEEDING MULTIPLIERS.



C. DATA SHIFTING DISABLED, BACKWARD SHIFTING DECIMATION REGISTERS FEEDING MULTIPLIERS.

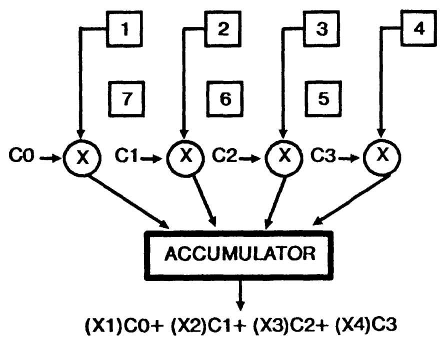
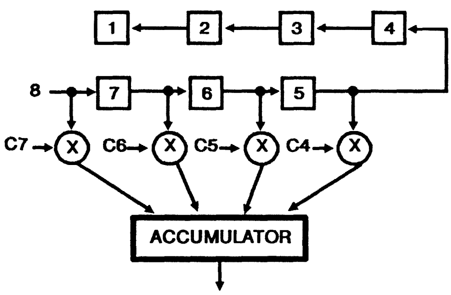


FIGURE 8. DATA FLOW DIAGRAMS FOR 8-TAP ASYMMETRIC FILTER

D. SHIFTING OF DATA SAMPLE 8 INTO FIR CELL ENABLED, FORWARD SHIFTING REGISTERS FEEDING MULTIPLIERS



(X1)C0+ (X2)C1+ (X3)C2+ (X4)C3
+ (X8)C7+ (X7)C6+ (X6)C5+ (X5)C4

FIGURE 8. DATA FLOW DIAGRAMS FOR 8-TAP ASYMMETRIC FILTER CONTINUED

For this application, each filter cell is configured as an odd length filter by writing 110H to the control register at address 000H. Even though an even tap filter is being implemented, the filter cells must be configured as odd length to ensure proper data flow. Also, the 4th bit at control address 001H must be set to disable data reversal, and TXFR# must be tied low. Since an 8-tap asymmetric filter is being implemented, two sets of coefficients must be stored. These eight coefficients could be loaded into the first two coefficient sets for FIR A by writing C0, C1, C2, C3, C7, C6, C5, and C4 to address 100H, 101H, 102H, 103H, 108H, 109H, 10aH, and 10bH respectively.

The sum of products required for this 8-tap filter require dynamic control over FWRD#, RVRS#, ACCEN, and CSEL0-4. The relative timing of these signals is shown in Figure 9.

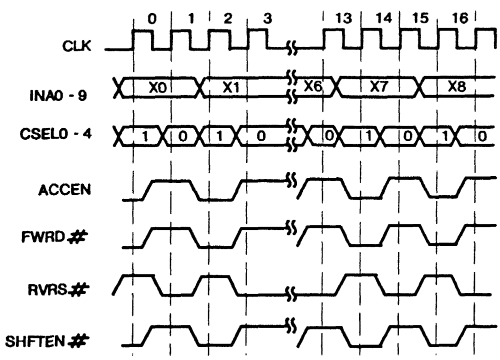


FIGURE 9. CONTROL TIMING FOR 8-TAP ASYMMETRIC FILTER

Example 4. Even-Tap Decimating Filter Example

The HSP43168 supports filtering applications requiring decimation to 16. In these applications the output data rate is reduced by a factor of N. As a result, N clock cycles can be used for the computation of the filter output. For example, each FIR cell can calculate 8 symmetric or 4 asymmetric taps in one clock. If the application requires decimation by two, the filter output can be calculated over two clocks thus boosting the number of taps per FIR cell to 16 symmetric or 8 asymmetric. For this example, each FIR cell is configured as an independent 24-tap decimate x3 filter.

The alignment of data relative to the 24 filter coefficients for a particular output is depicted graphically in Figure 10. As in previous examples, the HSP43168 implements the filtering operation by summing data samples prior to multiplication by the common coefficient. In this example an output is required every third CLK which allows 3 CLK's for computation. On each CLK, one of three sets of coefficients are used to calculate 8 of the filter taps. The block diagrams in Figure 12 show the data flow and accumulator output for the data/coefficient alignment in Figure 10.

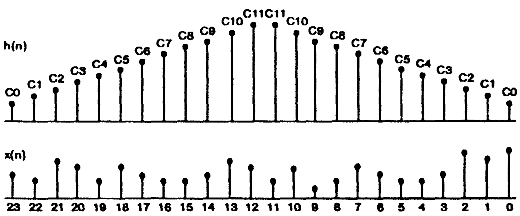
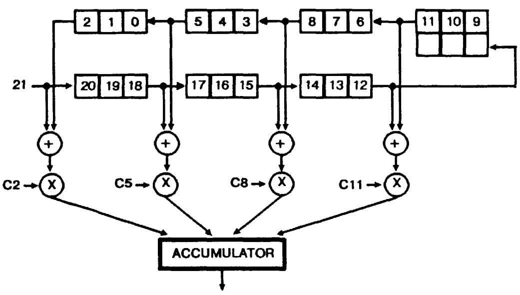


FIGURE 10. DATA/COEFFICIENT ALIGNMENT FOR 24-TAP DECIMATE BY 3 FIR FILTER

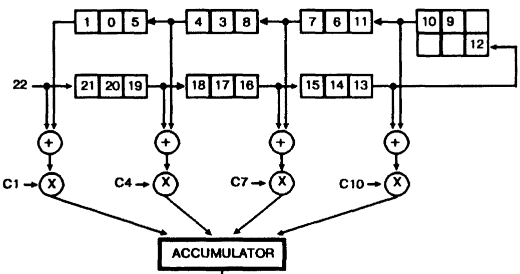
Proper data and coefficient alignment is achieved by asserting TXFR# once every three CLK's to switch the LIFO's which are being read and written. This has the effect of feeding blocks of three samples into the backward shifting decimation path which are reversed in sample order. In addition, ACCEN is de-asserted once every three clocks to allow accumulation over three CLK's. The three sets of coefficients required in the calculation of a 24-tap symmetric filter are cycled through using CSEL0-4. The timing relationship between the CSEL0-4, ACCEN, and TXFR# are shown in Figure 12.

A. COMPUTATIONAL FLOW AS DATA SAMPLE 21 IS CLOCKED INTO THE FEED FORWARD STAGE



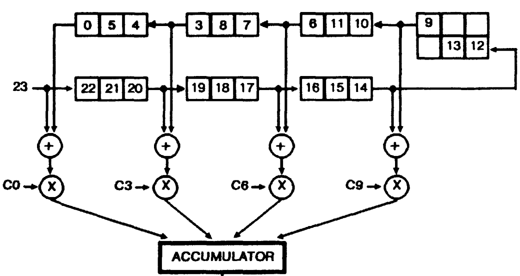
(X2+ X21)C2+ (X5+ X18)C5+ (X8+ X15)C8+ (X11+ X12)C11

B. COMPUTATIONAL FLOW AS DATA SAMPLE 22 IS CLOCKED INTO THE FEED FORWARD STAGE



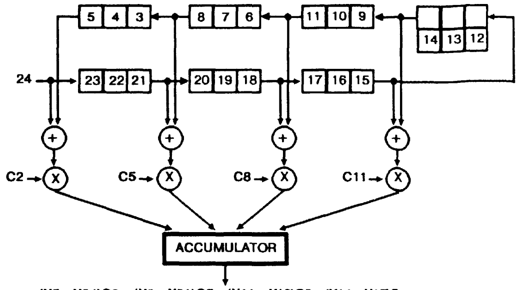
(X1+ X22)C1+ (X4X19)C4+ (X7+ X16)C7+ (X10+ X13)C10
+ (X2+ X21)C2+ (X5+ X18)C5+ (X8+ X15)C8+ (X11+ X12)C11

C. COMPUTATIONAL FLOW AS DATA SAMPLE 23 IS CLOCKED INTO THE FEED FORWARD STAGE



(X0+ X23)C0+ (X3+ X20)C3+ (X6+ X17)C6+ (X9+ X14)C9
+ (X1+ X22)C1+ (X4+ X19)C4+ (X7+ X16)C7+ (X10+ X13)C10
+ (X2+ X21)C2+ (X5+ X18)C5+ (X8+ X15)C8+ (X11+ X12)C11

D. COMPUTATIONAL FLOW AS DATA SAMPLE 24 IS CLOCKED INTO THE FEED FORWARD STAGE



(X5+ X24)C0+ (X8+ X21)C5+ (X11+ X18)C8+ (X14+ X15)C11

FIGURE 11. DATA FLOW DIAGRAMS FOR 24-TAP DECIMATE BY 3 FIR FILTER

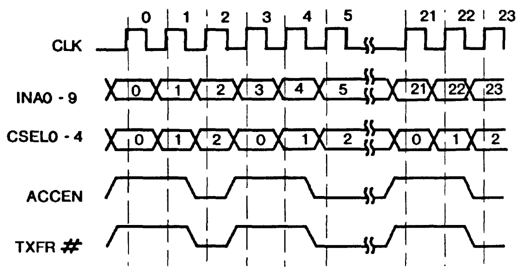


FIGURE 12. CONTROL SIGNAL TIMING FOR 24-TAP DECIMATE X3 FILTER

To operate in this mode the Dual is configured by writing 1d2 to address 000H via the microprocessor interface, CIN0-9, A0-8, and WR#. Data reversal must be enabled see (Table 2.0). The 12 unique coefficients for this example are stored as three sets of coefficients for either FIR cell. For FIR A, the coefficients are loaded into the Coefficient Bank by writing C2, C5, C8, C11, C1, C4, C7, C10, C0, C3, C6, and C9 to address 100H, 101H, 102H, 103H, 108H, 109H, 10aH, 10bH, 110H, 111H, 112H, and 113H respectively.

Example 5. Odd-Tap Decimating Symmetric Filter

This example highlights the use of the HSP43168 as two independent, 23-tap, symmetric, decimate by 3 filters. In this example, the operational differences in the control signals and data reversal structure may be compared to the previously discussed even-tap decimating filter.

As in the 24-tap example, an output is required every third CLK which allows 3 CLK's for computation. On each CLK, one of three sets of coefficients are used to calculate the filter taps. Since this is an odd length filter, the center coefficient must be scaled by 1/2 to compensate for the summation of the same data sample from the forward and backward shifting decimation paths.The block diagrams in Figure 14 show the data flow and accumulator output for the data coefficient alignment in Figure 13.

Proper data and coefficient alignment is achieved by asserting TXFR# once every three CLK's to switch the LIFO's which are being read and written. For odd length filters, data prior to the last register in the forward decimation path is routed to the Feedback Circuitry. As a result, TXFR# should be asserted one cycle prior to the input data samples which align with the center tap. The timing relationship between the CSEL0-5, ACCEN, and TXFR# are shown in Figure 15.

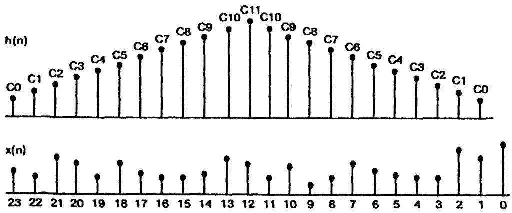
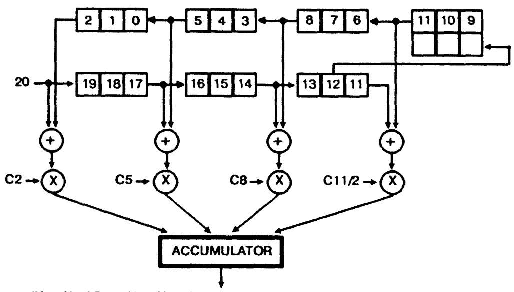
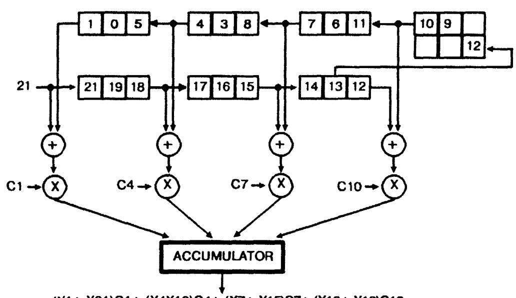


FIGURE 13. DATA/COEFFICIENT ALIGNMENT FOR 23-TAP DECIMATE BY 3 SYMMETRIC FILTER



(X2+ X20)C2+ (X5+ X17)C5+ (X8+ X14)C8+ (X11+ X11)C11/2

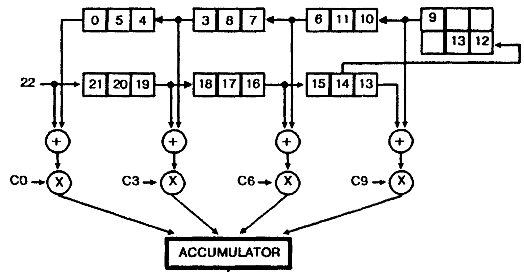
A. COMPUTATIONAL FLOW AS DATA SAMPLE 20 IS CLOCKED INTO THE FEED FORWARD STAGE



(X1+ X21)C1+ (X4X18)C4+ (X7+ X15)C7+ (X10+ X12)C10
+ (X2+ X20)C2+ (X5+ X17)C5+ (X8+ X14)C8+ (X11+ X11)C11/2

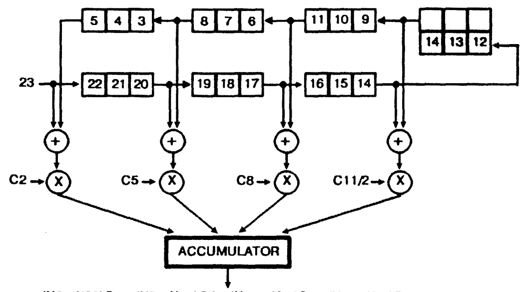
B. COMPUTATIONAL FLOW AS DATA SAMPLE 21 IS CLOCKED INTO THE FEED FORWARD STAGE

C. COMPUTATIONAL FLOW AS DATA SAMPLE 22 IS CLOCKED INTO THE FEED FORWARD STAGE



(X0+ X22)C0+ (X3+ X19)C3+ (X6+ X16)C6+ (X9+ X13)C9
+ (X1+ X21)C1+ (X4+ X18)C4+ (X7+ X15)C7+ (X10+ X12)C10
+ (X2+ X20)C2+ (X5+ X17)C5+ (X8+ X14)C8+ (X11+ X11)C11/2

D. COMPUTATIONAL FLOW AS DATA SAMPLE 23 IS CLOCKED INTO THE FEED FORWARD STAGE



(X5+ X23)C2+ (X8+ X20)C5+ (X11+ X17)C8+ (X14+ X14)C11/2

FIGURE 14. DATA FLOW DIAGRAMS FOR 23-TAP DECIMATE BY 3 SYMMETRIC FILTER

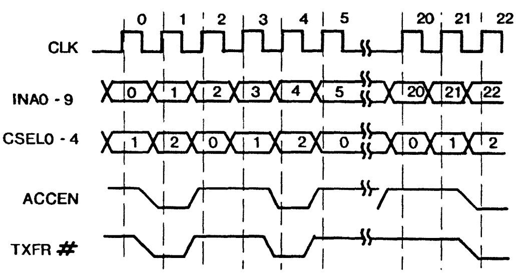


FIGURE 15. CONTROL SIGNAL TIMING FOR 23-TAP SYMMETRIC FILTER

To operate in this mode, the Dual is configured by writing 112H to address 000H via the microprocessor interface, CIN0-9, A0-8, and WR#. Data reversal must be enabled (see Table 2.0). The 12 unique coefficients for this example are stored as three sets of coefficients for either FIR cell. For FIR A, the coefficients are loaded into the Coefficient Bank by writing C2, C5, C8, (C11)/ 2, C1, C4, C7, C10, C0, C3, C6, and C9 to address 100H, 101H, 102H, 103H, 108H, 109H, 10aH, 10bH, 110H, 111H, 112H, and 113H respectively.

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output Voltage .... GND -0.5V to V_{CC} +0.5V
Storage Temperature .... -65°C to +150°C
ESD .... Class 1
Maximum Package Power Dissipation at +70°C .... 2.4W (MQFP), 3.6W (PLCC), 3.1W (PGA)
θ_{jc} .... 13.5°C/W (MQFP), 7.4°C/W (PLCC), 7.5°C/W (PGA)
θ_{ja} .... 33.0°C/W (MQFP), 22.3°C/W (PLCC), 33.5°C/W (PGA)
Gate Count 32529
Junction Temperature .... +175°C (PGA), +150°C (PLCC)
Lead Temperature (Soldering 10s) .... +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range, Commercial .... 5V ± 5%
Operating Temperature Range
Commercial .... 0°C to +70°C

D.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
I_{CCOP}	Power Supply Current	-	363	mA	V_{CC} = Max CLK Frequency 33MHz Note 2, Note 3, Note 4
I_{CCSB}	Standby Power Supply Current	-	500	μA	V_{CC} = Max, Outputs Not Loaded
I_I	Input Leakage Current	-10	10	μA	V_{CC} = Max, Input = 0V or V_{CC}
I_O	Output Leakage Current	-10	10	μA	V_{CC} = Max, Input = 0V or V_{CC}
V_{IH}	Logical One Input Voltage	2.0	-	V	V_{CC} = Max
V_{IL}	Logical Zero Input Voltage	-	0.8	V	V_{CC} = Min
V_{OH}	Logical One Output Voltage	2.6	-	V	I_{OH} = -400θA, V_{CC} = Min
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} = 2mA, V_{CC} = Min
V_{IHC}	Clock Input High	3.0	-	V	V_{CC} = Max
V_{ILC}	Clock input Low	-	0.8	V	V_{CC} = Min
C_{IN}	Input Capacitance	-	12	pF	CLK Frequency 1MHz All measurements referenced to GND. T_A = +25°C, Note 1
C_{OUT}	Output Capacitance	-	12	pF	

NOTES:

1. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.
2. Power Supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 11mA/MHz.
3. Output load per test load circuit and C_L = 40pF.
4. Maximum junction temperature must be considered when operating part at high clock frequencies.

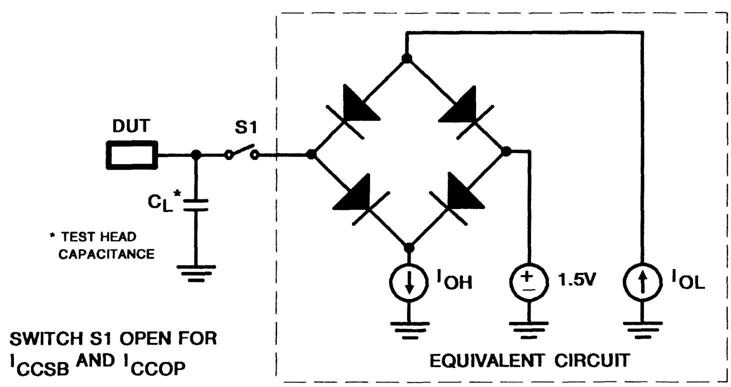
A.C. Electrical Specifications V_{CC} = +4.75V to +5.25V, T_A = 0°C to +70°C (Note 1)

SYMBOL	PARAMETER	33MHz MIN	33MHz MAX	45MHz MIN	45MHz MAX	COMMENTS
T_{CP}	CLK Period	30	-	22	-	ns
T_{CH}	CLK High	12	-	8	-	ns
T_{CL}	CLK Low	12	-	8	-	ns
T_{WP}	WR# Period	30	-	22	-	ns
T_{WH}	WR# High	12	-	10	-	ns
T_{WL}	WR# Low	12	-	10	-	ns
T_{AWS}	Set-up Time A0-8 to WR# Going Low	10	-	8	-	ns
TAWH	Hold Time A0-8 from WR# Going High	0	-	0	-	ns
TCWS	Set-up Time CIN0-9 to WR# Going High	12	-	10	-	ns
TCWH	Hold Time CIN0-9 from WR# Going High	1	-	1	-	ns
TWLCL	Set-up Time WR# Low to CLK Low	5	-	3	-	ns, Note 2
TCVCL	Set-up Time CIN0-9 to CLK Low	7	-	7	-	ns, Note 2
TECS	Set-up Time CSEL0-5, SHFTEN#, FWRD#, RVRS#, TXFR#, INA0-9, INB0-9, ACCEN, MUX0-1 to CLK Going High	15	-	12	-	ns
TECH	Hold Time CSEL0-5, SHFTEN#, FWRD#, RVRS#, TXFR#, INA0-9, INB0-9, ACCEN, MUX0-1 to CLK Going High	0	-	0	-	ns
TDO	CLK to Output Delay OUT0-27	-	14	-	12	ns
TOE	Output Enable Time	-	12	-	12	ns
TOD	Output Disable Time	-	12	-	12	ns, Note 3
TRF	Output Rise, Fall Time	-	6	-	6	ns, Note 3

NOTES:

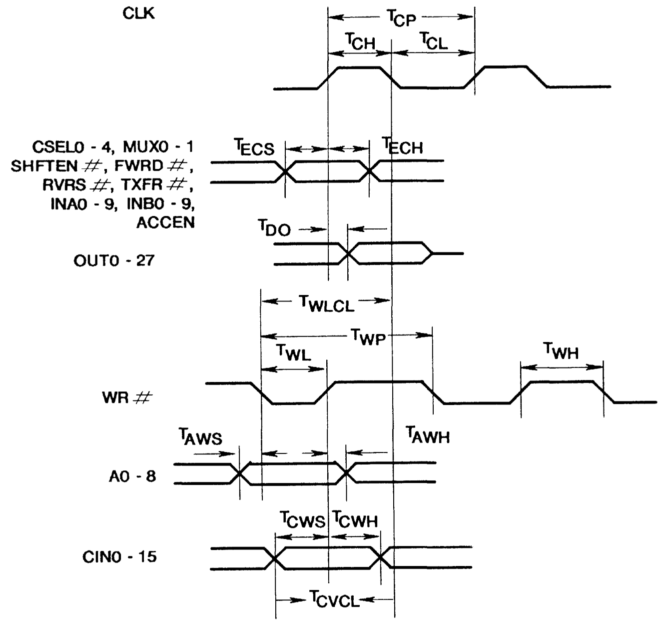
1. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -400μA. Input reference level CLK = 2.0V. Input reference level for all other inputs is 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V, V_{ILC} = 0V.
2. Set-up time requirement for loading of data on CIN0-9 to guarantee recognition on the following clock.
3. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.

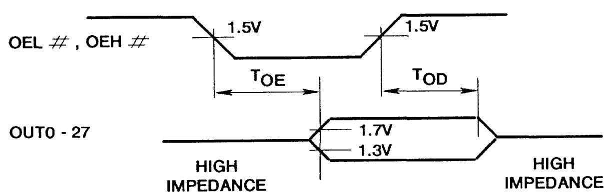
A.C. Test Load Circuit



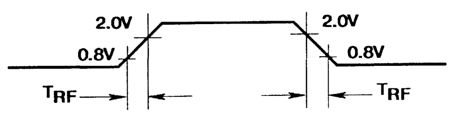
3
1D FILTERS

Waveforms





OUTPUT ENABLE, DISABLE TIMING



OUTPUT RISE AND FALL TIMES

HARRIS SEMICONDUCTOR

HSP43168/883

January 1994

Dual FIR Filter

Features

- **This Circuit Is Processed In Accordance to MIL-STD-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Two Independent 8-Tap FIR Filters Configurable as a Single 16-Tap FIR**
- **10-Bit Data & Coefficients**
- **On-Board Storage for 32 Programmable Coefficient Sets**
- **Up To: 256 FIR Taps, 16 x 16 2-D Kernels, or 10 x 20-Bit Data and Coefficients**
- **Programmable Decimation to 16**
- **Programmable Rounding on Output**
- **Standard Microprocessor Interface**
- **33MHz, 25.6MHz Versions**

Applications

- **Quadrature, Complex Filtering**
- **Correlation**
- **Image Processing**
- **PolyPhase Filtering**
- **Adaptive Filtering**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43168GM-25/883	-55°C to +125°C	84 Lead PGA
HSP43168GM-33/883	-55°C to +125°C	84 Lead PGA

Description

The HSP43168 Dual FIR Filter consists of two independent 8-tap FIR filters. Each filter supports decimation from 1 to 16 and provides on-board storage for 32 sets of coefficients. The Block Diagram shows two FIR cells each fed by a separate coefficient bank and one of two separate inputs. The outputs of the FIR cells are either summed or multiplexed by the MUX/Adder. The compute power in the FIR Cells can be configured to provide quadrature filtering, complex filtering, 2-D convolution, 1-D/2-D correlations, and interpolating/decimating filters.

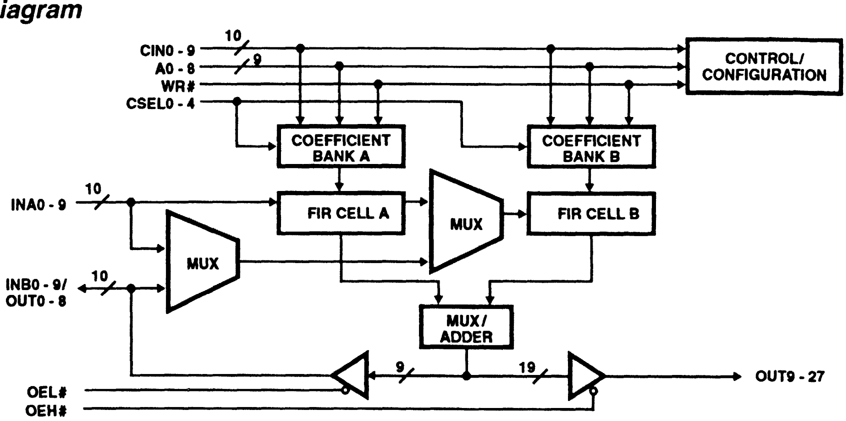
The FIR cells take advantage of symmetry in FIR coefficients by pre-adding data samples prior to multiplication. This allows an 8-tap FIR to be implemented using only 4 multipliers per filter cell. These cells can be configured as either a single 16-tap FIR filter or dual 8-tap FIR filters. Asymmetric filtering is also supported.

Decimation of up to 16 is provided to boost the effective number of filter taps from 2 to 16 times. Further, the decimation registers provide the delay necessary for fractional data conversion and 2-D filtering with kernels to 16x16.

The flexibility of the Dual is further enhanced by 32 sets of user programmable coefficients. Coefficient selection may be changed asynchronously from clock to clock. The ability to toggle between coefficient sets further simplifies applications such as polyphase or adaptive filtering.

The HSP43168 is a low power fully static design implemented in an advanced CMOS process. The configuration of the device is controlled through a standard microprocessor interface.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3177.2**

Pinouts

84 PIN PGA
TOP VIEW

	11	10	9	8	7	6	5	4	3	2	1	
L	GND	OUT15	OUT14	OUT12	OUT10	OUT11	INB1	INB4	INB5	INB6	INB9	L
K	OUT18	V_{CC}	OUT16	OUT13	V_{CC}	INB0	INB2	GND	INB7	INB8	INA1	K
J	OUT19	OUT17			OUT9	OEL#	INB3			INA0	INA2	J
H	OUT21	OUT20								INA3	INA4	H
G	OUT24	OUT23	OUT25						INA7	INA5	INA6	G
F	OUT27	OUT22	OUT26						INA8	INA9	V_{CC}	F
E	OEH#	GND	CLK						CIN2	CIN1	CIN0	E
D	V_{CC}	ACCEN								GND	CIN3	D
C	TXFR#	FWRD #			A5	A6	CSEL0			CIN6	CIN4	C
B	SHFT EN#	MUX0	MUX1	A0	A3	A2	V_{CC}	CSEL2	CIN9	CIN7	CIN5	B
A	RVRS#	WR#	GND	A1	A4	A7	A8	CSEL1	CSEL3	CSEL4	CIN8	A PIN 'A1' ID
	11	10	9	8	7	6	5	4	3	2	1	

84 PIN PGA
BOTTOM VIEW

	11	10	9	8	7	6	5	4	3	2	1	
A	RVRS #	WR#	GND	A1	A4	A7	A8	CSEL1	CSEL3	CSEL4	CIN8	A PIN 'A1' ID
B	SHFT EN#	MUX0	MUX1	A0	A3	A2	V_{CC}	CSEL2	CIN9	CIN7	CIN5	B
C	TXFR#	FWRD #			A5	A6	CSEL0			CIN6	CIN4	C
D	V_{CC}	ACCEN								GND	CIN3	D
E	OEH#	GND	CLK						CIN2	CIN1	CIN0	E
F	OUT27	OUT22	OUT26						INA8	INA9	V_{CC}	F
G	OUT24	OUT23	OUT25						INA7	INA5	INA6	G
H	OUT21	OUT20								INA3	INA4	H
J	OUT19	OUT17			OUT9	OEL#	INB3			INA0	INA2	J
K	OUT18	V_{CC}	OUT16	OUT13	V_{CC}	INB0	INB2	GND	INB7	INB8	INA1	K
L	GND	OUT15	OUT14	OUT12	OUT10	OUT11	INB1	INB4	INB5	INB6	INB9	L
	11	10	9	8	7	6	5	4	3	2	1	

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND-0.5V to V_{CC}+0.5V
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Temperature (Soldering 10s) . . . . . +300°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance — θ_{JA} / θ_{JC}
Ceramic PGA Package . . . . . 33.5°C/W 7.5°C/W
Maximum Package Power Dissipation at +125°C
Ceramic PGA Packazge . . . . . 1.49 W
Gate Count . . . . . 32529 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$-55° \le T_A \le +125°C$	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$-55° \le T_A \le +125°C$	-	0.8	V
Logical One Input Voltage Clock	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	$-55° \le T_A \le +125°C$	3.0	-	V
Logical Zero Input Voltage Clock	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	$-55° \le T_A \le +125°C$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400μA V_{CC}= 4.5V (Note 1)	1, 2, 3	$-55° \le T_A \le +125°C$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC}= 4.5V (Note 1)	1, 2, 3	$-55° \le T_A \le +125°C$	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55° \le T_A \le +125°C$	-10	+10	μA
Output Leakage Current	I_O	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55° \le T_A \le +125°C$	-10	+10	μA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND V_{CC} = 5.5V, Outputs Open	1, 2, 3	$-55° \le T_A \le +125°C$	-	500	μA
Operating Power Supply Current	I_{CCOP}	f = 25.6MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.5V (Note 2)	1, 2, 3	$-55° \le T_A \le +125°C$	-	281.6	mA
Functional Test	FT	(Note 3)	7, 8	$-55° \le T_A \le +125°C$	-	-	-

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 11mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH}(clock inputs) = 3.4V, V_{IH} (all other inputs) = 2.6V, V_{IL} = 0.4V, $V_{OH} \ge 1.5V$, and $V_{OL} \le 1.5V$.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	(-33MHz)		(-25MHz)		UNITS
					MIN	MAX	MIN	MAX	
CLK Period	T_{CP}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	30	-	39	-	ns
CLK High	T_{CH}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	12	-	15	-	ns
CLK Low	T_{CL}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	12	-	15	-	ns
WR# Period	T_{WP}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	30	-	39	-	ns
WR# High	T_{WH}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	12	-	15	-	ns
WR# Low	T_{WL}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	12	-	15	-	ns
Set-up Time; A0-8 to WR# Low	T_{AWS}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	10	-	10	-	ns
Hold Time; A0-8 to WR# High	T_{AWH}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	1	-	1	-	ns
Set-up Time; CIN0-9 to WR# High	T_{CWS}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	12	-	15	-	ns
Hold Time; CIN0-9 to WR# High	T_{CWH}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	1.5	-	1.5	-	ns
Set-up Time; WR# Low to CLK Low	T_{WLCL}	Note 3	9, 10, 11	$-55^o \leq T_A \leq +125^oC$	5	-	8	-	ns
Set-up Time; CIN0-9 to CLK Low	T_{CVCL}	Note 3	9, 10, 11	$-55^o \leq T_A \leq +125^oC$	8	-	8	-	ns
Set-up Time; CSEL0-5, SHFTEN#, FWRD#, RVRS#, TXFR#, MUX0-1 to CLK High	T_{ECS}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	15	-	17	-	ns
Hold Time; CSEL0-5, SHFTEN#, FWRD#, RVRS#, TXFR#, MUX0-1 to CLK High	T_{ECH}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	0	-	0	-	ns
CLK to Output Delay OUT0-27	T_{DO}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	-	15	-	17	ns
Output Enable Time	T_{OE}	Note 2	9, 10, 11	$-55^o \leq T_A \leq +125^oC$	-	12	-	12	ns

NOTES:

1. AC testing is performed as follows: Input levels (CLK Input) 4.0V and 0V; Input levels (all other inputs) 3.0V and 0V; Timing reference levels (CLK) 2.0V; All others 1.5V. V_{CC} = 4.5V and 5.5V. Output load per test load circuit with C_L = 40 pF. Output transition is measured at V_{OH} > 1.5V and V_{OL} < 1.5V.
2. Transition is measured at ±200mV from steady state voltage, Output loading per test load circuit, C_L = 40pF.
3. Set-up time requirements for loading of data on CIN0-9 to guarantee recognition on the following clock.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	(-33MHz)		(-25MHz)		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	V_{CC} = Open, f=1 MHz All measurements are referenced to device GND.	1	T_A = +25°C	-	12	-	12	pF
Output Capacitance	C_{OUT}		1	T_A = +25°C	-	12	-	12	pF
Output Disable Time	T_{OD}		1, 2	$-55° \leq T_A \leq +125°C$	-	12	-	12	ns
Output Rise Time	T_R	From 0.8V to 2.0V	1, 2	$-55° \leq T_A \leq +125°C$	-	8	-	8	ns
Output Fall Time	T_F	From 2.0V to 0.8V	1, 2	$-55° \leq T_A \leq +125°C$	-	8	-	8	ns

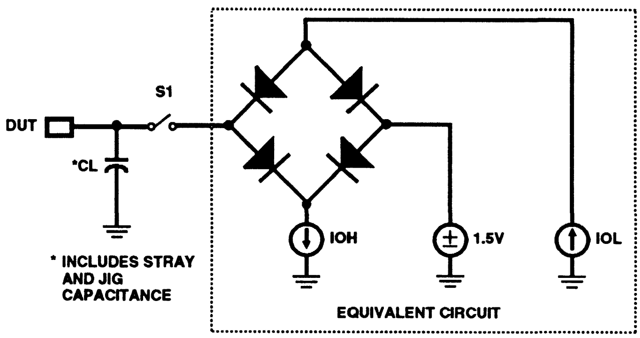
NOTE:

1. The parameters in Table 3 are controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
2. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

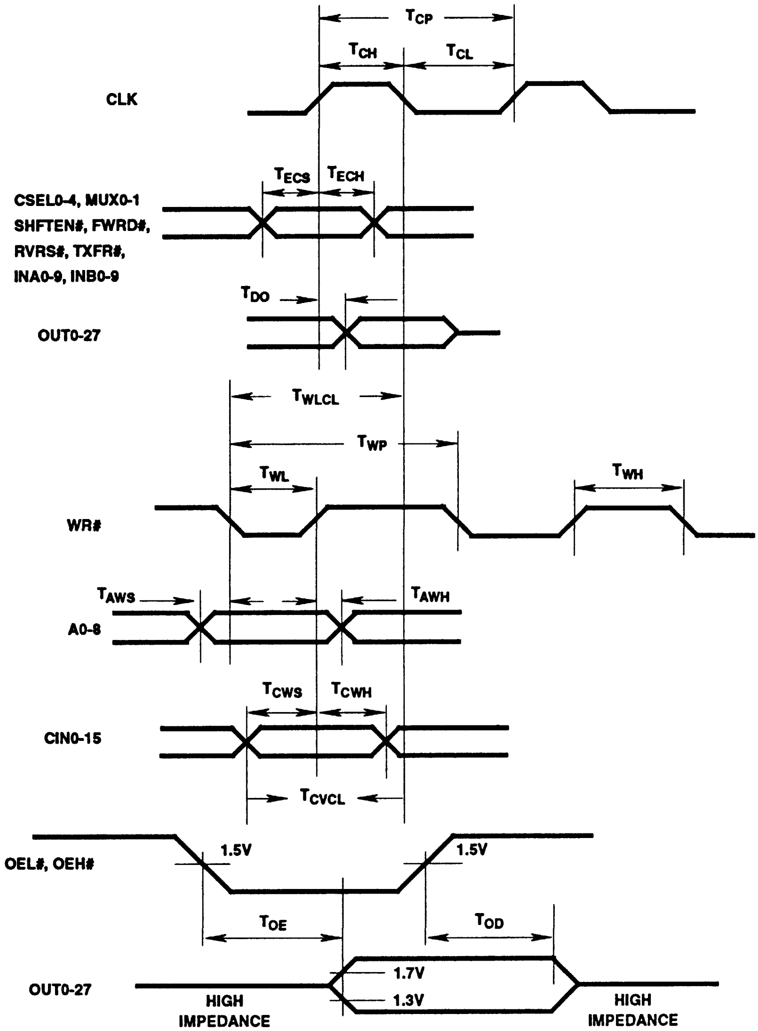
AC Test Load Circuit



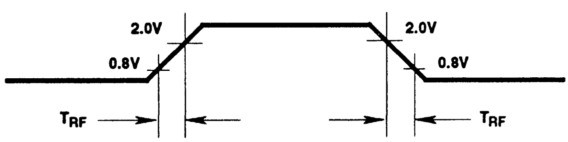
SWITCH S1 OPEN FOR I_{CCSB} AND I_{CCOP} TEST

3 1D FILTERS

Waveforms



OUTPUT ENABLE, DISABLE TIMING



OUTPUT RISE AND FALL TIMES

Burn-In Circuit

84 PIN PGA
BOTTOM VIEW

	11	10	9	8	7	6	5	4	3	2	1	
A	RVRS #	WR#	GND	A1	A4	A7	A8	CSEL1	CSEL3	CSEL4	CIN8	A PIN 'A1' ID
B	SHFT EN#	MUX0	MUX1	A0	A3	A2	V_{CC}	CSEL2	CIN9	CIN7	CIN5	B
C	TXFR#	FWRD #			A5	A6	CSEL0			CIN6	CIN4	C
D	V_{CC}	ACCEN								GND	CIN3	D
E	OEH#	GND	CLK						CIN2	CIN1	CIN0	E
F	OUT27	OUT22	OUT26						INA8	INA9	V_{CC}	F
G	OUT24	OUT23	OUT25						INA7	INA5	INA6	G
H	OUT21	OUT20								INA3	INA4	H
J	OUT19	OUT17			OUT9	OEL#	INB3			INA0	INA2	J
K	OUT18	V_{CC}	OUT16	OUT13	V_{CC}	INB0	INB2	GND	INB7	INB8	INA1	K
L	GND	OUT15	OUT14	OUT12	OUT10	OUT11	INB1	INB4	INB5	INB6	INB9	L
	11	10	9	8	7	6	5	4	3	2	1	

NOTES:

1. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND
3. V_{CC} = 5.5 ±0.5V.
4. 0.1µf (Min) capacitor between V_{CC} and GND per position.
5. F0 = 100KHz ±10%, F1 = F0/2, F2 = F1/2. . . , F16 = F15/2, 40 to 60% duty cycle.
6. Input voltage limits:
   V_{IL} = 0.8V Max, V_{IH} = 4.5 ±10%

PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	CIN8	F9	B11	SHFTEN	F14	F9	SUM26	$V_{CC}/2$	K2	INB8	F9
A2	CSEL4	F12	C1	CIN4	F7	F10	SUM22	$V_{CC}/2$	K3	INB7	F8
A3	CSEL3	F11	C2	CIN6	F9	F11	SUM27	$V_{CC}/2$	K4	GND	GND
A4	CSEL1	F9	C5	CSEL0	F8	G1	INA6	F7	K5	INB2	F3
A5	A8	F12	C6	A6	F11	G2	INA5	F6	K6	INB0	F1
A6	A7	F10	C7	A5	F12	G3	INA7	F8	K7	V_{CC}	V_{CC}
A7	A4	F11	C10	FWRD	F13	G9	SUM25	$V_{CC}/2$	K8	SUM13	$V_{CC}/2$
A8	A1	F12	C11	TXFR	F11	G10	SUM23	$V_{CC}/2$	K9	SUM16	$V_{CC}/2$
A9	GND	GND	D1	CIN3	F10	G11	SUM24	$V_{CC}/2$	K10	V_{CC}	V_{CC}
A10	WRB	F6	D2	GND	GND	H1	INA4	F5	K11	SUM18	$V_{CC}/2$
A11	RVRS	F12	D10	ACCEN	F13	H2	INA3	F4	L1	INB9	F10
B1	CIN5	F8	D11	V_{CC}	V_{CC}	H10	SUM20	$V_{CC}/2$	L2	INB6	F7
B2	CIN7	F10	E1	CIN0	F7	H11	SUM21	$V_{CC}/2$	L3	INB5	F6
B3	CIN9	F10	E2	CIN1	F8	J1	INA2	F3	L4	INB4	F5
B4	CSEL2	F10	E3	CIN2	F9	J2	INA0	F1	L5	INB1	F2
B5	V_{CC}	V_{CC}	E9	CLK	F0	J5	INB3	F4	L6	SUM11	$V_{CC}/2$
B6	A2	F11	E10	GND	GND	J6	OELB	F13	L7	SUM10	$V_{CC}/2$
B7	A3	F10	E11	OEHB	F14	J7	SUM9	$V_{CC}/2$	L8	SUM12	$V_{CC}/2$
B8	A0	F13	F1	V_{CC}	V_{CC}	J10	SUM17	$V_{CC}/2$	L9	SUM14	$V_{CC}/2$
B9	MUX1	F13	F2	INA9	F10	J11	SUM19	$V_{CC}/2$	L10	SUM15	$V_{CC}/2$
B10	MUX0	F12	F3	INA8	F9	K1	INA1	F2	L11	GND	GND

Metallization Topology

DIE DIMENSIONS:
314 x 348 x 19 ± 1mils

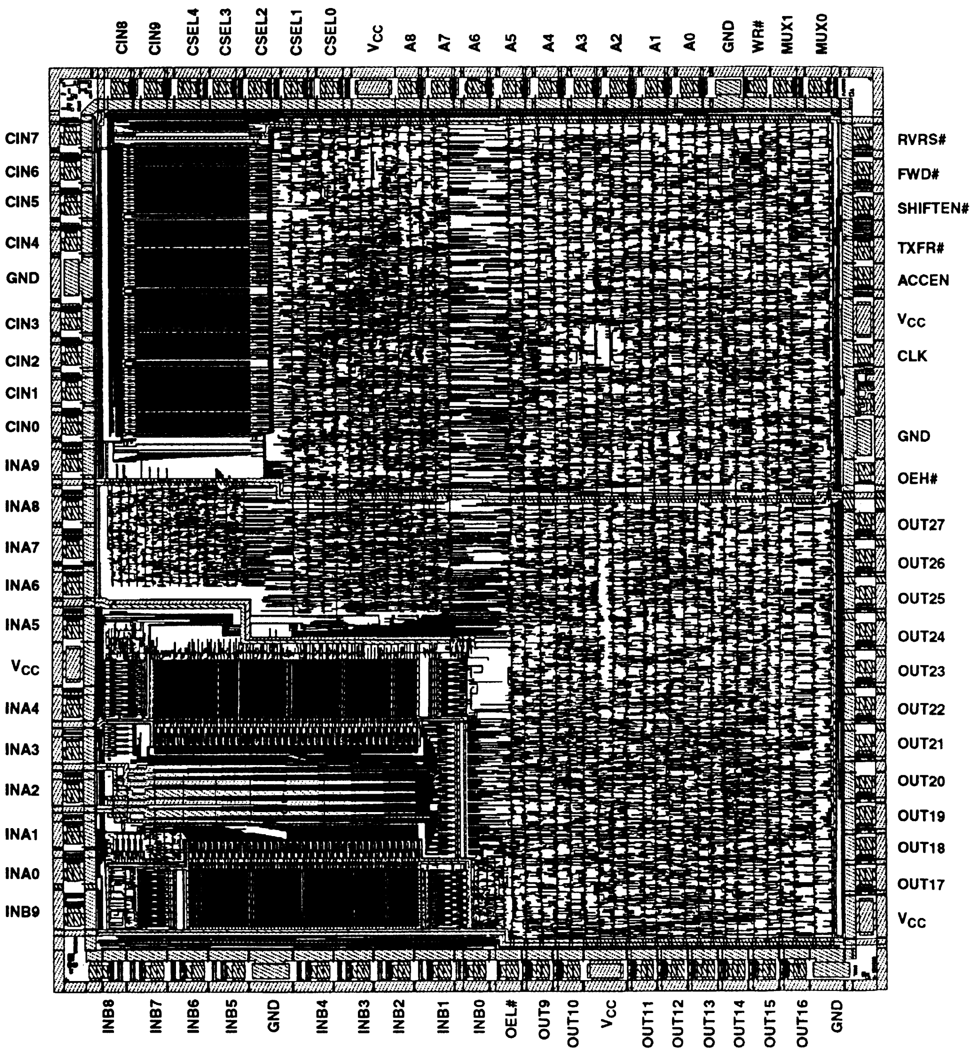
METALLIZATION:
Type: Si-Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:
1.93×10^5 A/cm^2

Metallization Mask Layout

HSP43168/883



HSP43216

January 1994

Halfband Filter

Features

- **Sample Rates to 52 MSPS**
- **Architected to Support Sample Rates to 104 MSPS Using External Multiplexer**
- **Four Modes of Operation:**
  - **Interpolate by 2 Filtering**
  - **Decimate by 2 Filtering**
  - **Quadrature to Real Signal Conversion**
  - **$F_S/4$ Quadrature Down Conversion Followed by Decimate by 2 Filtering**
- **67 Halfband FIR Filter with 20-Bit Coefficients**
- **1.24:1 Filter Shape Factor, >90dB Stopband Attenuation, <0.0003dB Passband Ripple**
- **Two's Complement or Offset Binary Outputs**
- **Programmable Rounding on Outputs**

Applications

- **Digital Down Conversion**
- **D/A and A/D pre/post Filtering**
- **Tuning Bandwidth Expansion for HSP45116 and HSP45106**

Description

The HSP43216 Halfband Filter addresses a wide variety of applications by combining $F_S/4$ (F_S = sample frequency) quadrature up/down convert circuitry with a fixed coefficient halfband filter processor as shown in the block diagram. These elements may be configured to operate in one of the four following modes: decimate by 2 filtering of a real input signal; interpolate by 2 filtering of a real input signal; $F_S/4$ quadrature down conversion of a real input signal followed by decimate-by-2 filtering to produce a complex analytic signal; interpolate-by-2 filtering of a complex analytic signal followed by $F_S/4$ quadrature up conversion to produce a real valued output.

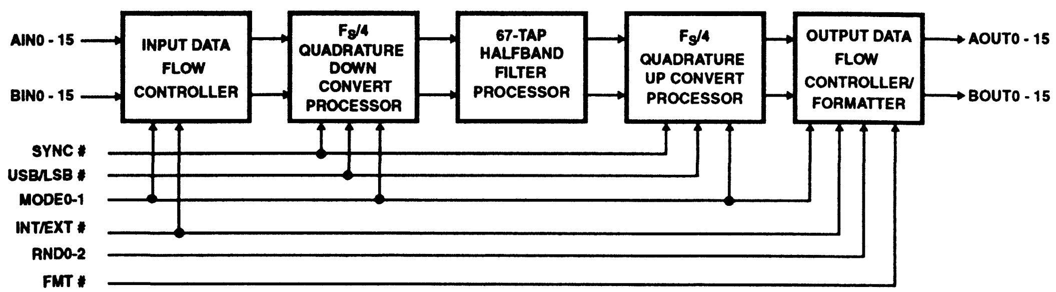
The frequency response of the HSP43216's halfband filter has a shape factor, (passband+transition band)/passband, of 1.24:1 with 90dB of stopband attenuation. The passband has less than 0.0003dB of ripple from $0F_S$ to $0.2F_S$ with stopband attenuation of greater than 90dB from $0.3F_S$ to Nyquist. At $0.25F_S$ the filter provides 6dB of attenuation.

The HSP43216 processes data streams with word widths up to 16-bits and data rates up to 52 MSPS. The processing through put of the part is easily doubled to rates of up to 104 MSPS by using the part together with an external multiplexer or demultiplexer. Programmable rounding is provided to support output precisions from 8-bits to 16-bits.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
HSP43216GC-52	0°C to +70°C	85 Lead PGA
HSP43216JC-52	0°C to +70°C	84 Lead PLCC

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3365.3**

Pinouts

85 PIN PGA
TOP VIEW

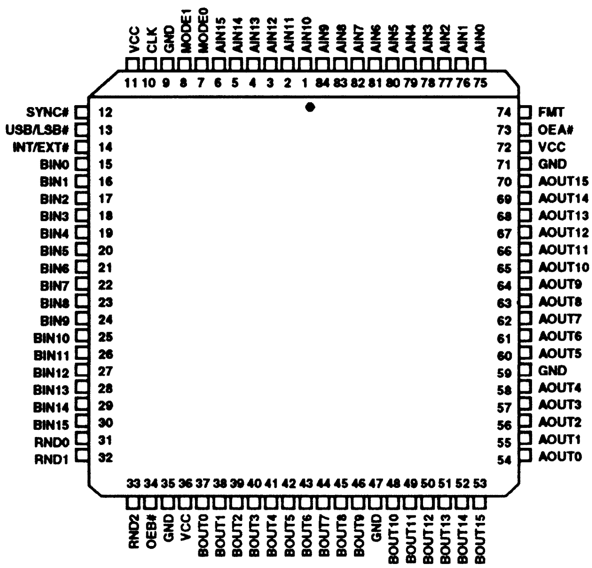
	11	10	9	8	7	6	5	4	3	2	1	
L	BOUT 15	BOUT 13	BOUT 12	BOUT 10	BOUT 8	GND	BOUT 4	BOUT 1	VCC	GND	RND1	L
K	AOUT 2	AOUT 0	BOUT 14	BOUT 11	BOUT 9	BOUT 5	BOUT 3	BOUT 0	OEB#	RND2	BIN15	K
J	AOUT 3	AOUT 1			BOUT 7	BOUT 6	BOUT 2			RND0	BIN14	J
H	GND	AOUT4								BIN13	BIN12	H
G	AOUT7	AOUT6	AOUT8						BIN8	BIN10	BIN9	G
F	AOUT 10	AOUT5	AOUT9						BIN7	BIN6	BIN11	F
E	AOUT 11	AOUT 12	AOUT 13						BIN3	BIN4	BIN5	E
D	AOUT 14	AOUT 15								BIN1	BIN2	D
C	GND	OEA#			AIN9	AIN10	AIN14		INDEX PIN	USB/ LSB#	BIN0	C
B	VCC	AIN0	AIN1	AIN4	AIN7	AIN6	AIN13	MODE 0	CLK	SYNC#	INT/ EXT#	B
A	FMT	AIN2	AIN3	AIN5	AIN8	AIN11	AIN12	AIN15	MODE1	GND	VCC	A
	11	10	9	8	7	6	5	4	3	2	1	PIN 'A1' ID

85 PIN PGA
BOTTOM VIEW

	1	2	3	4	5	6	7	8	9	10	11	
L	RND1	GND	VCC	BOUT1	BOUT4	GND	BOUT8	BOUT 10	BOUT 12	BOUT 13	BOUT 15	L
K	BIN15	RND2	OEB#	BOUT0	BOUT3	BOUT5	BOUT9	BOUT 11	BOUT 14	AOUT0	AOUT2	K
J	BIN14	RND0			BOUT2	BOUT6	BOUT7			AOUT1	AOUT3	J
H	BIN12	BIN13								AOUT4	GND	H
G	BIN9	BIN10	BIN8						AOUT8	AOUT6	AOUT7	G
F	BIN11	BIN6	BIN7						AOUT9	AOUT5	AOUT 10	F
E	BIN5	BIN4	BIN3						AOUT 13	AOUT 12	AOUT 11	E
D	BIN2	BIN1								AOUT 15	AOUT 14	D
C	BIN0	USB /LSB#	INDEX PIN		AIN14	AIN10	AIN9			OEA#	GND	C
B	INT/ EXT#	SYNC#	CLK	MODE0	AIN13	AIN6	AIN7	AIN4	AIN1	AIN0	VCC	B
A	VCC	GND	MODE1	AIN15	AIN12	AIN11	AIN8	AIN5	AIN3	AIN2	FMT	A
PIN 'A1' ID	1	2	3	4	5	6	7	8	9	10	11	

Pinouts (Continued)

84 LEAD PLCC
TOP VIEW

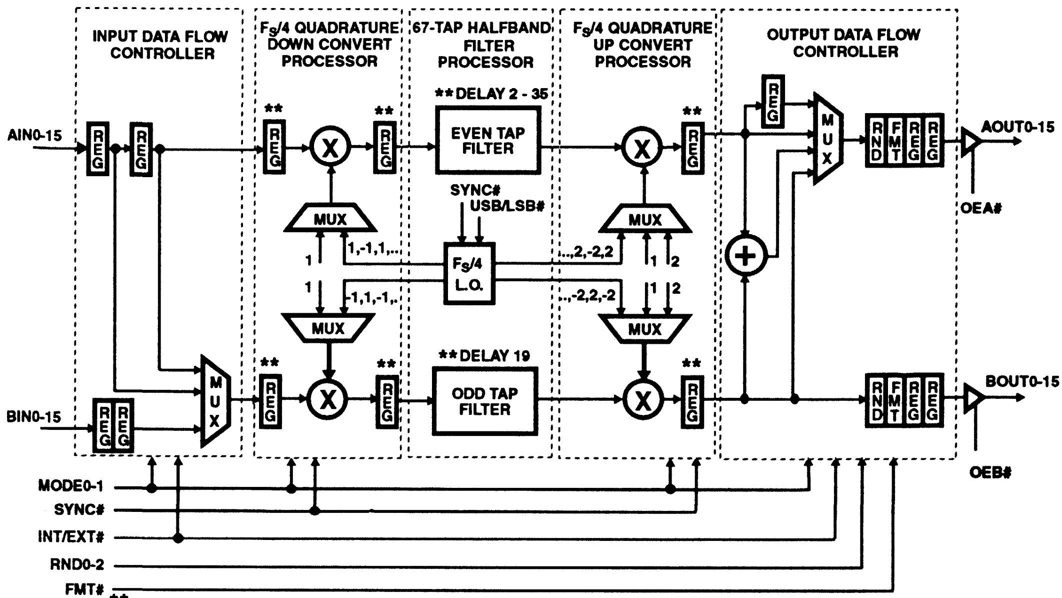


3

1D FILTERS

Pin Description

NAME	PLCC PIN	TYPE	DESCRIPTION
VCC	11, 36, 72	-	+5V Power
GND	9, 35, 47, 59, 71	-	Ground
CLK	10	I	Clock Input. (CMOS LEVEL)
AIN0-15	75 - 84, 1 - 6	I	Input Data Bus A. AIN0 is the LSB. Input data format is 16-bit Two's Complement.
BIN0-15	15 - 30	I	Input Data Bus B. BIN0 is the LSB. Input data format is 16-bit Two's Complement.
MODE0-1	7, 8	I	The Mode Select Inputs set one of four operational modes as highlighted in Table 1.
INT/EXT#	14	I	The Internal\External multiplexer select inputs set whether the data multiplex/demultiplex function required in the various operational modes is performed internally (High State) or externally to the chip (Low State).
SYNC#	12	I	This input is used to synchronize the input sample stream with the zero degree phase of the up or down convert Local Oscillators. In the straight decimate modes, this input can be use to synchronize the input sample stream with a particular phase of the halfband filter. (See the Operational Modes Section for additional information)
USB/LSB#	13	I	The Upper and Lower Sideband select line is used to specify the direction of frequency translation imparted on the data stream in the Up Convert and Quadrature to Real Convert Modes. (See Operational Modes Section for additional information)
RND0-2	31 - 33	I	The Round Select inputs set the number of output bits from eight (RND=000) to sixteen (RND=110). Least significant output bits are zeroed. See Table 4.
OEA#	73	I	Three State Control Output Bus A, OUTA0-15. Active Low.
OEB#	34	I	Three State Control Output Bus B, OUTB0-15. Active Low.
FMT	74	I	The Format select input is used to convert the two's complement output to offset binary (unsigned). When asserted high, the AOUT15 and BOUT15-bits are inverted from the normal two's complement representation.
AOUT0-15	54 - 58, 60 - 70	O	Output Bus A. AOUT0 is the LSB.
BOUT0-15	37 - 46, 48 - 53	O	Output Bus B. BOUT0 is the LSB.



** INDICATES ELEMENTS WHICH OPERATE AT CLK/2 WHEN THE INT/EXT# CONTROL INPUT IS HIGH.

FIGURE 1. HALFBAND BLOCK DIAGRAM

Functional Description

The operation of the HSP43216 centers around a fixed coefficient, 67-Tap, Halfband Filter Processor as shown in Figure 1. The Halfband Filter Processor operates stand alone to provide two fundamental modes of operation, interpolate or decimate by two filtering of a real signal. In two other modes, the Quadrature Up/Down Convert circuitry operates together with the Filter Processor block to provide $F_S/4$ Down Conversion with decimate by 2 filtering or Quadrature to Real Conversion.

In Down Convert and Decimate mode, a real input sample stream is spectrally shifted by $F_S/4$. Each component of the resulting complex signal is then halfband filtered and decimated by 2 to produce real and imaginary output samples at half of the input data rate.

In Quadrature to Real Conversion mode, the real and imaginary components of a quadrature input are interpolated by two and halfband filtered. The filtered result is then spectrally shifted by $F_S/4$ and the real component of this operation is output at twice the input sample rate.The HSP43216 is configured for different operational modes by setting the state of the mode control pins, MODE1-0 as shown in Table 1.

TABLE 1. MODE SELECT TABLE

MODE1-0	MODE
00	Decimate by Two
01	Interpolate by Two
10	Down Convert and Decimate
11	Quadrature to Real Conversion

Input Data Flow Controller

The Input Data Flow Controller routes data samples from the AIN0-15 and BIN0-15 inputs to the internal processing elements of the Halfband. The data routing paths are based on mode of operation and are more fully discussed in the Operational Modes section.

$F_S/4$ Quadrature Down Convert Processor

The $F_S/4$ Quadrature Down Convert Processor operates as a Quadrature LO which provides the negative $F_S/4$ spectral shift required to center the upper sideband of a real input signal at DC. This operation is equivalent to multiplying the real sample stream, x(n), by the quadrature components of the complex exponential $e^{-j(\pi/2)n}$ as given below:

$$x(n)e^{-j(\pi n/2)} = x(n)\cos(\pi n/2) + jx(n)\sin(-\pi n/2)$$

For added flexibility, a spectrally reversed version of the above process may be realized by configuring the Down Convert processor to impart a positive $F_S/4$ spectral shift on the input signal. This has the effect of centering the lower sideband of the input signal at DC and is achieved by reversing the sign of the sine term in the quadrature mix as shown below:

$$x(n)e^{j(\pi n/2)} = x(n)\cos(\pi n/2) + jx(n)\sin(\pi n/2)$$

The direction of the spectral shift imparted by the Down Convert Processor is set by the Upper Sideband/ Lower Sideband control input, USB/LSB#. When this input is "High", a $-F_S/4$ spectral shift is used to center the input signal's upper sideband at DC. When asserted low, a spectral shift of $F_S/4$ is used to center the lower sideband at

TABLE 2. FREQUENCY RESPONSE OF THE 67-TAP HALFBAND FILTER NORMALIZED TO THE SAMPLE RATE

FREQUENCY (NORMALIZED)	MAGNITUDE (dB)	FREQUENCY (NORMALIZED)	MAGNITUDE (dB)	FREQUENCY (NORMALIZED)	MAGNITUDE (dB)	FREQUENCY (NORMALIZED)	MAGNITUDE (dB)
0.000000	-0.000256	0.125000	-0.000278	0.250000	-6.020594	0.375000	-90.469534
0.003906	-0.000143	0.128906	-0.000098	0.253906	-7.989334	0.378906	-91.528735
0.007812	-0.000071	0.132812	0.000001	0.257812	-10.364986	0.382812	-98.960202
0.011719	-0.000013	0.136719	0.000077	0.261719	-13.194719	0.386719	-105.235066
0.015625	-0.000004	0.140625	0.000166	0.265625	-16.533196	0.390625	-97.073218
0.019531	-0.000001	0.144531	0.000106	0.269531	-20.447622	0.394531	-101.790858
0.023438	0.000032	0.148438	0.000015	0.273438	-25.024382	0.398438	-103.660592
0.027344	-0.000000	0.152344	-0.000022	0.277344	-30.379687	0.402344	-96.903272
0.031250	-0.000026	0.156250	-0.000048	0.281250	-36.679477	0.406250	-97.160860
0.035156	0.000002	0.160156	-0.000074	0.285156	-44.169450	0.410156	-106.804655
0.039062	0.000036	0.164062	-0.000022	0.289062	-53.259353	0.414062	-96.213761
0.042969	0.000050	0.167969	0.000005	0.292969	-64.619008	0.417969	-91.368358
0.046875	0.000021	0.171875	0.000009	0.296875	-79.291213	0.421875	-91.202963
0.050781	0.000008	0.175781	0.000041	0.300781	-90.247748	0.425781	-96.903271
0.054688	-0.000012	0.179688	0.000095	0.304688	-91.540418	0.429688	-103.058722
0.058594	-0.000140	0.183594	0.000090	0.308594	-96.987389	0.433594	-92.156508
0.062500	-0.000226	0.187500	-0.000012	0.312500	-97.990997	0.437500	-90.247741
0.066406	-0.000138	0.191406	-0.000037	0.316406	-94.450644	0.441406	-91.623161
0.070312	0.000010	0.195312	-0.000145	0.320312	-94.268681	0.445312	-98.760392
0.074219	0.000036	0.199219	-0.000208	0.324219	-97.250387	0.449219	-103.883238
0.078125	0.000179	0.203125	-0.000927	0.328125	-103.660592	0.453125	-96.861830
0.082031	0.000190	0.207031	-0.005089	0.332031	-105.940671	0.457031	-96.987388
0.085938	0.000064	0.210938	-0.018871	0.335938	-98.212931	0.460938	-100.046559
0.089844	0.000011	0.214844	-0.053894	0.339844	-94.313447	0.464844	-106.804655
0.093750	-0.000064	0.218750	-0.128250	0.343750	-95.354251	0.468750	-104.119091
0.097656	-0.000018	0.222656	-0.266964	0.347656	-98.447393	0.472656	-105.235066
0.101562	-0.000000	0.226562	-0.501238	0.351562	-103.249457	0.476562	-104.637666
0.105469	0.000020	0.230469	-0.866791	0.355469	-93.387604	0.480469	-105.940673
0.109375	0.000053	0.234375	-1.401949	0.359375	-91.390894	0.484375	-107.323099
0.113281	0.000012	0.238281	-2.145948	0.363281	-94.404415	0.488281	-102.375213
0.117188	-0.000022	0.242188	-3.137997	0.367188	-103.883234	0.492188	-94.009640
0.121094	-0.000149	0.246094	-4.416657	0.371094	-93.245384	0.496094	-91.312516

DC. The SYNC# control input may be used to synchronize the incoming data stream with the zero degree phase of the complex exponential as described in the Operational Modes section.

The real and imaginary sample streams generated by the down convert operation are passed to the Halfband Filter block on the upper and lower processing legs respectively.

The Down Convert Processor is only active in Down Convert and Decimate Mode, MODE1-0 = 10. In the other modes, the data on the upper and lower processing legs pass unaltered.

67-Tap Halfband Filter Processor

The processing required to implement the 67-Tap Halfband filter is distributed across two polyphase branches comprised of even and odd tap filters as shown in Figure 1. The Even Tap Filter performs a filtering operation using the even indexed coefficients (even phase) of the halfband filter. The Odd Tap Filter uses the odd indexed coefficients (odd phase) of the halfband filter. Note: the odd tap filter's processing reduces to a delay and scale operation since the center tap is the only non-zero odd tap for a halfband filter. Together the polyphase filters perform the sum of-products required to implement the 67 tap halfband filter in an architecture capable of supporting a variety of operational modes. The frequency response of the halfband filter is given graphically in Figure 2 and in tabular form in Table 2.

The polyphase implementation of the halfband filter provides the flexibility to realize a variety of filter configurations. In Decimate by Two Mode, the outputs of the each polyphase branch are summed to yield the filter output. In Interpolate by Two mode, the polyphase filters produce independent outputs which are multiplexed into a single sample stream at the interpolated data rate. In the Up Convert and Down Convert Modes, the polyphase branches filter the real and imaginary components of a complex sample stream with the equivalent of identical 67-Tap Halfband Filters. For these modes, the real component is processed by the Even Tap filter and the imaginary component is processed by the Odd Tap filter. The Operational Modes Section provides further details regarding the data flow and operation of the Filter Processor for the various modes.

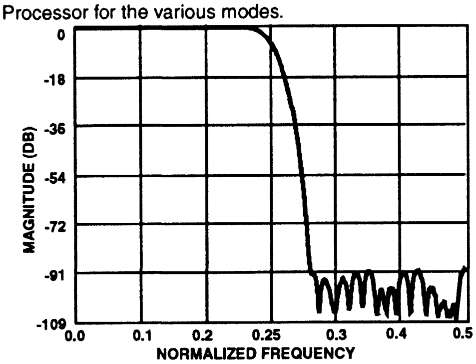


FIGURE 2. FREQUENCY RESPONSE OF 67 - TAP HALFBAND FILTER

F_S/4 Quadrature Up Convert Processor

The $F_S/4$ Quadrature Up Convert Processor provides the $F_S/4$ spectral shift used to construct a real signal from a complex sample stream. The operation performed is equivalent to multiplying a quadrature data stream, i(n)+jq(n), by samples of a complex exponential, $e^{-j(\pi/2)n}$, and outputting the real part of that mathematical operation as given below:

$$\mathrm{Real}\{(i(n) + jq(n))\, e^{j(\pi n/2)}\}$$

$$= \mathrm{Real}\{[i(n)\cos(\pi n/2) - q(n)\sin(\pi n/2)] + j\,[i(n)\sin(\pi n/2) + q(n)\cos(\pi n/2)]\}$$

$$= i(n)\cos(\pi n/2) - q(n)\sin(\pi n/2)$$

$$= i(n)\cos(\pi n/2) + q(n)\sin(-\pi n/2)$$

In the above operation, a positive $F_S/4$ spectral shift is imparted on the quadrature input which causes the upper sideband of the resulting real output to be defined by the spectral content of the input signal. For added flexibility, the Up Convert processor may be configured to impart a negative $F_S/4$ shift on the quadrature input which generates a real output whose lower sideband is defined the spectrum of the quadrature input. The state of the USB/LSB# control input determines the direction of the spectral shift. If this input is set "High", a positive $F_S/4$ shift is introduced by the Up Convert Processor. If USB/LSB# is asserted "Low", a negative $F_S/4$ spectral shift is introduced.

The Up Convert Processor implements the up convert operation by multiplying the in-phase and quadrature samples on the upper and lower processing legs by the nonzero sine and cosine terms in the above expression. The resulting data is then multiplexed together in the Output Flow Controller to yield the real output sample stream. The SYNC# control input may be used to align the zero degree phase of the Up Convert LO with a particular input sample as described in the Operational Modes Section.

The Up Convert Processor also scales the data streams output from the Filter Processor as required by the operational mode. In the modes which employ interpolation, the Up Convert Processor scales the Filter Processor's output by two to compensate for the attenuation of one half caused by the interpolation process. In down convert and decimate mode, the filter processor output is also scaled by two to compensate for the attenuation introduced by the down covert process. The scaling operations performed are summarized in Table 3.

TABLE 3. SCALE FACTORS APPLIED BY UP CONVERT PROCESSOR vs MODE

MODE	SCALE FACTOR
Decimate by Two (MODE1-0 = 00)	1.0
Interpolate by Two (MODE1-0 = 01)	2.0
Down Convert and Decimate (MODE1-0 = 10)	2.0
Quadrature to Real (MODE1-0 =11)	2.0

Output Data Flow Controller

The Output Flow Controller routes data to the AOUT0-15 and BOUT0-15 output depending on mode of operation. In decimate by two mode (MODE1-0 = 00), output from the filter processor's polyphase branches are summed and output through AOUT0-15. In Down Convert and Decimate mode (MODE1-0 = 10), real and imaginary data streams produced by the down convert process pass are output directly to AOUT0-15 and BOUT0-15 respectively. In the two modes using interpolation, MODE1-0 = 01 or 11, with internal multiplexing enabled, INT/EXT# set high, data sam ples output from the polyphase branches are internally multiplexed into a single stream and output via AOUT0-15. If a mode using interpolation is specified together with external multiplexing, INT/EXT# set low, the data stream multiplexing is performed off chip and the data on the upper and lower processing legs is output through AOUT0-15 and BOUT015.

The Output Data Flow Controller also sets the binary format and precision of the parts two 16-bit outputs. The data format is specified as either two's complement (FMT input low) or offset binary (FMT input high). The precision of the output data is set from 8 to 16-bits via the round control inputs, RND2-0. The RND2-0 inputs round the output data to a precision ranging from 8 to 16-bits as specified in Table 4. Saturation logic is incorporated in the output flow controller to insure that numerical growth associated with a worst case signal input or rounding condition saturates to a 16-bit value.

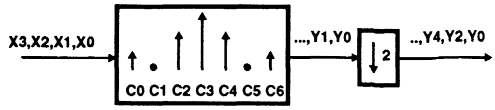
TABLE 4. OUTPUT ROUNDING CONTROL

RND 2-0	ROUND FUNCTION
000	Round output to 8-bits, AOUT15-8 and BOUT15-8, zero lower bits.
001	Round output to 9-bits, AOUT15-7 and BOUT15-7, zero lower bits.
010	Round output to 10-bits, AOUT15-6 and BOUT15-6, zero lower bits.
011	Round output to 11-bits, AOUT15-5 and BOUT15-5, zero lower bits.
100	Round output to 12-bits, AOUT15-4 and BOUT15-4, zero lower bits.
101	Round output to 14-bits, AOUT15-2 and BOUT15-2, zero lower bits.
110	Round output to 16-bits, AOUT15-0 and BOUT15-0.
111	Zero all outputs.

Operational Modes

Decimate By 2 Filter Mode (Mode1-0= 00)

The concept of operation for Decimate by Two Filter mode is most easily understood by comparing the 7 tap transversal filter implementation to the equivalent polyphase implementation. The transversal implementation is shown in Figure 3.



Y(0) = X0(C0)+X1(C1)+X2(C2)+X3(C3)+X4(C4)+X5(C5)+X6(C6)
* Y(1) = X1(C0)+X2(C1)+X3(C2)+X4(C3)+X5(C4)+X6(C5)+X7(C6)
Y(2) = X2(C0)+X3(C1)+X4(C2)+X5(C3)+X6(C4)+X7(C5)+X8(C6)
* Y(3) = X3(C0)+X4(C1)+X5(C2)+X6(C3)+X7(C4)+X8(C5)+X9(C6)

•
•
•

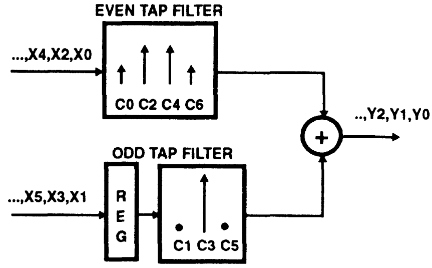
* INDICATES SAMPLES DISCARDED BY DECIMATION PROCESS

FIGURE 3. TRANSVERSAL IMPLEMENTATION OF DECIMATE BY 2 HALFBAND FILTER

By inspecting the sum-of-products for the decimated output in Figure 3, it is seen that even indexed input samples are always multiplied by the even filter coefficients and the odd samples are always multiplied by the odd coefficients. This computational partitioning is realized in the polyphase implementation shown in Figure 4.

In the polyphase implementation, the input data is broken into even and odd sample streams which are processed by a set of polyphase filters running at one half of the input data rate. These filters are designated as even or odd tap filters depending upon whether the coefficients were derived from the even or odd indexed coefficients of the original transversal filter. This architecture only produces the outputs which are not discarded by the decimation proces. NOTE: since the only non-zero tap for a halfband filter is the center tap, the Odd Tap Filter reduces to a delay and multiply operation.

The operation of the HSP43216 in Decimate by Two mode is analogous to the polyphase implementation in Figure 4. In this mode, the internal data paths are routed as shown in Figure 5A and Figure 5B. The different data flows depend on whether internal or external multiplexing has been selected using the INT/EXT# control input. In either case, an input data stream is decomposed into even and odd sample streams which are then routed to the even and odd tap polyphase filters. The output of each polyphase filter is summed and output via AOUT0-15.



Y(0) = X0(C0)+X1(C1)+X2(C2)+X3(C3)+X4(C4)+X5(C5)+X6(C6)
Y(1) = X2(C0)+X3(C1)+X4(C2)+X5(C3)+X6(C4)+X7(C5)+X8(C6)

•
•
•

FIGURE 4. POLYPHASE IMPLEMENTATION OF DECIMATE BY 2 HALFBAND FILTER

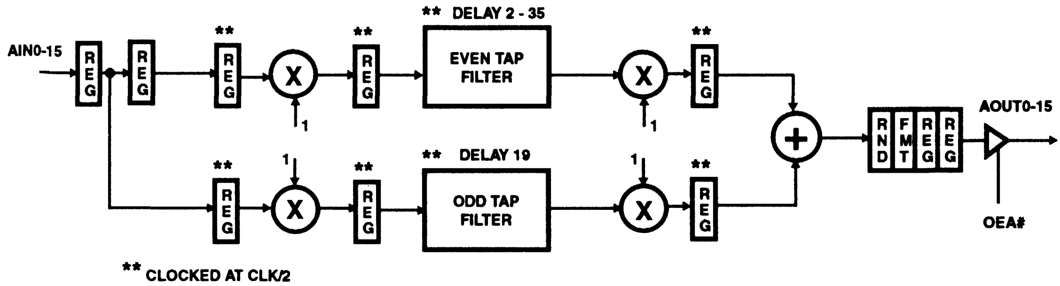


FIGURE 5A. DATA FLOW DIAGRAM FOR DECIMATE BY 2 FILTER MODE (INT/EXT# = 1)

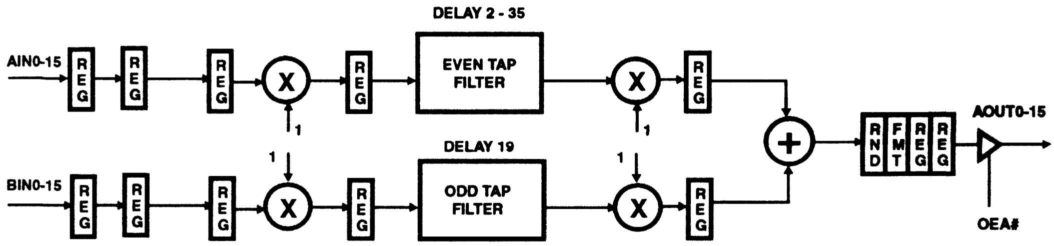
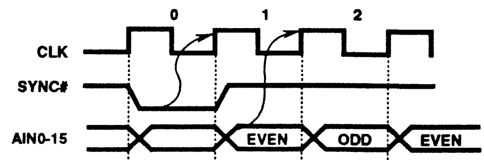


FIGURE 5B. DATA FLOW DIAGRAM FOR DECIMATE BY 2 FILTER MODE (INT/EXT# = 0)

If internal multiplexing is selected (INT/EXT# = 1), the input data stream is decomposed into even and odd samples internally by the processing elements operating at one half of the input CLK (see elements marked by "**" in Figure 5A). In this mode, the Data Flow Controller routes data samples input through AIN0-15 to upper and lower processing legs with a one sample relative delay. Since a new data sample is clocked into either of the processing legs at CLK/2, each leg processes a data stream comprised of every other input sample, and the one sample relative delay of each leg's input forces the even samples to be clocked into one leg while the odd samples are clocked into the other. The user may choose which sample gets routed to the upper (even) processing leg by asserting SYNC#. Specifically, a sample input on the CLK following the assertion of SYNC# will be routed to the upper processing leg as shown in Figure 6. With internal multiplexing, the minimum pipeline delay on the upper processing leg is 14 CLK's and the pipeline delay on the bottom leg is 47 CLK's. The filtered and decimated data stream is held on AOUT0-15 for 2 CLK's.

If external multiplexing is selected (INT/EXT# = 0), a demultiplex function is required off chip to break the input data into even and odd sample streams for input through AIN0-15 and BIN0-15. In this mode, the Data Flow Controller routes the even and odd sample streams directly to the following processing elements which are all running at the input CLK rate. This allows the device to perform decimate by two filtering on signals sampled at up to twice the maximum CLK rate of the device (104 MSPS). With external multiplexing, the minimum pipeline delay through the upper processing leg is 9 CLK's and the pipeline delay through the lower processing leg is 26 CLK's as shown in Figure 5B. In this mode, SYNC# has no effect on part operation. NOTE: for proper operation, the samples demultiplexed to the AIN0-15 input must precede those input to the BIN0-15 input in sample order. For example, given a data sequence x0, x1, x2 and x3, the demultiplex function would route x0 and x2 to AIN0-15 and x1 and x3 to BIN0-15.



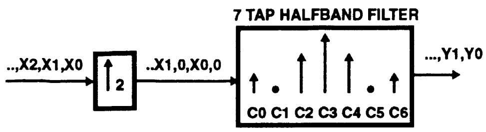
INPUTS DESIGNATED AS EVEN ARE PROCESSED ON THE UPPER LEG, INPUTS DESIGNATED AS ODD ARE PROCESSED ON THE LOWER LEG.

FIGURE 6. DATA SYNCHRONIZATION WITH PROCESSING LEGS (INT/EXT# = 1)

Interpolate By 2 Filter Mode (Mode1-0 = 01)

As with the Decimate by Two mode the concept of operation for the Interpolate by Two Filter mode is more easily understood by comparing a 7 tap transversal filter implementation to the equivalent polyphase implementation. The transversal implementation is shown in Figure 7.

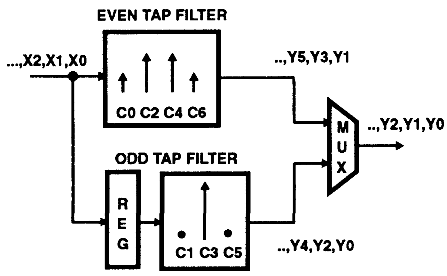
By inspecting filter outputs in Figure 7, it is seen that the even indexed outputs are the result of the sum-of-products for the odd coefficients, and the odd indexed outputs are theresult of the sum-of-products for the even coefficients. This computational partitioning is evident in the polyphase implementation shown in Figure 8.



Y(0) = 0(C0)+X0(C1)+0(C2)+X1(C3)+0(C4)+X2(C5)+0(C6)
Y(1) = X0(C0)+0(C1)+X1(C2)+0(C3)+X2(C4)+0(C5)+X3(C6)
Y(2) = 0(C0)+X1(C1)+0(C2)+X2(C3)+0(C4)+X3(C5)+0(C6)
Y(3) = X1(C0)+0(C1)+X2(C2)+0(C3)+X3(C4)+0(C5)+X4(C6)

⋮

FIGURE 7. TRANSVERSAL IMPLEMENTATION OF INTERPOLATE BY TWO HALFBAND FILTER.



Y0 = X0(C1)+X1(C3)+X2(C5)
Y1 = X0(C0)+X1(C2)+X2(C4)+X3(C6)
Y2 = X1(C1)+X2(C3)+X3(C5)

⋮

FIGURE 8. POLYPHASE IMPLEMENTATION OF INTERPOLATE BY TWO HALFBAND FILTER

In the polyphase implementation, the input data stream feeds even and odd tap filters running at the input sample rate. The interpolated sample stream is derived by multiplexing the output of each polyphase branch into a single data stream at twice the input sample rate. As in the Decimate by Two example, the even or odd tap filters are comprised of the even or odd indexed coefficients from the original transversal filter.

The operation of the HSP43216 in Interpolate by Two mode is analogous to the polyphase example above. In this mode the internal data flow is routed as shown in Figure 9A and Figure 9B. The different data flows depend on the selection of internal or external multiplexing via INT/EXT#. In this mode, data input through AIN0-15 is fed to the even and odd polyphase branches of the filter processor. The output of each branch is multiplexed together to generate the output data stream at the interpolated rate. NOTE: the output of each polyphase branch is scaled by two to compensate for the attenuation of one half caused by interpolation.

If internal multiplexing is selected (INT/EXT# = 1), the data stream input through AIN0-15 is fed to both the upper and lower processing legs as shown in Figure 9A. The output of each processing leg is then multiplexed together to produce the interpolated sample stream at twice the input sample rate. In this mode the device is clocked at the interpolated data rate to support the multiplexing of each processing leg's output into a single data stream. The upper and lower processing legs each run at the input data rate of CLK/2 as indicated by the "**" marking the various registers and processing elements in Figure 9A. In this mode, data samples are clocked into the part on every other rising edge of CLK. The SYNC# signal is used to specify which set of CLK

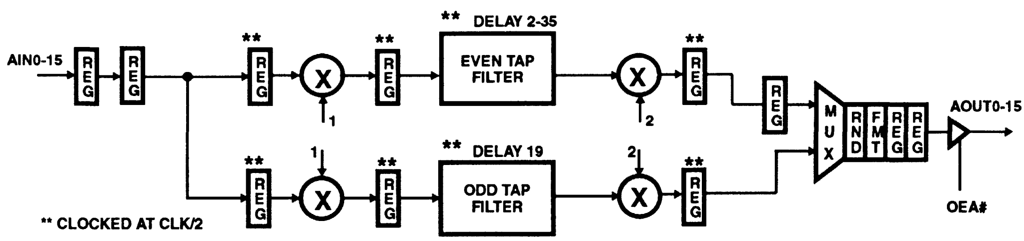


FIGURE 9A. DATA FLOW DIAGRAM FOR INTERPOLATE BY 2 FILTER MODE (INT/EXT# = 1)

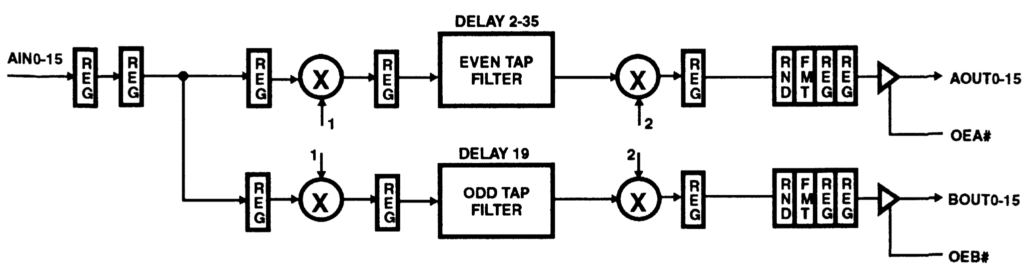


FIGURE 9B. DATA FLOW DIAGRAM FOR INTERPOLATE BY 2 FILTER MODE (INT/EXT# = 0) cycles are used to register data at the part's input. Specifically, every other rising edge of CLK starting one CLK after the assertion of SYNC# will be used to clock data into the part. With internal multiplexing the minimum pipeline delay through the upper processing leg is 15 CLK's and the pipeline delay through the lower processing leg is 48 CLK's.

If external multiplexing is selected (INT/EXT# = 0), the upper and lower processing legs are output through AOUT0-15 and BOUT0-15 for multiplexing into a single data stream off chip.This allows the processing legs to run at the maximum clock rate which coincides with an interpolated output data rate of 104 MSPS. NOTE: the samples output on BOUT0-15 precede those on AOUT0-15 in sample order. This requires a multiplexing scenario in which BOUT0-15 is selected before AOUT0-15. With external multiplexing, the minimum pipeline delay through the upper processing leg is 9 CLK's and the pipeline delay through the lower processing leg is 26 CLK's as shown in Figure 9B. In this mode SYNC# has no effect on part operation.

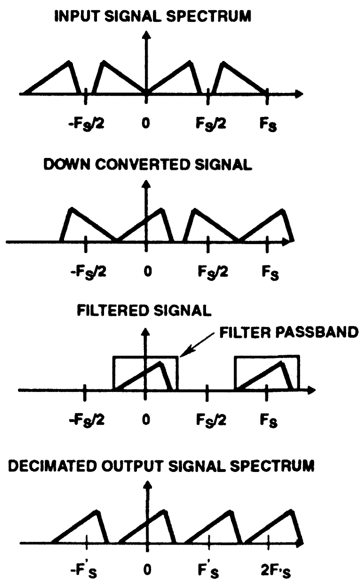
Down Convert and Decimate Mode (MODE1-0 = 10)

In Down Convert and Decimate Mode a real input signal is spectrally shifted $-F_S/4$ which centers the upper sideband at DC. This operation produces real and imaginary components which are each filtered and decimated by identical 67-tap halfband filters. For added flexibility, a positive $F_S/4$ spectral shift may be selected which centers the lower sideband at DC. The direction of the spectral shift is selected via USB/LSB# as described in the Quadrature Down Convert section. A spectral representation of the down convert and decimate operation is shown in Figure 10 (USB/LSB#=1). NOTE: each of the complex terms output by the Filter Processor are scaled by two to compensate for the attenuation of one half introduced by the down conversion process.

The Down Convert and Decimate mode is most easily understood by first considering the transversal implementation using a 7 tap filter as shown in Figure 11.

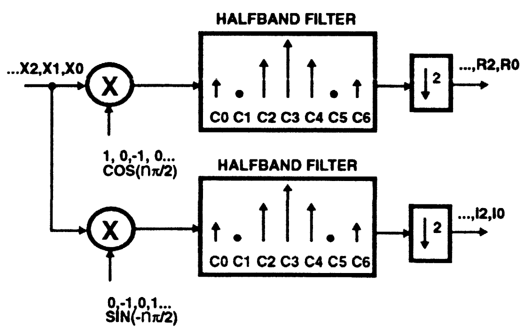
By examining the combination of down conversion, filtering and decimation, it is seen that the real outputs are only dependent on the sum-of-products for the even indexed samples and filter coefficients, and the imaginary outputs are only a function of the sum-of-products for the odd indexed samples and filter coefficients. This computational partitioning allows the quadrature filters required after down conversion to be realized using the same poly-phase processing elementsused in the previous two modes.

A functional block diagram of the polyphase implementation is shown in Figure 12. In this implementation, the input data stream is broken into even and odd sample streams and processed independently by the even and odd tap filters. By decomposing the sample stream into even and odd samples, the zero mix terms produced by the down convert LO drop out of the data streams, and the output of each of the filters represent the decimated data streams for both the real and imaginary outputs.



F_S = INPUT SAMPLE RATE
F'_S = DECIMATED SAMPLE RATE,$F_S/2$

FIGURE 10. DOWN CONVERT AND DECIMATE OPERATION



REAL OUTPUTS

R0 = X0(C0)+0(C1)-X2(C2)+0(C3)+X4(C4)+0(C5)-X6(C6)
• R1 = 0(C0)-X2(C1)+0(C2)+X4(C3)+0(C4)-X6(C5)+0(C6)
R2 = -X2(C0)+0(C1)+X4(C2)+0(C3)-X6(C4)+0(C5)+X4(C6)
• R3 = 0(C0)+X4(C1)+0(C2)-X6(C3)+0(C4)+X4(C5)+0(C6)
⋮

IMAGINARY OUTPUTS

I0 = 0(C0)-X1(C1)+0(C2)+X3(C3)+0(C4)-X5(C5)+0(C6)
• I1 = -X1(C0)+0(C1)+X3(C2)+0(C3)-X5(C4)+0(C5)+X7(C6)
I2 = 0(C0)+X3(C1)+0(C2)-X5(C3)+0(C4)+X7(C5)+0(C6)
• I3 = X3(C0)+0(C1)-X5(C2)+0(C3)+X7(C4)+0(C5)-X9(C6)
⋮

• INDICATES SAMPLES DISCARDED BY DECIMATION PROCESS

FIGURE 11. DOWN CONVERT AND DECIMATE FUNCTION USING TRANSVERSAL FILTERS

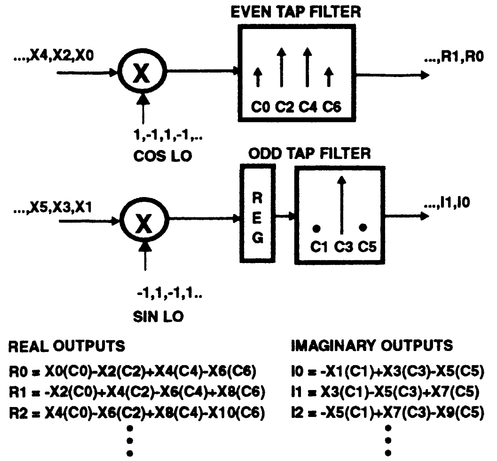
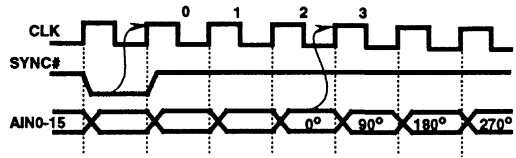


FIGURE 12. DOWN CONVERT AND DECIMATE FUNCTION USING POLYPHASE FILTERS

The HSP43216's implementation of Down Convert and Decimate mode is analogous to the polyphase solution shown in Figure 12. The part's data flow diagram for this mode is shown in Figure 13A and Figure 13B. As seen in the figures, the input sample data is broken into even and odd sample streams which feed the upper and lower processing legs as described in the Decimate By 2 Mode section. The data on each processing leg is then modulated with the non zero quadrature components of the complex exponent (see Quadrature Down Convert Section). Following this operation, the upper leg becomes the processing chain for the real (In-phase) component of the quadrature down conversion and the lower leg processes the complex (Quadrature) component of the down conversion. The filter processing block implements the equivalent of a decimate by two Halfband filter on each of the quadrature legs.

If internal multiplexing is specified (INT/EXT# = 1), the upper and lower processing legs are fed with even and odd sample streams which are derived from data input through AIN0-15. The input sample stream may be synchronized with the zero degree phase term of the down converter LO by using the SYNC# control input. For example, an input data sample will be fed into the real (upper) processing leg and mixed with the zero degree cosine term of the quadrature LO if it is input on the 4th CLK following the assertion of SYNC# as shown in Figure 14. The pipeline delay through the real processing leg (upper leg) is 14 CLK's and the delay through the imaginary processing leg (lower leg) is 47 CLK's. The complex samples output through AOUT0-15 and BOUT0-15 are present for 2 CLK's since the quadrature streams have been decimated by two in the filter processor.



THE SAMPLE DESIGNATED BY THE 0° AND 180° LABELS ARE MIXED WITH THE RESPECTIVE COSINE TERMS ON THE UPPER PROCESSING LEG, AND THE OTHER SAMPLES, THOSE LABELED BY 90° AND 270°, ARE MIXED WITH THE RESPECTIVE SINE TERMS ON THE LOWER LEG.

FIGURE 14. DATA SYNCHRONIZATION TO 0° PHASE OF QUADRATURE LO

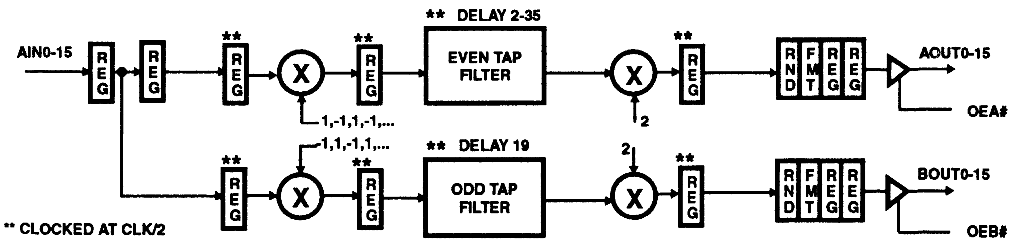


FIGURE 13A. DATA FLOW DIAGRAM FOR DOWN CONVERT AND DECIMATE MODE (INT/EXT# = 1)

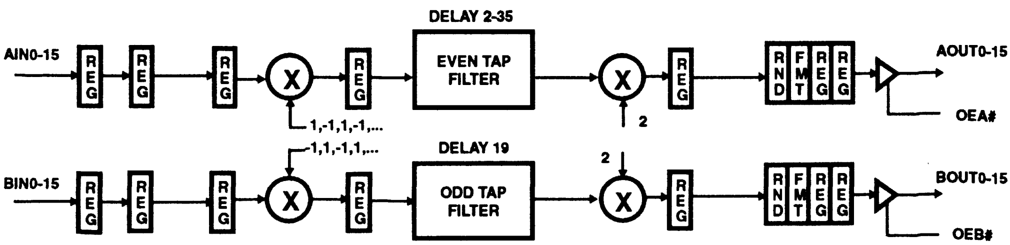
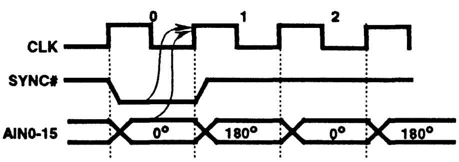


FIGURE 13B. DATA FLOW DIAGRAM FOR DOWN CONVERT AND DECIMATE MODE (INT/EXT# = 0)

If external multiplexing is selected (INT/EXT# = 0), a demultiplex function is required off chip to break the input data stream into even and odd samples for input through AIN0-15 and BIN0-15. In this mode, the real and imaginary processing legs run at the input clock rate which allows the device to perform the down convert and decimate function on real signals sampled at up to twice the maximum speed grade of the device (104 MSPS). With external multiplexing, the minimum pipeline delay through the upper processing leg is 9 CLK's and the pipeline delay through the lower processing leg is 26 CLK's as shown in Figure 13B. To synchronize the even samples input through AIN0-15 with the zero degree cosine term of the quadrature LO, SYNC# should be asserted on the same clock that the target sample is present at the input of the part as shown in Figure 15. NOTE: for proper operation, the samples demultiplexed to the AIN0-15 input must precede those input to the BIN0-15 input in sample order. For example, given a data sequence x0,x1,x2,and x3, the demultiplex function would route x0 and x2 to AIN0-15 and x1 and x3 to BIN0-15.



THE 0° AND 180° LABELS INDICATE THE PHASE ALIGNMENT OF THE SAMPLES INPUT THROUGH AIN0-15 WITH THE COSINE TERM OF THE QUADRATURE DOWN CONVERT LO.

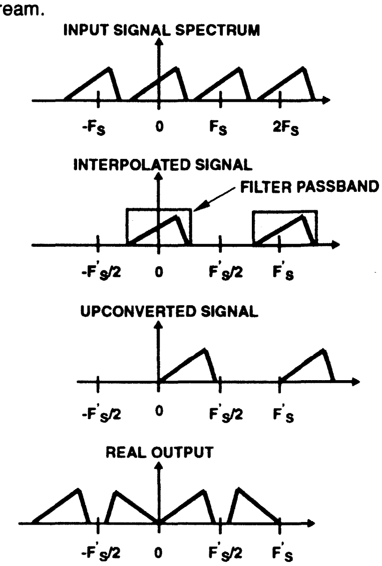
FIGURE 15. DATA SYNCHRONIZATION WITH PHASE OF DOWN CONVERT LO

Quadrature to Real Conversion Mode (MODE1-0 = 10)

The Quadrature to Real Conversion mode is used to construct a real output from a quadrature input. To accomplish this, the Halfband Filter Processor interpolates the quadrature components of the complex input signal by a factor of two. Next, the Quadrature Up-Convert Processor spectrally shifts the signal by $F_S/4$ and derives the real output as described in the $F_S/4$ Quadrature Up-Convert Processor Section. The direction of the spectral shift is controlled via the USB/LSB# input and is used to designate the frequency content of the complex input as either the upper or lower sideband of the resulting real output signal. A spectral representation of quadrature to real conversion is shown in Figure 16 for USB/LSB# = 1. NOTE: the $F_S/4$ Up-Convert Processor uses quadrature mix factors scaled by two to compensate for the attenuation introduced by the interpolation process.

The Quadrature to Real Conversion mode is most easily understood by first considering an implementation using a 7 tap transversal filter as shown in Figure 17. By examining the combination of interpolation, filtering, and up conversion it is seen that a particular output is only dependent on the sum-of-products for the even indexed samples and coefficientsor the sum-of-products for the odd indexed samples and coefficients. This computational partitioning allows the dual interpolation filters required in this m ode to be realized using the same poly-phase filter structure used in the other modes.

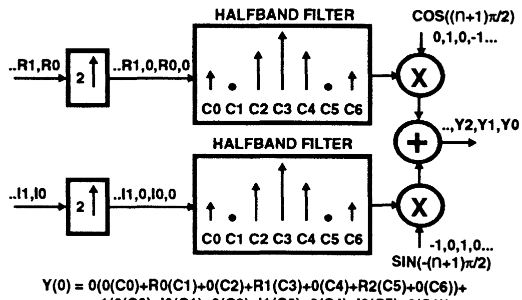
A functional block diagram of the polyphase implementation for Quadrature to Real Conversion mode is shown in Figure 18. In this implementation, the real and imaginary components of a complex input stream drive the even and odd tap filters. The output of each filter is then modulated by the non-zero mix factors and multiplexed into a single real output stream.



F_S = INPUT SAMPLE RATE
F'_S = INTERPOLATED SAMPLE RATE, $2F_S$

FIGURE 16. QUADRATURE TO REAL CONVERSION

As in the other modes, the operation of the HSP43216 in Quadrature to real Conversion mode is analogous to that of the polyphase solution described above. The data flow diagrams for this particular mode are shown in Figures 19A and 19B.



Y(0) = 0(0(C0)+R0(C1)+0(C2)+R1(C3)+0(C4)+R2(C5)+0(C6))+
-1(0(C0)+I0(C1)+0(C2)+I1(C3)+0(C4)+I2(C5)+0(C6))

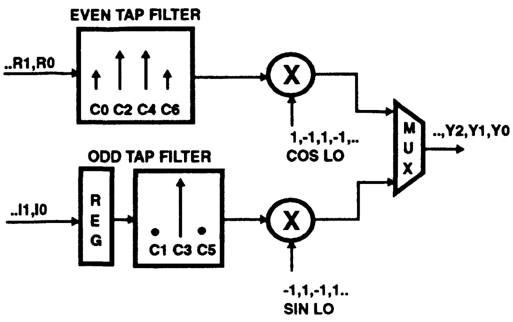
Y(1) = 1(R0(C0)+0(C1)+R1(C2)+0(C3)+R2(C4)+0(C5)+R3(C6))+
0(I0(C0)+0(C1)+I1(C2)+0(C3)+I2(C4)+0(C5)+I3(C6))

Y(2) = 0(0(C0)+R1(C1)+0(C2)+R2(C3)+0(C4)+R3(C5)+0(C6))+
1(0(C0)+I1(C1)+0(C2)+I2(C3)+0(C4)+I3(C5)+0(C6))

Y(3) = -1(R1(C0)+0(C1)+R2(C2)+0(C3)+R3(C4)+0(C5)+R4(C6))+
0(I1(C0)+0(C1)+I2(C2)+0(C3)+I3(C4)+0(C5)+I4(C6))

⋮

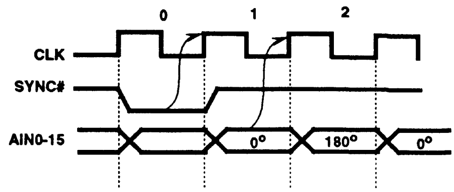
FIGURE 17. QUADRATURE TO REAL CONVERTER USING TRANSVERSAL FILTERS



Y(0) = -1(I0(C1)+I1(C3))+I2(C5))
Y(1) = 1(R0(C0)+R1(C2)+R2(C4))+R3(C6))
Y(2) = 1(I1(C1)+I2(C3)+I3(C5))
Y(3) = -1(R1(C0)+R2(C2)+R3(C4)+R4(C6))

FIGURE 18. POLYPHASE IMPLEMENTATION OF QUADRATURE TO REAL CONVERTER

If Internal Multiplexing is specified (INT/EXT# = 1), the real and imaginary components of the quadrature input are fed through AIN0-15 and BIN0-15 and processed on the upper and lower legs respectively (see Figure 19A). Each component of the complex input is interpolated, mixed with the non-zero sine and cosine terms of the quadrature LO, and multiplexed together into a real output sample stream through AOUT0-15. Prior to the output multiplexer, the upper and lower processing legs each run at the input data rate of CLK/2 as indicated by the "**" marking the various registers and processing elements in Figure 19A. The complex input sample stream may be synchronized with the zero degree phase of the up converters quadrature LO by asserting the SYNC# control input one cycle prior to the targeted data sample as shown in Figure 20. This ensures that the real sample input on the upper processing leg will be mixed with the zero degree cosine term. The minimum pipeline delay through the real processing leg (upper leg) is 15 CLK's and the delay through the imaginary processing leg (lower leg) is 48 CLK's.



THE 0° LABEL INDICATES THE SAMPLE WHICH WILL BE MIXED WITH THE 0° COSINE TERM OF THE QUADRATURE UP-CONVERT LO.

FIGURE 20. DATA SYNCHRONIZATION WITH PROCESSING LEGS (INT/EXT# = 1)

If external multiplexing is selected (INT/EXT# = 0), output from the upper and lower processing legs exit through AOUT0-15 and BOUT0-15 for multiplexing into a single data stream off chip (see Figure 19B).This allows the processing legs to run at the maximum CLK rate which coincides with an interpolated output data rate of up to 104MSPS. NOTE: the output on BOUT0-15 precedes that on AOUT0-15 in sample order. This requires a multiplexing scenario which selects BOUT0-15 then AOUT0-15 on each CLK of the HSP43216. With external multiplexing, the minimum pipeline delay through the upper processing leg is 9 CLK's and the pipeline delay through the lower processing leg is 26 CLK's as shown in Figure 19B. The SYNC# control input is used as described in the preceding paragraph.

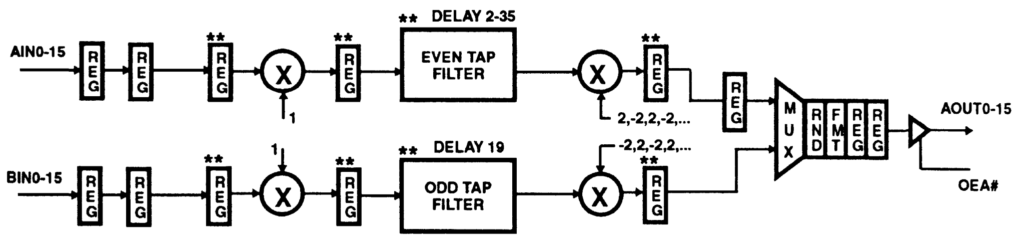


FIGURE 19A. DATA FLOW DIAGRAM FOR QUADRATURE TO REAL CONVERSION MODE (INT/EXT# = 1)

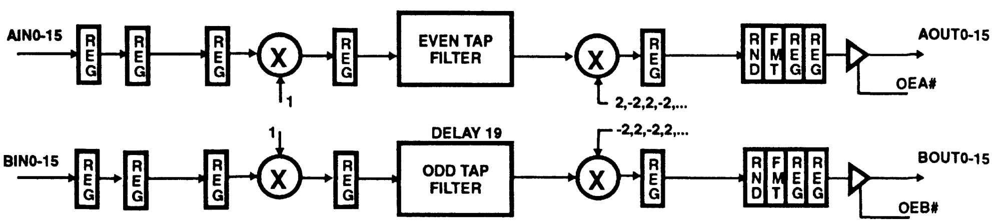


FIGURE 19B. DATA FLOW DIAGRAM FOR QUADRATURE TO REAL CONVERSION MODE (INT/EXT# = 0)

Absolute Maximum Ratings

Supply Voltage .... +7.0V
Input, Output or I/O Voltage .... GND-0.5V to VCC+0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... 150°C (PLCC),175°C(PGA)
Lead Temperature (Soldering 10s) .... +300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
PGA Package	37.2°C/W	6°C/W
PLCC Package	23.0°C/W	9°C/W

Maximum Package Power Dissipation at 70°C
PGA Package 2.8W
PLCC Package 3.5W
Gate Count .... 35469 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.75V to +5.25V
Operating Temperature Range .... 0°C to +70°C

DC Electrical Specifications (V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Power Supply Current	I_{CCOP}	-	468	mA	V_{CC} = Max, CLK Frequency 52MHz INT/EXT# = '1', Notes 1, 3
		-	572	mA	V_{CC} = Max, CLK Frequency 52MHz INT/EXT# = '0', Notes 2, 3
Standby Power Supply Current	I_{CCSB}	-	500	μA	V_{CC} = Max, Outputs Not Loaded
Input Leakage Current	I_I	-10	10	μA	V_{CC} = Max, Input = 0V or V_{CC}
Output Leakage Current	I_O	-10	10	V	V_{CC} = Max, Input = 0V or V_{CC}
Clock Input High	V_{IHC}	3.0	-	V	V_{CC} = Max
Clock Input Low	V_{ILC}	-	0.8	V	V_{CC} = Min
Logical One Input Voltage	V_{IH}	2.0	-	V	V_{CC} = Max
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = Min
Logical One Output Voltage	V_{OH}	2.6	-	V	I_{OH} = -3mA, V_{CC} = Min
Logical Zero Output Voltage	V_{OL}	-	0.4	V	I_{OL} = 5mA, V_{CC} = Min
Input Capacitance	C_{IN}	-	12	pF	CLK Frequency 1MHz, All measurements referenced to GND. T_A = +25°C, Note 4
Output Capacitance	C_{OUT}	-	12	pF	

NOTES:

1. Power supply current is proportional to frequency. Typical rating is 9mA/MHz when Internal Multiplexing is selected, INT/EXT# = 1.
2. Power supply current is proportional to frequency. Typical rating is 11mA/MHz when External Multiplexing is selected, INT/EXT# = 0.
3. Output load per test circuit and C_L = 40pF.
4. Not tested, but characterized at initial design and at major process/design changes.
5. Maximum junction temperature must be considered when operating part at high clock frequencies.

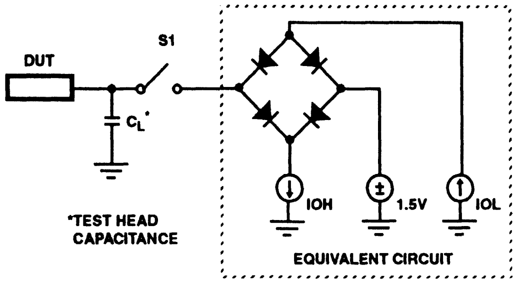
AC Electrical Specifications (Note 1)

PARAMETER	SYMBOL	52MHz MIN	52MHz MAX	UNITS	TEST CONDITIONS
CLK Period	T_{CP}	19	-	ns	-
CLK High	T_{CH}	7	-	ns	-
CLK Low	T_{CL}	7	-	ns	-
Setup Time AIN0-15, BIN0-15 to CLK	T_{DS}	7	-	ns	-
Hold Time AIN0-15, BIN0-15from CLK	T_{DH}	0	-	ns	-
MODE0-1, RND0-2, INT/EXT#,SYN-C#,USB/LSB# Setup Time to CLK	T_{RS}	7	-	ns	-
MODE0-1, RND0-2, INT/EXT#,SYN-C#,USB/LSB# Hold Time to CLK	T_{RH}	0	-	ns	-
CLK to AOUT0-15, BOUT0-15 Delay	T_{DO}	-	9	ns	
Output Enable Time	T_{OE}	-	9	ns	-
Output Disable Time	T_{OD}	-	9	ns	Note 2
Output rise, fall time	T_{RF}	-	3	ns	Note 2

NOTES:

1. AC tests performed with C_L = 40pF, I_{OL} = 5mA, and I_{OH} = -3mA. Input reference level for CLK is 2.0V, all other inputs 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V.
2. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.

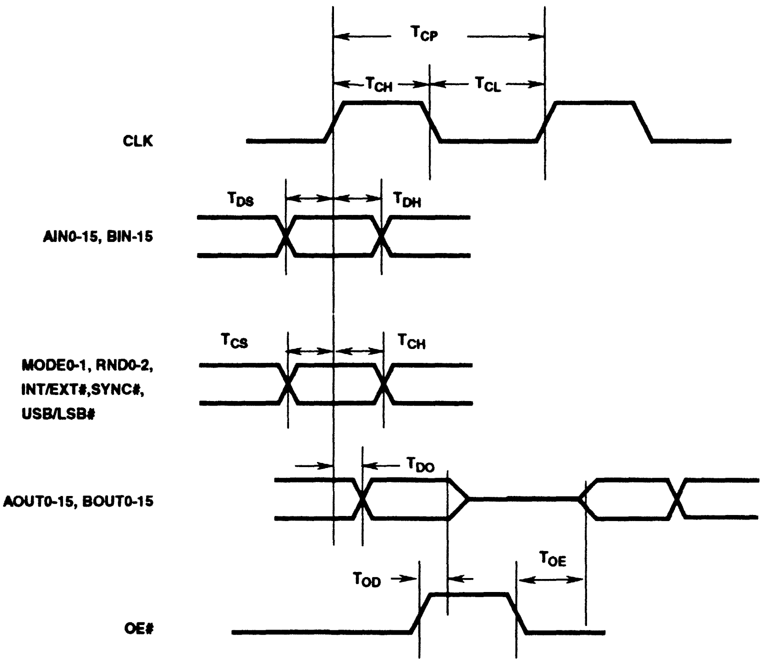
AC Test Load Circuit



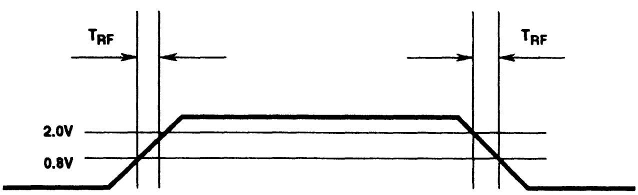
SWITCH S1 OPEN FOR I_{CCSB} AND I_{CCOP}

Waveforms

TIMING RELATIVE TO CLK



OUTPUT RISE AND FALL TIMES



HSP43220

January 1994

Decimating Digital Filter

Features

- **Single Chip Narrow Band Filter with up to 96dB Attenuation**
- **DC to 33MHz Clock Rate**
- **16-Bit 2's Complement Input**
- **20-Bit Coefficients in FIR**
- **24-Bit Extended Precision Output**
- **Programmable Decimation up to a Maximum of 16,384**
- **Standard 16-Bit Microprocessor Interface**
- **Filter Design Software Available DECI•MATE™**

Applications

- **Very Narrow Band Filters**
- **Zoom Spectral Analysis**
- **Channelized Receivers**
- **Large Sample Rate Converter**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43220VC-15	0°C to +70°C	100 Lead MQFP
HSP43220VC-25	0°C to +70°C	100 Lead MQFP
HSP43220VC-33	0°C to +70°C	100 Lead MQFP
HSP43220JC-15	0°C to +70°C	84 Lead PLCC
HSP43220JC-25	0°C to +70°C	84 Lead PLCC
HSP43220JC-33	0°C to +70°C	84 Lead PLCC
HSP43220GC-15	0°C to +70°C	84 Lead PGA
HSP43220GC-25	0°C to +70°C	84 Lead PGA
HSP43220GC-33	0°C to +70°C	84 Lead PGA
HSP43220TM-15	-55°C to +125°C	84 Lead TAB
HSP43220TM-25	-55°C to +125°C	84 Lead TAB

Description

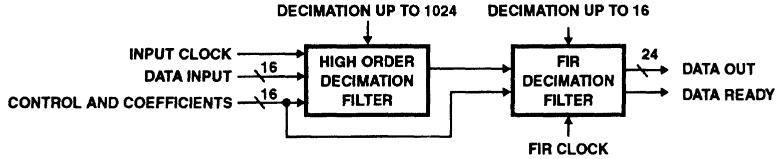
The HSP43220 Decimating Digital Filter is a linear phase low pass decimation filter which is optimized for filtering narrow band signals in a broad spectrum of a signal processing applications. The HSP43220 offers a single chip solution to signal processing application which have historically required several boards of IC's. This reduction in component count results in faster development times as well as reduction of hardware costs.

The HSP43220 is implemented as a two stage filter structure. As seen in the block diagram, the first stage is a high order decimation filter (HDF) which utilizes an efficient decimation (sample rate reduction) technique to obtain decimation up to 1024 through a coarse low-pass filtering process. The HDF provides up to 96dB aliasing rejection in the signal pass band. The second stage consists of a finite impulse response (FIR) decimation filter structured as a transversal FIR filter with up to 512 symmetric taps which can implement filters with sharp transition regions. The FIR can perform further decimation by up to 16 if required while preserving the 96dB aliasing attenuation obtained by the HDF. The combined total decimation capability is 16,384.

The HSP43220 accepts 16-bit parallel data in 2's complement format at sampling rates up to 33MSPS. It provides a 16-bit microprocessor compatible interface to simplify the task of programming and three-state outputs to allow the connection of several IC's to a common bus. The HSP43220 also provides the capability to bypass either the HDF or the FIR for additional flexibility.

The pinout TAB package can be obtained by referring to the Metallization Mask Layout of the HSP43220/883 data sheet.

Block Diagram



DECI•MATE™ is a registered trademark of Harris Corporation.
IBM PC™, XT™, AT™, PS/2™ are registered trademarks of International Business Machines, Inc.

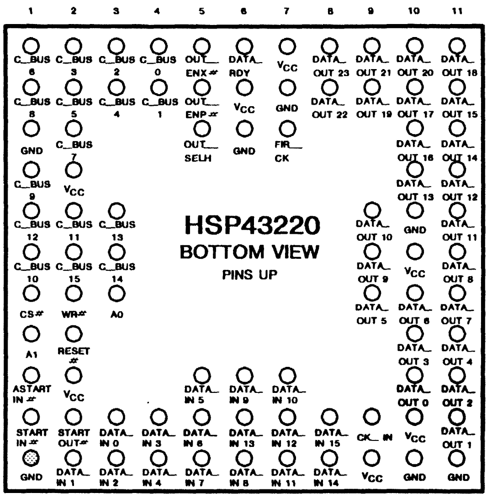
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2486.4**

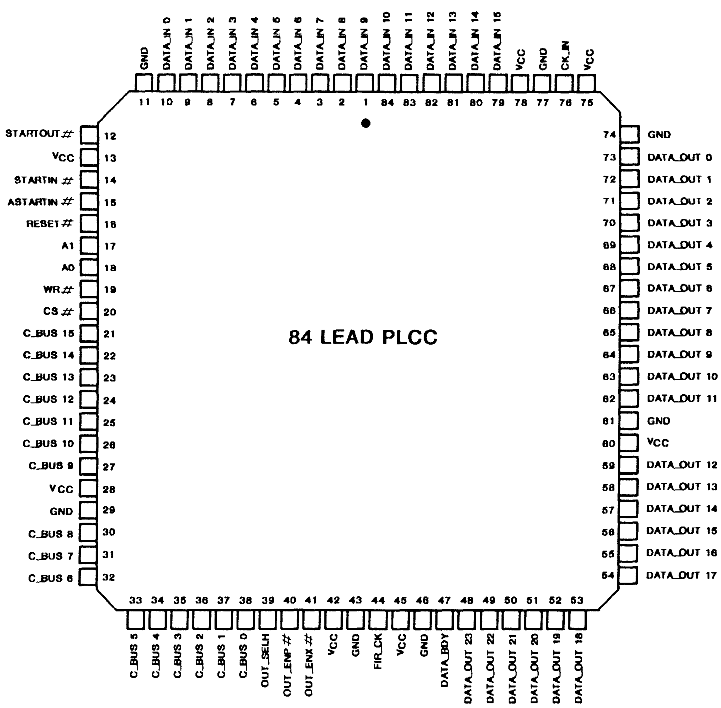
Package Pinouts

84 PIN GRID ARRAY (PGA)

	1	2	3	4	5	6	7	8	9	10	11
A	GND	DATA_IN 1	DATA_IN 2	DATA_IN 4	DATA_IN 7	DATA_IN 8	DATA_IN 11	DATA_IN 14	VCC	GND	GND
B	START IN#	START OUT#	DATA_IN 0	DATA_IN 3	DATA_IN 6	DATA_IN 13	DATA_IN 12	DATA_IN 15	CK_IN	VCC	DATA_OUT 1
C	ASTART IN#	VCC			DATA_IN 5	DATA_IN 9	DATA_IN 10			DATA_OUT 0	DATA_OUT 2
D	A1	RESET#								DATA_OUT 3	DATA_OUT 4
E	CS#	WR#	A0						DATA_OUT 5	DATA_OUT 6	DATA_OUT 7
F	C_BUS 10	C_BUS 15	C_BUS 14		HSP43220 TOP VIEW PINS DOWN				DATA_OUT 9	VCC	DATA_OUT 8
G	C_BUS 12	C_BUS 11	C_BUS 13						DATA_OUT 10	GND	DATA_OUT 11
H	C_BUS 9	VCC								DATA_OUT 13	DATA_OUT 12
J	GND	C_BUS 7			OUT_SELH	GND	FIR_CK			DATA_OUT 16	DATA_OUT 14
K	C_BUS 8	C_BUS 5	C_BUS 4	C_BUS 1	OUT_ENP#	VCC	GND	DATA_OUT 22	DATA_OUT 19	DATA_OUT 17	DATA_OUT 15
L	C_BUS 6	C_BUS 3	C_BUS 2	C_BUS 0	OUT_ENX#	DATA_RDY	VCC	DATA_OUT 23	DATA_OUT 21	DATA_OUT 20	DATA_OUT 18



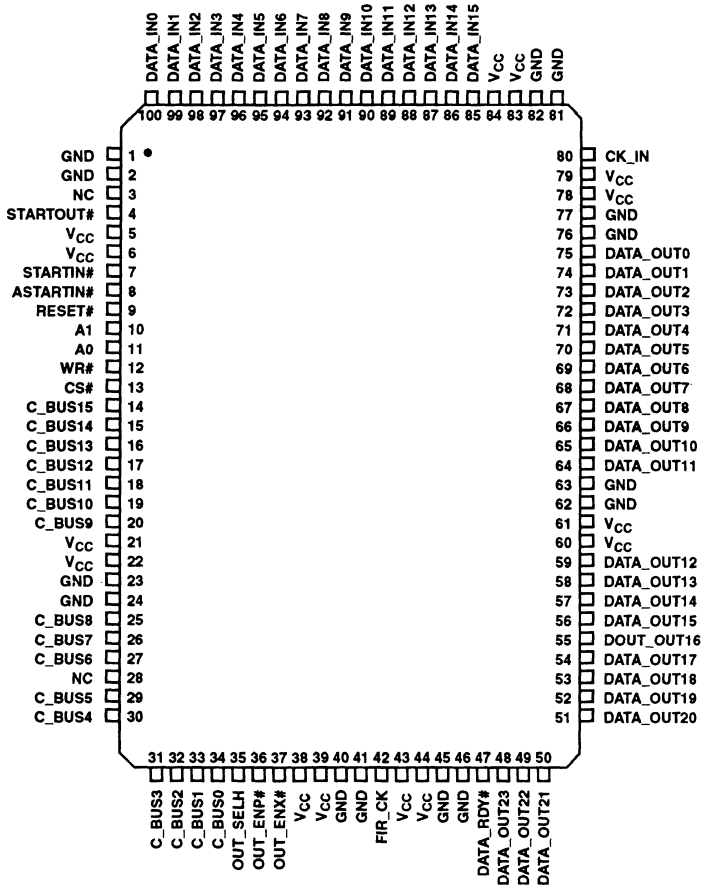
84 PLASTIC LEADED CHIP CARRIER (PLCC)



Pinouts (Continued)

100 LEAD MQFP

TOP VIEW



Pin Description

NAME	PLCC PIN	TYPE	DESCRIPTION
V_{CC}	13, 28, 42, 45, 60, 75, 78		The +5V power supply pins.
GND	11, 29, 43, 46, 61, 74, 77		The device ground.
CK_IN	76	I	Input sample clock. Operations in the HDF are synchronous with the rising edge of this clock signal. The maximum clock frequency is 33MHz. CK_IN is synchronous with FIR_CK and thus the two clocks may be tied together if required, or CK_IN can be divided down from FIR_CK. CK_IN is a CMOS level signal.
FIR_CK	44	I	Input clock for the FIR filter. This clock must be synchronous with CK_IN. Operations in the FIR are synchronous with the rising edge of this clock signal. The maximum clock frequency is 33 MHz. FIR_CK is a CMOS level signal.
DATA_IN0-15	1-10, 79-84	I	Input Data bus. This bus is used to provide the 16-bit input data to the HSP43220. The data must be provided in a synchronous fashion, and is latched on the rising edge of the CK_IN signal. The data bus is in 2's complement fractional format.
C_BUS0-15	21-27, 30-38	I	Control Input bus. This input bus is used to load all the filter parameters. The pins WR#, CS# and A0 , A1 are used to select the destination of the data on the Control bus and write the Control bus data into the appropriate register as selected by A0 and A1.
DATA_OUT 0-23	48-59, 62-73	O	Output Data bus. This 24-Bit output port is used to provide the filtered result in 2's complement format. The upper 8 bits of the output, DATA_OUT16-23 will provide extension or growth bits depending on the state of OUT_SELH and whether the FIR has been put in bypass mode. Output bits DATA_OUT0-15 will provide bits 2^0 through 2^{-15} when the FIR is not bypassed and will provide the bits 2^{-16} through 2^{-31} when the FIR is in bypass mode.
DATA_RDY	47	O	An active high output strobe that is synchronous with FIR_CK that indicates that the result of the just completed FIR cycle is available on the data bus.
RESET#	16	I	RESET# is an asynchronous signal which requires that the input clocks CK_IN and FIR_CK are active when RESET# is asserted. RESET# disables the clock divider and clears all of the internal data registers in the HDF. The FIR filter data path is not initialized. The control register bits that are cleared are F_BYP, H_STAGES, and H_DRATE. The F_DIS bit is set. In order to guarantee consistent operation of the part, the user must reset the DDF after power up.
WR#	19	I	Write strobe. WR# is used for loading the internal registers of the HSP43220. When CS# and WR# are asserted, the rising edge of WR# will latch the C_BUS0-15 data into the register specified by A0 and A1.
CS#	20	I	Chip Select. The Chip Select input enables loading of the internal registers. When CS# and WR# are low, the A0 and A1 address lines are decoded to determine the destination of the data on C_BUS0-15. The rising edge of WR# then loads the appropriate register as specified by A0 and A1.
A0, A1	18, 17	I	Control Register Address. These lines are decoded to determine which control register is the destination for the data on C_BUS0-15. Register loading is controlled by the A0 and A1, WR# and CS# inputs.
ASTARTIN#	15	I	ASTARTIN# is an asynchronous signal which is sampled on the rising edge of CK_IN. It is used to put the DDF in operational mode. ASTARTIN# is internally synchronized to CK_IN and is used to generate STARTOUT#.
STARTOUT#	12	O	STARTOUT# is a pulse generated from the internally synchronized version of ASTARTIN#. It is provided as an output for use in multi-chip configurations to synchronously start multiple HSP43220's. The width of STARTOUT# is equal to the period of CK_IN.
STARTIN#	14	I	STARTIN# is a synchronous input. A high to low transition of this signal is required to start the part. STARTIN# is sampled on the rising edge of CK_IN. This synchronous signal can be used to start single or multiple HSP43220's.
OUT_SELH	39	I	Output Select. The OUT_SELH input controls which bits are provided at output pins DATA_OUT16-23. A HIGH on this control line selects bits 2^8 through 2^1 from the accumulator output. A LOW on this control line selects bits 2^{-16} through 2^{-23} from the accumulator output. Processing is not interrupted by this pin.
OUT_ENP#	40	I	Output Enable. The OUT_ENP# input controls the state of the lower 16 bits of the output data bus, DATA_OUT0-15. A LOW on this control line enables the lower 16 bits of the output bus. When OUT_ENP# is HIGH , the output drivers are in the high impedance state. Processing is not interrupted by this pin.
OUT_ENX#	41	I	Output Enable. The OUT_ENX# input controls the state of the upper 8 bits of the output data bus, DATA_OUT16-23. A LOW on this control line enables the upper 8 bits of the output bus. When OUT_ENX# is HIGH, the output drivers are in the high impedance state. Processing is not interrupted by this pin.

The HDF

The first filter section is called the High Order Decimation Filter (HDF) and is optimized to perform decimation by large factors. It implements a low pass filter using only adders and delay elements instead of a large number of multiplier/accumulators that would be required using a standard FIR filter.

The HDF is divided into 4 sections: the HDF filter section, the clock divider, the control register logic and the start logic (Figure 1).

Data Shifter

After being latched into the Input Register the data enters the Data Shifter. The data is positioned at the output of the shifter to prevent errors due to overflow occurring at the output of the HDF. The number of bits to shift is controlled by H_GROWTH.

Integrator Section

The data from the shifter goes to the Integrator section. This is a cascade of 5 integrator (or accumulator) stages, which implement a low pass filter. Each accumulator is implemented as an adder followed by a register in the feed forward path. The integrator is clocked by the sample clock, CK_IN as shown in Figure 2. The bit width of each integrator stage goes from 66 bits at the first integrator down to 26 bits at the output of the fifth integrator. Bit truncation is performed at each integrator stage because the data in the integrator stages is being accumulated and thus is growing, therefore the lower bits become insignificant, and can be truncated without losing significant data.

There are three signals that control the integrator section; they are H_STAGES, H_BYP and RESET#. In Figure 2 these control signals have been decoded and are labelled INT_EN1 - INT_EN5. The order of the filter is loaded via the control bus and is called H_STAGES. H_STAGES is decoded to provide the enables for each integrator stage. When a given integrator stage is selected, the feedback path is enabled and the integrator accumulates the current data sample with the previous sum. The integrator section can be put in bypass mode by the H_BYP bit. When H_BYP or RESET# is asserted, the feedback paths in all integrator stages are cleared.

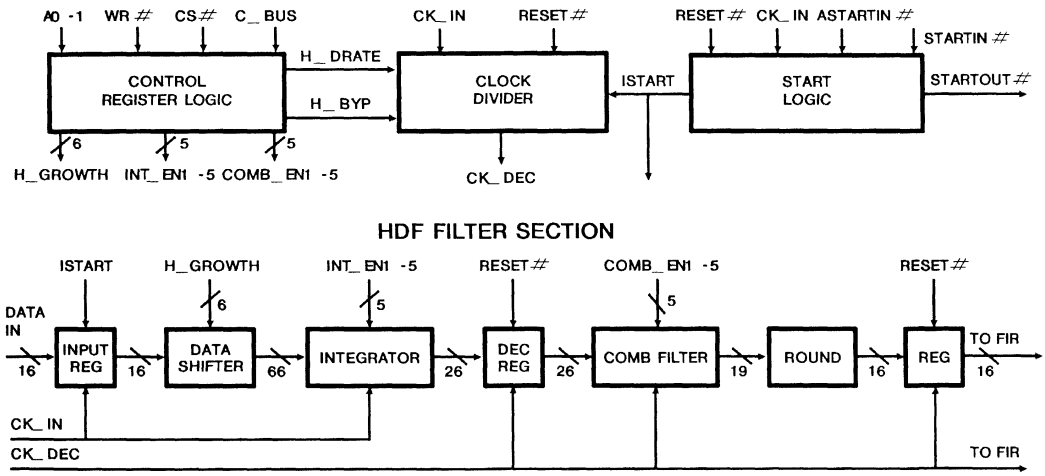


FIGURE 1. HIGH ORDER DECIMATION FILTER

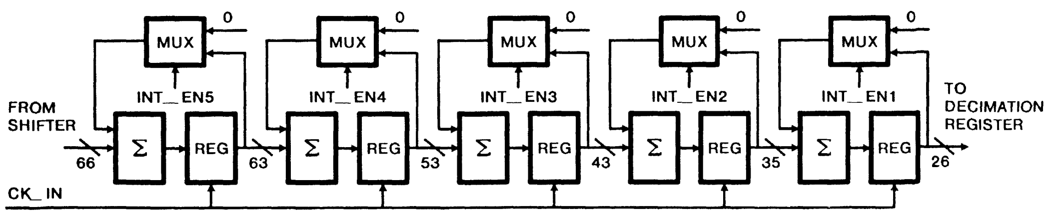


FIGURE 2. INTEGRATOR

Decimation Register

The output of the Integrator section is latched into the Decimation Register by CK_DEC. The output of the Decimation register is cleared when RESET# is asserted. The HDF decimation rate = H_DRATE +1, which is defined as Hdec for convenience.

Comb Filter Section

The output of the Decimation Register is passed to the Comb Filter Section. The Comb section consists of 5 cascaded Comb filters or differentiators. Each Comb filter section calculates the difference between the current and previous integrator output. Each Comb filter consists of a register which is clocked by CK_DEC, followed by an subtractor, where the subtractor calculates the difference between the input and output of the register. Bit truncations are done at each stage as shown in Figure 3. The first stage bit width is 26 bits and the output of the fifth stage is 19 bits.

There are three signals that control the Comb Filter; H_STAGES, H_BYP and RESET#. In Figure 3 these control signals are decoded as COMB_EN1 - COMB_EN5. The order of the Comb filter is controlled by H_STAGES, which is programmed over the control bus. H_BYP is used to put the comb section in bypass mode. RESET# causes the register output in each Comb stage to be cleared. The H_BYP and RESET# control pins, when asserted force the output of all registers to zero so data is passed through the subtractor unaltered. When the H_STAGES control bits enable a given stage the output of the register is subtracted from the input.

It is important to note that the Comb filter section has a speed limitation. The Input sampling rate divided by the decimation factor in the HDF (CK_IN/Hdec) should not exceed 4MHz. Violating this condition causes the output of the filter to be incorrect. When the HDF is put in bypass mode this limitation does not apply. Equation 1.0 describes the relationship between F_TAPS, F_DRATE, H_DRATE, CK_IN and FIR_CK.

Rounder

The filter accuracy is limited by the 16 bit data input. To maintain the maximum accuracy, the output of the comb is rounded to 16 bits.

The Rounder performs a symmetric round of the 19 bit output of the last Comb stage. Symmetric rounding is done to prevent the synthesis of a 0Hz spectral component by the rounding process and thus causing a reduction in spurious free dynamic range. Saturation logic is also provided to prevent roll over from the largest positive value to the most negative value after rounding. The output of the last comb filter stage in the HDF section has a 16 bit integer portion with a 3 bit fractional part in 2's complement format.

The rounding algorithm is as follows:

POSITIVE NUMBERS	
Fractional Portion Greater Than or Equal to 0.5	Round Up
Fractional Portion Less Than 0.5	Truncate

NEGATIVE NUMBERS	
Fractional Portion Less Than or Equal to 0.5	Round Up
Fractional Portion Greater Than 0.5	Truncate

The output of the rounder is latched into the HDF output register with CK_DEC. CK_DEC is generated by the Clock Divider section. The output of the register is cleared when RESET# is asserted.

Clock Divider and Control Logic

The clock divider divides CK_IN by the decimation factor Hdec to produce CK_DEC. CK_DEC clocks the Decimation Register, Comb Filter section, HDF output register. In the FIR filter CK_DEC is used to indicate that a new data sample is available for processing. The clock generator is cleared by RESET# and is not enabled until the DDF is started by an internal start signal (see Start Logic).

The Control Register Logic enables the updating of the Control registers which contain all of the filter parameter data. When WR# and CS# are asserted, the control register addressed by bits A0 and A1 is loaded with the data on the C_BUS.

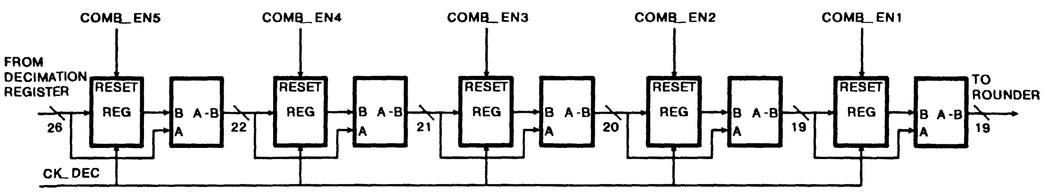


FIGURE 3. COMB FILTER

DDF Control Registers

F_Register (A1 = 0, A0 = 0)

F_OAD	F_BYP	F_ESYM	F_DRATE				F_TAPS								
FA0	FB0	ES0	D3	D2	D1	D0	T8	T7	T6	T5	T4	T3	T2	T1	T0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

F_TAPS

Bits T0-T8 are used to specify the number of FIR filter taps. The number entered is one less than the number of taps required. For example, to specify a 511 tap filter F_TAPS would be programmed to 510. The minimum number of FIR taps = 3 (F_TAPS=2).

F_DRATE

Bits D0-D3 are used to specify the amount of FIR decimation. The number entered is one less than the decimation required. For example, to specify decimation of 16, F_DRATE would be programmed to 15. For no FIR decimation, F_DRATE would be set equal to 0. FDRATE +1 is defined as Fdec.

F_ESYM

Bit ES0 is used to select the FIR symmetry. F_ESYM is set equal to one to select even symmetry and set equal to zero to select odd symmetry. When F_ESYM is one, data is added in the pre-adder; when it is zero, data is subtracted. Normally set to one.

F_BYP

Bit FB0 is used to select FIR bypass mode. FIR bypass mode is selected by setting F_BYP=1. When FIR bypass mode is selected, the FIR is internally set up for a 3 tap even symmetric filter, no decimation (F_DRATE=0) and F_0AD is set equal to one to zero one side of the preadder. In FIR bypass mode all FIR filter parameters, except F_CLA, are ignored, including the contents of the FIR coefficient RAM. In FIR bypass mode the output data is brought output on the lower 16 bits of the output bus DATA_OUT 0-15. To disable FIR bypass mode, F_BYP is set equal to zero. When F_BYP is returned to zero, the coefficients must be reloaded.

F_0AD

Bit FA0 is used to select the zero the preadder mode. This mode zeros one of the inputs to the pre-adder. Zero preadder mode is selected by setting F_0AD equal to one. This feature is useful when implementing arbitrary phase filters or can be used to verify the filter coefficients. To disable the Zero Preadder mode F_0AD is set equal to zero.

FIGURE 4.

DDF Control Registers (Continued)

FC_Register (A1 = 0, A0 = 1)

F_CF															
C19	C18	C17	C16	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4
X	X	X	X	X	X	X	X	X	X	X	X	C3	C2	C1	C0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

F_CF

Bits C0-C19 represent the coefficient data, where C19 is the MSB. Two writes are required to write each coefficient which is 2's complement fractional format. The first write loads C19 through C4; C3 through C0 are loaded on the second write cycle. As the coefficients are written into this register they are formatted into a 20 bit coefficient and written into the Coefficient RAM sequentially starting with address location zero. The coefficients must be loaded sequentially, with the center tap being the last coefficient to be loaded. See coefficient RAM, below.

FIGURE 5.

H_Register 1 (A1 = 1, A0 = 0)

RESERVED			F_DIS	F_CLA	H_BYP	H_DRATE									
			FD0	FC0	HB0	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

H_DRATE

Bits R0-R9 are used to select the amount of decimation in the HDF. The amount of decimation selected is programmed as the required decimation minus one; for instance to select decimation of 1024 H_DRATE is set equal to 1023. HDRATE +1 is defined as Hdec.

H_BYP

Bit HB0 is used to select HDF bypass mode. This mode is selected by setting H_BYP =1. When this mode is selected the input data passes through the HDF unfiltered. Internally H_STAGES and H_DRATE are both set to zero and H_GROWTH is set to 50. H_REGISTER 2 must be reloaded when H_BYP is returned to 0. To disable HDF bypass mode H_BYP=0. The relationship between CK_IN and FIR_CK in this and all other modes is defined by equation 1.0.

F_CLA

Bit FC0 is used to select the clear accumulator mode in the FIR. This mode is enabled by setting F_CLA=1 and is disabled by setting F_CLA=0. In normal operation this bit should be set equal to zero. This mode zeros the feedback path in the accumulator of the multiplier/accumualator (MAC). It also allows the multiplier output to be clocked off the chip by FIR_CK, thus DATA_RDY has no meaning in this mode. This mode can be used in conjunction with the F_0AD bit to read out the FIR coefficients from the coefficient RAM.

F_DIS

Bit FD0 is used to select the FIR disable mode. This feature enables the FIR parameters to be changed. This feature is selected by setting F_DIS=1. This mode terminates the current FIR cycle. While this feature is selected, the HDF contines to process data and write it into the FIR data RAM. When the FIR re-programming is completed, the FIR can be re-enabled either by clearing F_DIS, or by asserting one of the start inputs, which automatically clears F_DIS.

FIGURE 6

DDF Control Registers (Continued)

H_Register 2 (A1 = 1, A0 = 1)

RESERVED							H_GROWTH						H_STAGES		
							G5	G4	G3	G2	G1	G0	N2	N1	N0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

H_STAGES

Bits N0-N2 are used to select the number of stages or order of the HDF filter. The number that is programmed in is equal to the required number of stages. For a 5th order filter, H_STAGES would be set equal to 5.

H_GROWTH

Bits G0-G5 are used to select the proper amount of growth bits. H_GROWTH is calculated using the following equation:

H_GROWTH = 50 - CEILING {H_STAGES X log (Hdec)/ log(2)}

where the CEILING { } means use the next largest integer of the result of the value in brackets and log is the log to the base 10.

The value of H_GROWTH represents the position of the LSB on the output of the data shifter.

FIGURE 7

Start Logic

The Start Logic generates a start signal that is used internally to synchronously start the DDF. If ASTARTIN# is asserted (STARTIN# must be tied high) the Start Logic synchronizes it to CK_IN by double latching the signal and generating the signal STARTOUT#, which is shown in Figure 8. The STARTOUT# signal is then used to synchronously start other DDFs in a multi-chip configuration (the STARTOUT# signal of the first DDF would be tied to the STARTIN# of the second DDF). The NAND gate shown in Figure 8 then passes this synchronized signal to be used on chip to provide a synchronous start. Once started, the chip requires a RESET# to halt operation.

When STARTIN# is asserted (ASTARTIN# must be tied high) the NAND gate passes STARTIN# which is used to provide the internal start, ISTART, for the DDF. When RESET# is asserted the internal start signal is held inactive, thus it is necessary to assert either ASTARTIN# or STARTIN# in order to start the DDF. The timing of the first valid DATA_IN with respect to START_IN# is shown in the Timing Waveforms below.

In using ASTARTIN# or STARTIN# a high to low transition must be detected by the rising edge of CK_IN, therefore these signals must have been high for more than one CK_IN cycle and then taken low.

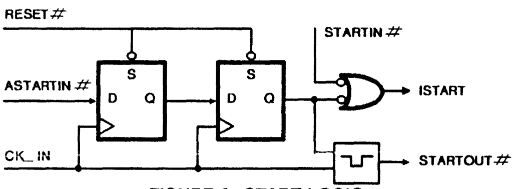


FIGURE 8. START LOGIC

The FIR Section

The second filter in the top level block diagram is a Finite Impulse Response (FIR) filter which performs the final shaping of the signal spectrum and suppresses the aliasing components in the transition band of the HDF. This enables the DDF to implement filters with narrow pass bands and sharp transition bands.

The FIR is implemented in a transversal structure using a single multiplier/accumulator (MAC) and RAM for storage of the data and filter coefficients as shown in Figure 9. The FIR can implement up to 512 symmetric taps and decimation up to 16.

The FIR is divided into 2 sections: the FIR filter section and the FIR control logic.

Coefficient RAM

The Coefficient RAM stores the coefficients for the current FIR filter being implemented. The coefficients are loaded into the Coefficient RAM over the control bus (C_BUS). The coefficients are written into the Coefficient RAM sequentially, starting at location zero. It is only necessary to write one half of the coefficients when symmetric filters are being implemented, where the last coefficient to be written in is the center tap.

The coefficients are loaded into address 01 in two writes. The first write loads the upper 16 bits of the 20 bit coefficient, C4 through C19. The second write loads the lower 4 bits of the coefficient, C0 through C3, where C19 is the MSB. The two 16 bit writes are then formatted into the 20 bit coefficient that is then loaded into the Coefficient RAM starting at RAM address location zero, where the coefficient at this location is the outer tap (or the first coefficient value).

To reload coefficients, the Coefficient RAM Address pointer must be reset to location zero so that the coefficients will be loaded in the order the FIR filter expects. There are two methods that can be used to reset the Coefficient RAM address pointer. The first is to assert RESET#, which automatically resets the pointer, but also clears the HDF and alters some of the control register bits. (RESET# does not change any of the coefficient values.) The second method is to set the F_DIS bit in control register H_ REGISTER1. This control bit allows any of the FIR control register bits to be re-programmed, but does not automatically modify any control registers. When the programming is completed, the FIR is re-started by clearing the F_DIS bit or by asserting one of the start inputs (ASTARTIN# or STARTIN#). The F_DIS bit allows the filter parameters to be changed more quickly and is thus the recommended reprogramming method.

Data RAM

The Data RAM stores the data needed for the filter calculation. The format of the data is:

$2^0.2^{-1}2^{-2}2^{-3}2^{-4}2^{-5}2^{-6}2^{-7}2^{-8}2^{-9}2^{-10}2^{-11}2^{-12}2^{-13}2^{-14}2^{-15}$

where the sign bit is in the 2^0 location.

The 16 bit output of the HDF Output Register is written into the Data Ram on the rising edge of CK_DEC.

RESET# initializes the write pointer to the data RAM. After a RESET# occurs, the output of the FIR will not be valid until the number of new data samples written to the Data RAM equals TAPS.

The filter always operates on the most current sample and the taps-1 previous samples. Thus if the F_DIS bit is set, data continues to be written into the data RAM coming from the HDF section. When the FIR is enabled again the filter will be operating on the most current data samples and thus another transient response will not occur.

The maximum throughput of the FIR filter is limited by the use of a single Multiplier/Accumulator (MAC). The data output from the HDF being clocked into the FIR filter by CK_DEC must not be at a rate that causes an erroneous result being calculated because data is being overwritten.

The equation shown below describes the relationship between, FIR_CK, CK_DEC, the number of taps that can be implemented in the FIR, the decimation rate in the HDF and the decimation rate in the FIR. (In the Design Considerations section of the OPERATIONAL SECTION there is a chart that shows the tradeoffs between these parameters.)

$$\text{FIR\_CK} \geq \frac{\text{CK\_IN}[(\text{TAPS}/2)+4+\text{Fdec}]}{\text{Hdec Fdec}} \qquad (1.0)$$

This equation expresses the minimum FIR_CK. The minimum FIR_CK is the smallest integer multiple of CK_IN that satisfies equation 1.0. In addition, the T_{SK} specification must be met (see A.C. Electrical Specifications). Fdec is the decimation rate in the FIR (Fdec = F_DRATE +1), where TAPS = the number of taps in the FIR for even length filters and equals the number of taps+1 for odd length filters.

Solving the above equation for the maximum number of taps:

$$TAPS = 2\left(\frac{FIR\_CK\ Hdec\ Fdec}{CK\_IN} - Fdec - 4\right) \qquad (2.0)$$

In using this equation, it must be kept in mind that CK_IN/ Hdec must be less than or equal to 4MHz (unless the HDF is in bypass mode in which case this limitation in the HDF does not apply). In the OPERATIONAL SECTION under the Design Considerations, there is a table that shows the trade-offs of these parameters. In addition, Harris provides a software package called DECI • MATE™ which designs the DDF filter from System specifications.

The registered outputs of the data RAM are added or subtracted in the 17 bit pre-adder. The F_0AD control bit allows zeros to be input into one side of the pre-adder. This provides the capability to implement non-symmetric filters.

The selection of adding the register outputs for an even symmetric filter or for subtracting the register outputs for odd symmetric filter is provided by the control bit F_ESYM, which is programmed over the control bus. When subtraction is selected, the new data is subtracted from the old data. The 17 bit output of the adder forms one input of the multiplier/accumulator.

A control bit F_CLA provides the capability to clear the feedback path in the accumulator such that multiplier output will not be accumulated, but will instead flow directly to the output register. The bit weightings of the data and coefficients as they are processed in the FIR is shown below.

Input Data (from HDF) $2^0.2^{-1} \ldots 2^{-15}$

Pre-adder Output $2^1 2^0.2^{-1} \ldots 2^{-15}$

Coefficient $2^0.2^{-1} \ldots 2^{-19}$

Accumulator $2^8 \ldots 2^0.2^1 \ldots 2^{-34}$

FIR Output

The 40 most significant bits of the accumulator are latched into the output register. The lower 3 bits are not brought to the output. The 40 bits out of the output register are selected to be output by a pair of multiplexers. This register is clocked by FIR_CK (see Figure 9).

There are two multiplexers that route 24 of the 40 output bits from the output register to the output pins. The first multiplexer selects the output register bits that will be routed to output pins DATA_OUT16-23 and the second multiplexer selects the output register bits that will be routed to output pins DATA_OUT0-15.

The multiplexers are controlled by the control signal F_BYP and the OUT_SELH pin. F_BYP and OUT_SELH both control the first multiplexer that selects the upper 8 bits of the output bus, DATA_OUT16-23. F_BYP controls the second multiplexer that selects the lower 16 bits of the output bus, DATA_OUT0-15. The output formatter is shown in detail in Figure 10.

FIR Control Logic

The DATA_RDY strobe indicates that new data is available on the output of the FIR. The rising edge of DATA_RDY can be used to load the output data into an external register or RAM.

Data Format

The DDF maintains 16 bits of accuracy in both the HDF and FIR filter stages. The data formats and bit weightings are shown in Figure 11.

Operational Section

Start Configurations

The scenario to put the DDF into operational mode is: reset the DDF by asserting the RESET# input, configure the DDF over the control bus, and apply a start signal, either by ASTARTIN# or STARTIN#. Until the DDF is put in operational mode with a start pulse, the DDF ignores all data inputs.

To use the asynchronous start, an asynchronous active low pulse is applied to the ASTARTIN# input. ASTARTIN# is internally synchronized to the sample clock, CK_IN, and generates STARTOUT#. This signal is also used internally when the asynchronous mode is selected. It puts the DDF in operational mode and allows the DDF to begin accepting data. When the ASTARTIN# input is being used, the STARTIN# input must be tied high to ensure proper operation.

To start the DDF synchronously, the STARTIN# is asserted with a active low pulse that has been externally synchronized to CK_IN. Internally the DDF then uses this start pulse to put the DDF in operate mode and start accepting data inputs. When STARTIN# is used to start the DDF the ASTARTIN# input must be tied high to prevent false starts.

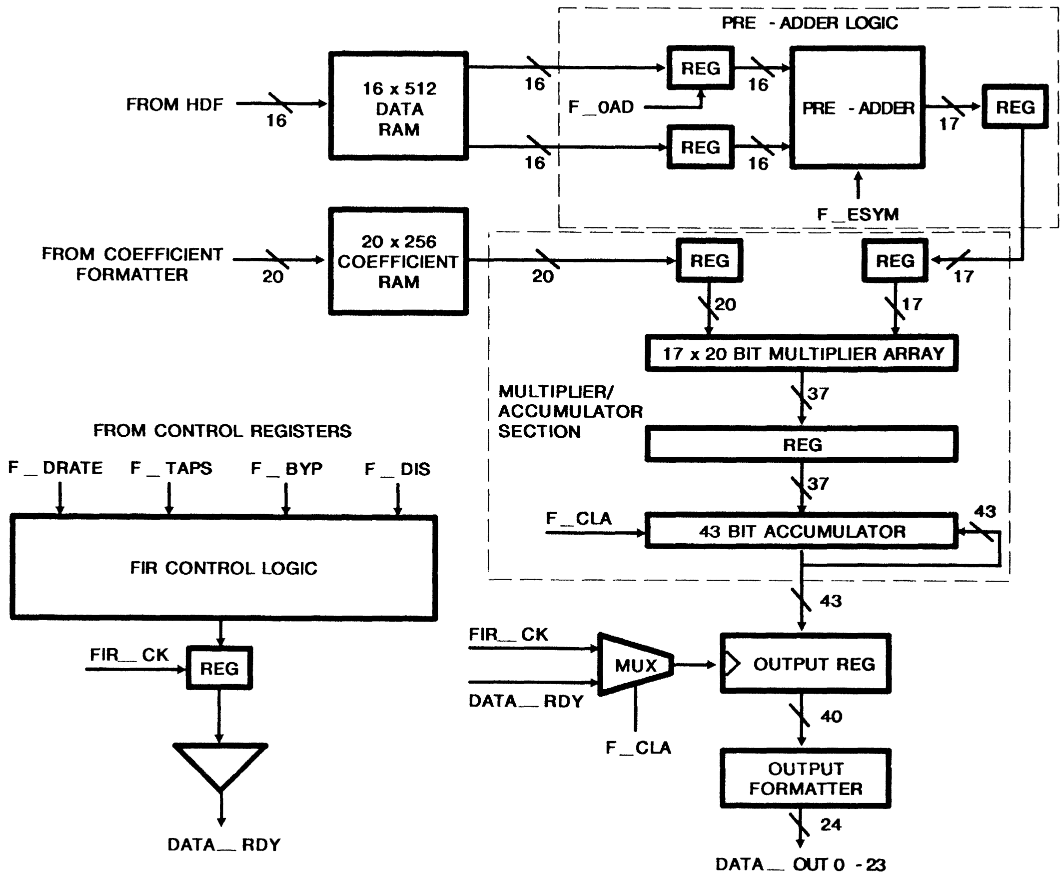


FIGURE 9. FIR FILTER

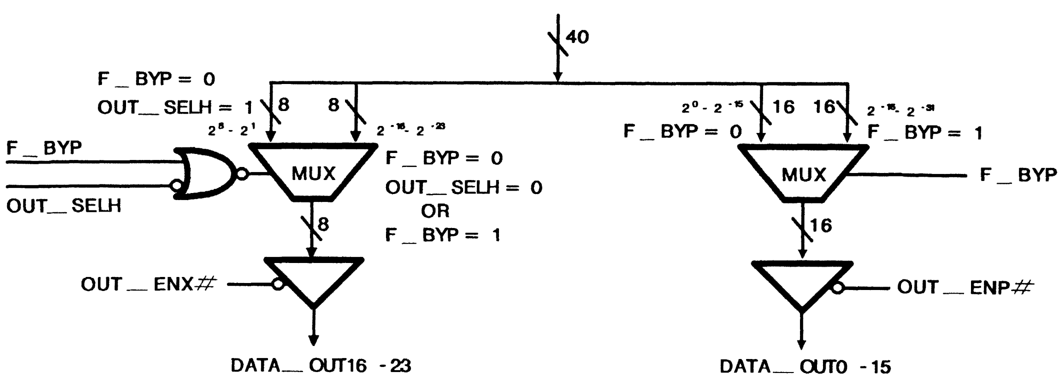


FIGURE 10. FIR OUTPUT FORMATTER

3

1D FILTERS

INPUT DATA FORMAT

Fractional Two's Complement Input

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

FIR COEFFICIENT FORMAT

Fractional Two's Complement Input

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4
-2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

3	2	1	0
2^{-16}	2^{-17}	2^{-18}	2^{-19}

OUTPUT DATA FORMAT

Fractional Two's Complement Output

FOR: OUT__SELH = 1
F__BYP = 0

23	22	21	20	19	18	17	16
-2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

FOR: OUT__SELH = 0
F__BYP = 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

23	22	21	20	19	18	17	16
2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

FOR: OUT__SELH = X
F__BYP = 1

23	22	21	20	19	18	17	16
2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}

FIGURE 11.

Multi-Chip Start Configurations

Since there are two methods to start up the DDF, there are also two configurations that can be used to start up multiple chips.

The first method is shown in Figure 12. The timing of the STARTOUT# circuitry starts the second DDF on the same clock as the first. If more DDF's are also to be started synchronously, STARTOUT# is connected to their STARTIN#'s.

The second method to start up DDF's in a multiple chip configuration is to use the synchronous start scenario.

The STARTIN# input is wired to all the chips in the chain, and is asserted by a active low synchronous pulse that has been externally synchronized to CK_IN. In this way all DDF's are synchronously started. The ASTARTIN# input on all the chips is tied high to prevent false starts. The STARTOUT# outputs are all left unconnected. This configuration is illustrated in Figure 13.

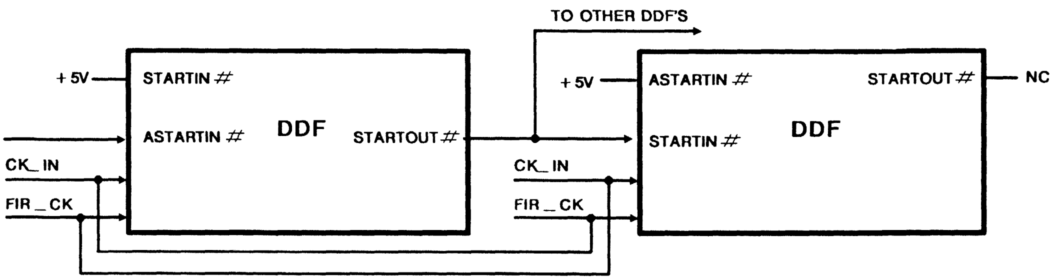


FIGURE 12. ASYNCHRONOUS START UP

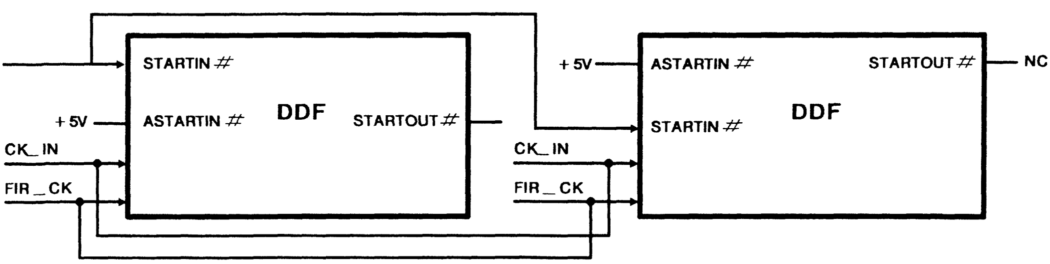


FIGURE 13. SYNCHRONOUS START UP

3

1D FILTERS

Chip Set Application

The HSP43220 is ideally suited for narrow band filtering in Communications, Instrumentation and Signal Processing applications. The HSP43220 provides a fully integrated solution to high order decimation filtering.

The combination of the HSP43220 and the HSP45116 (which is a NCOM Numerically Controlled Oscillator/ Modulator) provides a complete solution to digital receivers. The diagram in Figure 14 illustrates this concept.

The HSP45116 down converts the signal of interest to baseband, generating a real component and an imaginary component. A HSP43220 then performs low pass filtering and reduces the sampling rate of each of the signals.

The system scenario for the use of the DDF involves a narrow band signal that has been over-sampled. The signal is over-sampled in order to capture a wide frequency band containing many narrow band signals. The NCOM is "tuned" to the frequency of the signal of interest and performs a complex down conversion to baseband of this signal, which results in a complex signal centered at baseband. A pair of DDF's then low pass filters the NCOM output, extracting the signal of interest.

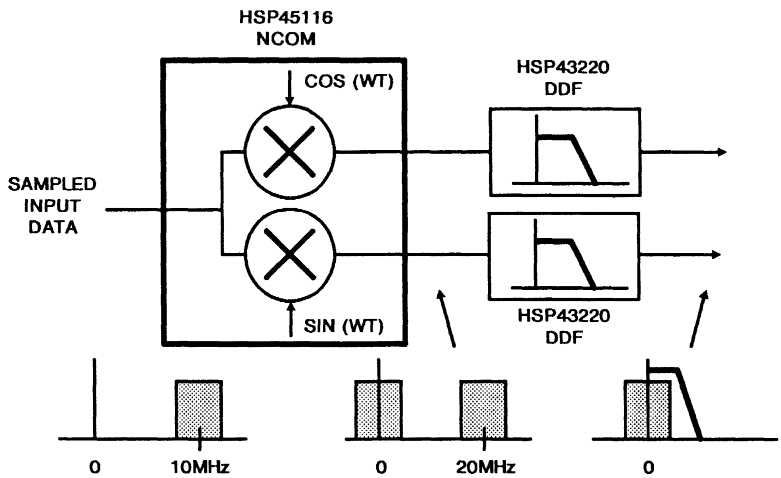


FIGURE 14. DIGITAL CHANNELIZER

Design Trade-Off Considerations

Equation 2.0 in the Functional Description section expresses the relationship between the number of TAPS which can be implemented in the FIR as a function of CK_IN, FIR_CK, Hdec, Fdec. Figure 15 provides a tradeoff of these parameters. For a given speed grade and the ratio of the clocks, and assuming minimum decimation in the HDF, the number of FIR taps that can be implemented is given in equation 2.0.

SPEED GRADE (MHz)	FIR_CK / CK_IN	MIN Hdec	TAPS				
			Fdec = 1	Fdec = 2	Fdec = 4	Fdec = 8	Fdec = 16
33	1	9	8	24	56	120	248
25.6	1	7	4	16	40	88	184
15	1	4	*	4	16	40	88
33	2	5	10	28	64	136	280
25.6	2	4	6	20	48	104	216
15	2	2	*	4	16	40	88
33	4	3	14	36	80	168	344
25.6	4	2	6	20	48	104	216
15	4	1	*	4	16	40	88
33	8	2	22	52	112	232	472
25.6	8	1	6	20	48	104	216
15	8	1	6	20	48	104	216

* Filter Not Realizable

FIGURE 15. DESIGN TRADE OFF FOR MINIMUM Hdec

DECI•MATE

Harris provides a development system which assists the design engineer to utilizing this filter. The DECI • MATE software package provides the user with both filter design and simulation environments for filter evaluation and design. These tools are integrated within one standard DSP CAD environment, The Athena Group's Monarch Professional DSP Software package.

The software package is designed specifically for the DDF. It provides all the filter design software for this proprietary architecture. It provides a user-friendly menu driven interface to allow the user to input system level filter requirements. It provides the frequency response curves and a data flow simulation of the specified filter design (Figure 16). It also creates all the information necessary to program the DDF, including a PROM file for programming the control registers.

This software package runs on an IBM™ PC™, XT™, AT™, PS/2™ computer or 100% compatible with the following configuration:

640K RAM
5.25" or 3.5" Floppy drive
hard disk
math co-processor
MS/PC-DOS 2.0 or higher
CGA, MCGA, EGA, VGA and
Hercules graphics adapters

For more information, see the description of DECI-MATE in the Development Tools Section of this databook.

```
                      HSP43220 DDF FILTER SPECIFICATION

Filter File        : vectors\example.DDF
Input Sample Rate:          33 MHz    Design Mode          :   AUTO
Output Rate        :       100 kHz    Generate Report      :   YES
Passband           :        20 kHz    Display Response     :   LOG
Transition Band    :       7.5 kHz    Save Freq Responses:     YES
Passband Atten     :       0.5 dB     Save FIR Response    :   YES
Stopband Atten     :        80 dB


FIR Type           :   PRECOMP



HDF Order          :           4   FIR Input Rate    :      300 kHz
HDF Decimation     :         110   FIR Clock (min)   :       33 MHz
HDF Scale Factor   :     0.54542   FIR Order         :      135
                                   FIR Decimation    :        3

                    (C) Harris Semiconductor 1990
```

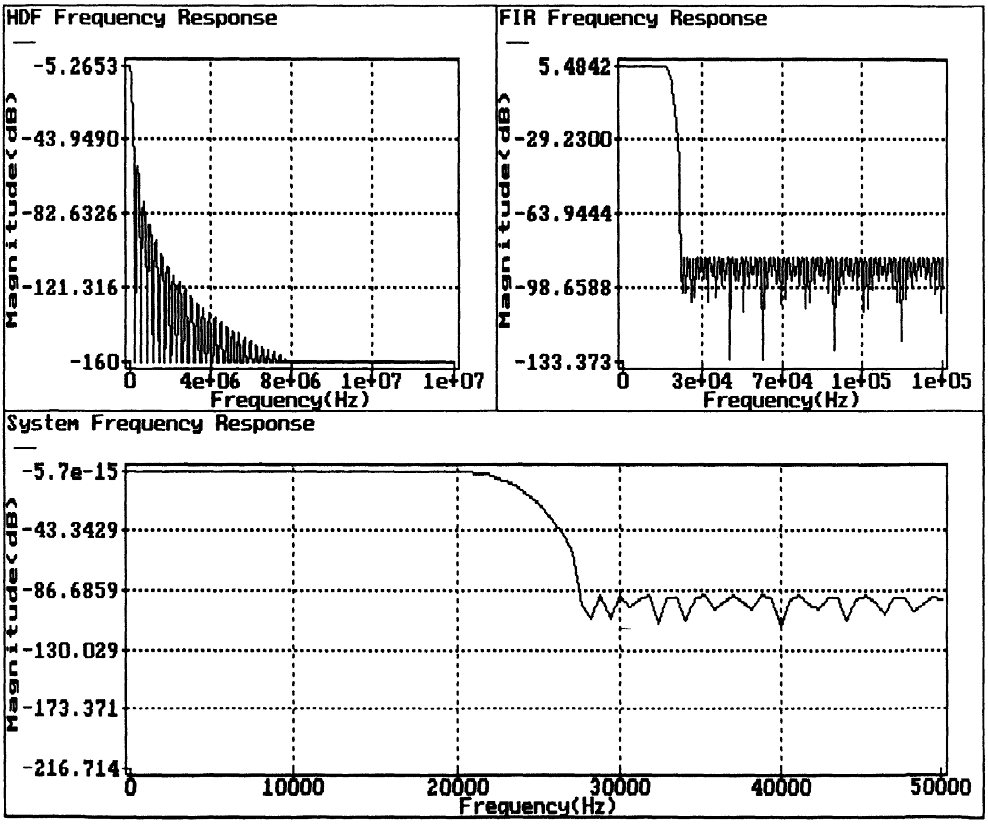


FIGURE 16. DECI•MATE DESIGN MODULE SCREENS

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output or I/O Voltage Applied ...... GND -0.5V to V_{CC} +0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature
PGA .... +175°C
PLCC .... +150°C
Lead Temperature (Soldering 10s) .... +300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
PGA Package	32.9°C/W	7.2°C/W
MQFP	33.0°C/W	13.5°C/W
PLCC	33.8°C/W	10.9°C/W

Maximum Package Power Dissipation
PGA 3.2W
MQFP 2.4W
PLCC 2.4W
Component Count .... 193,000 Transistors

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.75V to +5.25V
Operating Temperature Range .... 0°C to +70°C

DC Electrical Specifications

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.0	-	V	V_{CC} = 5.25V
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = 4.75V
High Level Clock Input	V_{IHC}	3.0	-	V	V_{CC} = 5.25V
Low Level Clock Input	V_{ILC}	-	0.8	V	V_{CC} = 4.75V
Output HIGH Voltage	V_{OH}	2.6	-	V	I_{OH} = -400μA, V_{CC} = 4.75V
Output LOW Voltage	V_{OL}	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.75V
Input Leakage Current	I_I	-10	10	μA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V
I/O Leakage Current	I_O	-10	10	μA	V_{OUT} = V_{CC} or GND, V_{CC} = 5.25V
Standby Power Supply Current	I_{CCSB}	-	500	μA	V_{IN} = V_{CC} or GND V_{CC} = 5.25V, Note 3
Operating Power Supply Current	I_{CCOP}	-	120	mA	f = 15MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Notes 1 and 3

Capacitance T_A = +25°C, Note 2

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_{IN}	-	12	pF	FREQ = 1MHz, V_{CC} = Open, All measurements are referenced to device ground
Output Capacitance	C_O	-	10	pF	

NOTES:

1. Power supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 8mA/MHz.
2. Not tested, but characterized at initial design and at major process/design changes.
3. Output load per test load circuit with switch open and C_L = 40pF.

A.C. Electrical Specifications V_{CC} = +4.75V to +5.25V, T_A = 0°C to +70°C

PARAMETER	SYMBOL	-15 MIN	-15 MAX	-25 MIN	-25 MAX	-33 MIN	-33 MAX	UNITS	TEST CONDITIONS
Input Clock Frequency	F_{CK}	0	15	0	25.6	0	33	MHz	
FIR Clock Frequency	F_{FIR}	0	15	0	25.6	0	33	MHz	
Input Clock Period	T_{CK}	66	-	39	-	30	-	ns	
FIR Clock Period	T_{FIR}	66	-	39	-	30	-	ns	
Clock Pulse Width Low	T_{SPWL}	26	-	16	-	13	-	ns	
Clock Pulse Width High	T_{SPWH}	26	-	16	-	13	-	ns	
Clock Skew Between FIR_CK and CK_IN	T_{SK}	0	T_{FIR}-25	0	T_{FIR}-15	0	T_{FIR}-15	ns	
CK_IN Pulse Width Low	T_{CH1L}	29	-	19	-	19	-	ns	Note 1, Note 4
CK_IN Pulse Width High	T_{CH1H}	29	-	19	-	19	-	ns	Note 1, Note 4
CK_IN Setup to FIR_CK	T_{CIS}	27	-	17	-	17	-	ns	Note 1, Note 4
CK_IN Hold from FIR_CK	T_{CIH}	2	-	2	-	2	-	ns	Note 1, Note 4
RESET# Pulse Width Low	T_{RSPW}	$4T_{CK}$	-	$4T_{CK}$	-	$4T_{CK}$	-	ns	
Recovery Time on RESET#	T_{RTRS}	$8T_{CK}$	-	$8T_{CK}$	-	$8T_{CK}$	-	ns	
ASTARTIN# Pulse Width Low	T_{AST}	T_{CK}+10	-	T_{CK}+10	-	T_{CK}+10	-	ns	
STARTOUT# Delay from CK_IN	T_{STOD}	-	35	-	20	-	18	ns	
STARTIN# Setup to CK_IN	T_{STIC}	25	-	15	-	10	-	ns	
Setup Time on DATA_IN	T_{SET}	20	-	15	-	14	-	ns	
Hold Time on All inputs	T_{HOLD}	0	-	0	-	0	-	ns	
Write Pulse Width Low	T_{WL}	26	-	15	-	12	-	ns	
Write Pulse Width High	T_{WH}	26	-	20	-	18	-	ns	
Setup Time on Address Bus Before the Rising Edge of Write	T_{STADD}	26	-	20	-	20	-	ns	
Setup Time on Chip Select Before the Rising Edge of Write	T_{STCS}	26	-	20	-	20	-	ns	
Setup Time on Control Bus Before the Rising Edge of Write	T_{STCB}	26	-	20	-	20	-	ns	
DATA_RDY Pulse Width Low	T_{DRPWL}	$2T_{FIR}$-20	-	$2T_{FIR}$-10	-	$2T_{FIR}$-10	-	ns	
DATA_OUT Delay Relative to FIR_CK	T_{FIRDV}	-	50	-	35	-	28	ns	
DATA RDY Valid Delay Relative to FIR_CK	T_{FIRDR}	-	35	-	25	-	20	ns	
DATA_OUT Delay Relative to OUT_SELH	T_{OUT}	-	25	-	20	-	20	ns	
Output Enable to Data Out Valid	T_{OEV}	-	15	-	15	-	15	ns	Note 2
Output Disable to Data Out Three State	T_{OEZ}	-	15	-	15	-	15	ns	Note 1
Output Rise, Output Fall Times	T_R,T_F	-	8	-	8	-	6	ns	from .8V to 2V, Note 1

NOTES:

1. Controlled by design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
2. Transition is measured at ±200mV from steady state voltage with loading as specified in test load circuit with and C_L = 40pF.
3. A.C. Testing is performed as follows: Input levels (CLK Input) 4.0V and 0V, Input levels (all other Inputs) 0V and 3.0V, Timing reference levels (CLK) = 2.0V, (Others) = 1.5V, Output load per test load circuit and C_L = 40pF.
4. Applies only when H_BYP = 1 or H_DRATE = 0.

Absolute Maximum Ratings

Supply Voltage . . . . . . +8.0V
Input or Output Voltage Applied . . . . GND -0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . . . -65°C to +150°C
Junction Temperature . . . . . . +175°C
Lead Temperature (Soldering 10s) . . . . . . 300°C
ESD Classification . . . . . . Class 1

Reliability Information

Gate Count 48, 250

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . . -55°C to +125°C

DC Electrical Specifications T_A = -55°C to +125°C

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.2	-	V	V_{CC} = 5.5V
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = 4.5V
Output HIGH Voltage	V_{OH}	2.6	-	V	I_{OH} = -400µA, V_{CC} = 4.5V (Note 1)
Output LOW Voltage	V_{OL}	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.5V (Note 1)
Input Leakage Current	I_I	-10	+10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V
Output Leakage Current	I_O	-10	+10	µA	V_{OUT} = V_{CC} or GND, V_{CC} = 5.5V
Clock Input High	V_{IHC}	3.0	-	V	V_{CC} = 5.5V
Clock Input Low	V_{ILC}	-	0.8	V	V_{CC} = 4.5V
Standby Power Supply Current	I_{CCSB}	-	500	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open
Operating Power Supply Current	I_{CCOP}	-	120	mA	f = 15MHz, V_{CC} = 5.5V (Note 2)
Functional Test	FT	-	-		(Note 3)

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 8mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH} = 2.6V, V_{IL} = 0.4V, $V_{OH} \geq$ 1.5V, $V_{OL} \leq$ 1.5V, V_{IHC} = 3.4V and V_{ILC} = 0.4V.

AC Electrical Specifications T_A = -55°C to +125°C

PARAMETER	SYMBOL	-15 (15MHz)		-25 (25.6MHz)		UNITS	(NOTE 1) CONDITIONS
		MIN	MAX	MIN	MAX		
Input Clock Period	T_{CK}	66	-	39	-	ns	
FIR Clock Period	T_{FIR}	66	-	39	-	ns	
Clock Pulse Width Low	T_{SPWL}	26	-	16	-	ns	
Clock Pulse Width High	T_{SPWH}	26	-	16	-	ns	
Clock Skew Between FIR_CK and CK_IN	T_{SK}	0	T_{FIR} - 25	0	T_{FIR} - 19	ns	
RESET# Pulse Width Low	T_{RSPW}	$4T_{CK}$	-	$4T_{CK}$	-	ns	
Recovery Time On RESET#	T_{RTRS}	$8T_{CK}$	-	$8T_{CK}$	-	ns	
ASTARTIN# Pulse Width Low	T_{AST}	T_{CK} + 10	-	T_{CK} + 10	-	ns	
STARTOUT# Delay From CK_IN	T_{STOD}	-	35	-	20	ns	
STARTIN# Setup To CK_IN	T_{STIC}	25	-	15	-	ns	

AC Electrical Specifications T_A = -55°C to +125°C (Continued)

PARAMETER	SYMBOL	-15 (15MHz) MIN	-15 (15MHz) MAX	-25 (25.6MHz) MIN	-25 (25.6MHz) MAX	UNITS	(NOTE 1) CONDITIONS
Setup Time on DATA_IN	T_{SET}	20	-	16	-	ns	
Hold Time on All Inputs	T_{HOLD}	0	-	0	-	ns	
Write Pulse Width Low	T_{WL}	26	-	15	-	ns	
Write Pulse Width High	T_{WH}	26	-	20	-	ns	
Setup Time on Address Bus Before the Rising Edge of Write	T_{STADD}	28	-	24	-	ns	
Setup Time on Chip Select Before the Rising Edge of Write	T_{STCS}	28	-	24	-	ns	
Setup Time on Control Bus Before the Rising Edge of Write	T_{STCB}	28	-	24	-	ns	
DATA_RDY Pulse Width Low	T_{DRPWL}	$2T_{FIR}$ - 20	-	$2T_{FIR}$ - 10	-	ns	
DATA_OUT Delay Relative to FIR_CK	T_{FIRDV}	-	50	-	35	ns	
DATA_RDY Valid Delay Relative to FIR_CK	T_{FIRDR}	-	35	-	25	ns	
DATA_OUT Delay Relative to OUT_SELH	T_{OUT}	-	30	-	25	ns	
Output Enable to Data Out Valid	T_{OEV}	-	20	-	20	ns	(Note 2)

NOTES:

1. AC Testing: V_{CC} = 4.5V and 5.5V. Inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a Logic "1" and "0". CLK is driven at 4.0V and 0V and measured at 2.0V.
2. Transition is measured at ±200mV from steady state voltage with loading as specified by test load circuit and C_L = 40pF.

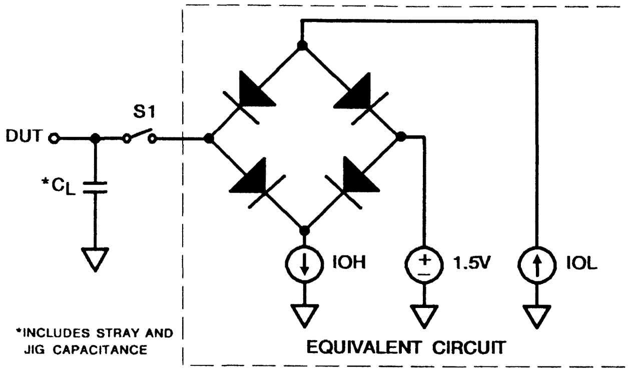
Electrical Specifications T_A = -55°C to +125°C

PARAMETER	SYMBOL	NOTES	-15 MIN	-15 MAX	-25 MIN	-25 MAX	UNITS	CONDITIONS
CK_IN Pulse Width Low	T_{CH1L}	1, 3	29	-	19	-	ns	
CK_IN Pulse Width High	T_{CH1H}	1, 3	29	-	19	-	ns	
CK_IN Setup to FIR_CK	T_{CIS}	1, 3	27	-	17	-	ns	
CK_IN Hold from FIR_CK	T_{CIH}	1, 3	2	-	2	-	ns	
Output Disable Delay	T_{OEZ}	1, 2	-	20	-	20	ns	
Output Rise Time	T_{OR}	1, 2	-	8	-	8	ns	
Output Fall Time	T_{OF}	1, 2	-	8	-	8	ns	

NOTES:

1. The parameters in this table are controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
2. Loading is as specified in the test load circuit with C_L = 40pF.
3. Applies only when H_BYP = 1 or H_DRATE = 0.

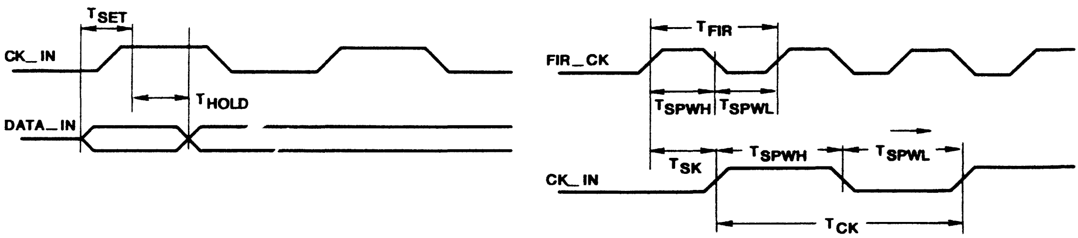
Test Load Circuit



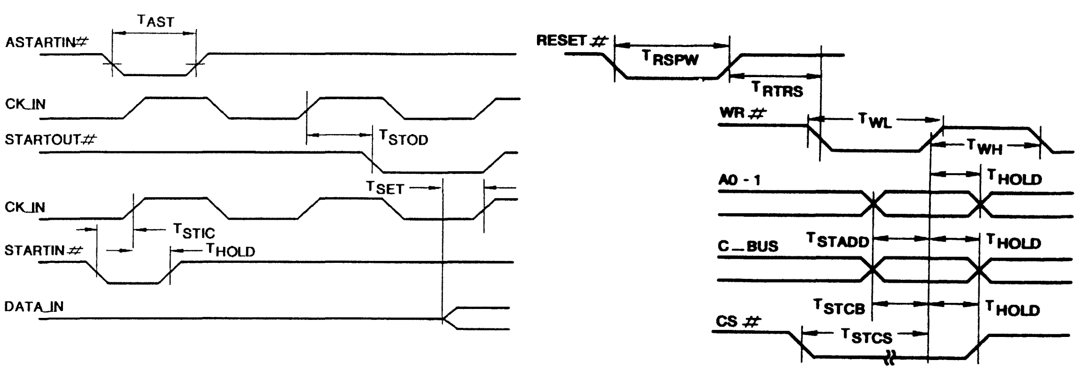
Switch S1 Open for I_{CCSB} and I_{CCOP} Tests

Timing Waveforms

INPUT TIMING

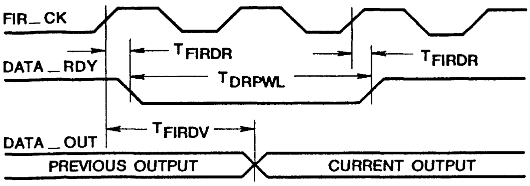


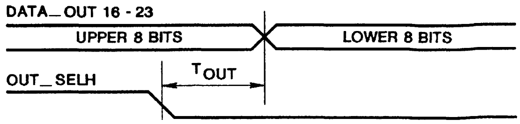
START TIMING

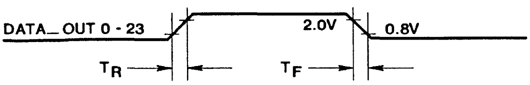


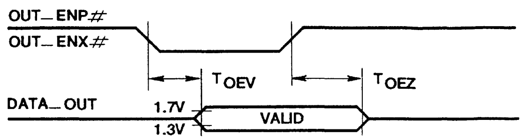
Timing Waveforms (Continued)

OUTPUT TIMING









HSP43220/883

January 1994

Decimating Digital Filter

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Single Chip Narrow Band Filter with up to 96dB Attenuation
- DC to 25.6MHz Clock Rate
- 16-Bit 2's Complement Input
- 20-Bit Coefficients in FIR
- 24-Bit Extended Precision Output
- Programmable Decimation up to a Maximum of 16,384
- Standard 16-Bit Microprocessor Interface
- Filter Design Software Available DECI•MATE™

Applications

- Very Narrow Band Filters
- Zoom Spectral Analysis
- Channelized Receivers

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43220GM-15/883	-55°C to +125°C	84 Lead PGA
HSP43220GM-25/883	-55°C to +125°C	84 Lead PGA

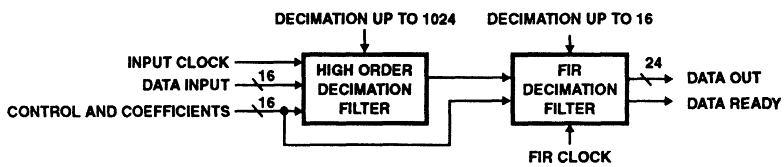
Description

The HSP43220/883 Decimating Digital Filter is a linear phase low pass decimation filter which is optimized for and filtering narrow band signals in a broad spectrum of a signal processing applications. The HSP43220/883 offers a single chip solution to signal processing application which have historically required several boards of IC's. This reduction in component count results in faster development times as well as reduction of hardware costs.

The HSP43220/883 is implemented as a two stage filter structure. As seen in the block diagram, the first stage is a high order decimation filter (HDF) which utilizes an efficient decimation (sample rate reduction) technique to obtain decimation up to 1024 through a coarse low-pass filtering process. The HDF provides up to 96dB aliasing rejection in the signal pass band. The second stage consists of a finite impulse response (FIR) decimation filter structured as a transversal FIR filter with up to 512 symmetric taps which can implement filters with sharp transition regions. The FIR can perform further decimation by up to 16 if required while preserving the 96dB aliasing attenuation obtained by the HDF. The combined total decimation capability is 16,384.

The HSP43220/883 accepts 16-bit parallel data in 2's complement format at sampling rates up to 30MSPS. It provides a 16-bit microprocessor compatible interface to simplify the task of programming and three-state outputs to allow the connection of several IC's to a common bus. The HSP43220/883 also provides the capability to bypass either the HDF or the FIR for additional flexibility.

Block Diagram



Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output Voltage Applied .... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering, Ten Seconds) .... +300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic PGA Package	32.9°C/W	7.2°C/W

Maximum Package Power Dissipation at +125°C
Ceramic PGA Package .... 1.52 Watt
Gate Count .... 48,250 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range .... -55°C to +125°C

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	-55°C $\leq T_A \leq$ +125°C	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	-55°C $\leq T_A \leq$ +125°C	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C $\leq T_A \leq$ +125°C	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C $\leq T_A \leq$ +125°C	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	-55°C $\leq T_A \leq$ +125°C	-10	+10	µA
Output Leakage Current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	-55°C $\leq T_A \leq$ +125°C	-10	+10	µA
Clock Input High	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	-55°C $\leq T_A \leq$ +125°C	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	-55°C $\leq T_A \leq$ +125°C	-	0.8	V
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V, Outputs Open	1, 2, 3	-55°C $\leq T_A \leq$ +125°C	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 15.0MHz V_{CC} = 5.5V (Note 2)	1, 2, 3	-55°C $\leq T_A \leq$ +125°C	-	120.0	mA
Functional Test	FT	(Note 3)	7, 8	-55°C $\leq T_A \leq$ +125°C	-	-	

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 8mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, VOH $\geq$ 1.5V, $V_{OL} \leq$ 1.5V, V_{IHC} = 3.4V, and V_{ILC} = 0.4V.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS -15 (15MHz) MIN	LIMITS -15 (15MHz) MAX	LIMITS -25 (25.6MHz) MIN	LIMITS -25 (25.6MHz) MAX	UNITS
Input Clock Period	T_{CK}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	66	-	39	-	ns
FIR Clock Period	T_{FIR}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	66	-	39	-	ns
Clock Pulse Width Low	T_{SPWL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	26	-	16	-	ns
Clock Pulse Width High	T_{SPWH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	26	-	16	-	ns
Clock Skew Between FIR_CK and CK_IN	T_{SK}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	T_{FIR} - 25	0	T_{FIR} - 19	ns
RESET# Pulse Width Low	T_{RSPW}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	$4T_{CK}$	-	$4T_{CK}$	-	ns
Recovery Time On RESET#	T_{RTRS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	$8T_{CK}$	-	$8T_{CK}$	-	ns
ASTARTIN# Pulse Width Low	T_{AST}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	T_{CK} + 10	-	T_{CK} + 10	-	ns
STARTOUT# Delay From CK_IN	T_{STOD}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	35	-	20	ns
STARTIN# Setup To CK_IN	T_{STIC}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	25	-	15	-	ns
Setup Time on DATA_IN	T_{SET}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	16	-	ns
Hold Time on All Inputs	T_{HOLD}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Write Pulse Width Low	T_{WL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	26	-	15	-	ns
Write Pulse Width High	T_{WH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	26	-	20	-	ns
Setup Time on Address Bus Before the Rising Edge of Write	T_{STADD}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	28	-	24	-	ns
Setup Time on Chip Select Before the Rising Edge of Write	T_{STCS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	28	-	24	-	ns
Setup Time on Control Bus Before the Rising Edge of Write	T_{STCB}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	28	-	24	-	ns
DATA_RDY Pulse Width Low	T_{DRPWL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	$2T_{FIR}$ - 20	-	$2T_{FIR}$ - 10	-	ns
DATA_OUT Delay Relative to FIR_CK	T_{FIRDV}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	50	-	35	ns
DATA_RDY Valid Delay Relative to FIR_CK	T_{FIRDR}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	35	-	25	ns
DATA_OUT Delay Relative to OUT_SELH	T_{OUT}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	30	-	25	ns
Output Enable to Data Out Valid	T_{OEV}	Note 2	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	20	-	20	ns

NOTES:

1. A.C. Testing: VCC = 4.5V and 5.5V. Inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a Logic "1" and "0". CLK is driven at 4.0V and 0V and measured at 2.0V.
2. Transition is measured at ±200mV from steady state voltage with loading as specified by test load circuit and C_L = 40pF.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS -15 (15MHz) MIN	LIMITS -15 (15MHz) MAX	LIMITS -25 (25.6MHz) MIN	LIMITS -25 (25.6MHz) MAX	UNITS
CK_IN Pulse Width Low	T_{CH1L}		1, 3	$-55^oC \leq T_A \leq +125^oC$	29	-	19	-	ns
CK_IN Pulse Width High	T_{CH1H}		1, 3	$-55^oC \leq T_A \leq +125^oC$	29	-	19	-	ns
CK_IN Setup to FIR_CK	T_{CIS}		1, 3	$-55^oC \leq T_A \leq +125^oC$	27	-	17	-	ns
CK_IN Hold from FIR_CK	T_{CIH}		1, 3	$-55^oC \leq T_A \leq +125^oC$	2	-	2	-	ns
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	12	-	12	pF
Output Capacitance	C_{OUT}	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	10	-	10	pF
Output Disable Delay	T_{OEZ}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	20	-	20	ns
Output Rise Time	T_{OR}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	8	-	8	ns
Output Fall Time	T_{OF}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	8	-	8	ns

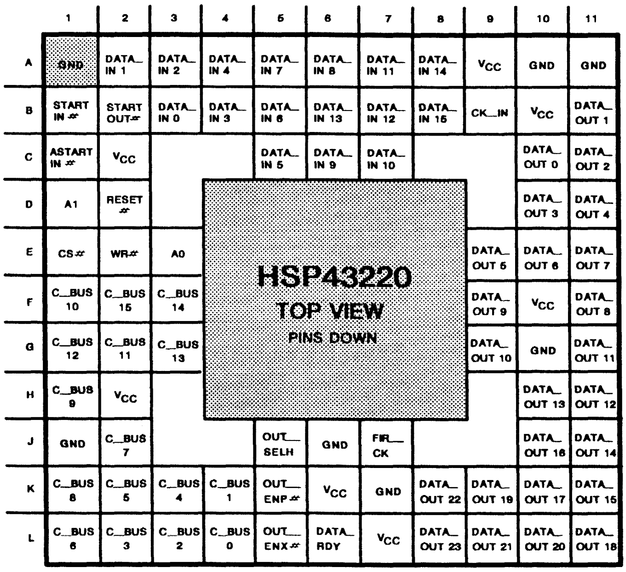
NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Loading is as specified in the test load circuit with C_L = 40pF.
3. Applies only when H_BYP = 1 or H_DRATE = 0.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	—	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Burn-In Circuit



PIN LEAD	PIN NAME	BURN-IN SIGNAL
A1	GND	GND
A2	DATA_IN 1	F2
A3	DATA_IN 2	F3
A4	DATA_IN 4	F5
A5	DATA_IN 7	F8
A6	DATA_IN 8	F1
A7	DATA_IN 11	F4
A8	DATA_IN 14	F7
A9	V_{CC}	V_{CC}
A10	GND	GND
A11	GND	GND
B1	STARTIN#	F15
B2	STARTOUT#	$V_{CC}/2$
B3	DATA_IN 0	F1
B4	DATA_IN 3	F4
B5	DATA_IN 6	F7
B6	DATA_IN 13	F6
B7	DATA_IN 12	F5
B8	DATA_IN 15	F8
B9	CK_IN	F0
B10	V_{CC}	V_{CC}
B11	DATA_OUT 1	$V_{CC}/2$

PIN LEAD	PIN NAME	BURN-IN SIGNAL
C1	ASTARTIN#	F15
C2	V_{CC}	V_{CC}
C5	DATA_IN 5	F6
C6	DATA_IN 9	F2
C7	DATA_IN 10	F3
C10	DATA_OUT 0	$V_{CC}/2$
C11	DATA_OUT 2	$V_{CC}/2$
D1	A1	F14
D2	RESET#	F16
D10	DATA_OUT 3	$V_{CC}/2$
D11	DATA_OUT 4	$V_{CC}/2$
E1	CS#	F11
E2	WR#	F11
E3	A0	F13
E9	DATA_OUT 5	$V_{CC}/2$
E10	DATA_OUT 6	$V_{CC}/2$
E11	DATA_OUT 7	$V_{CC}/2$
F1	C_BUS 10	F3
F2	C_BUS 15	F8
F3	C_BUS 14	F7
F9	DATA_OUT 9	$V_{CC}/2$
F10	V_{CC}	V_{CC}

PIN LEAD	PIN NAME	BURN-IN SIGNAL
F11	DATA_OUT 3	$V_{CC}/2$
G1	C_BUS 12	F5
G2	C_BUS 11	F4
G3	C_BUS 13	F6
G9	DATA_OUT 10	$V_{CC}/2$
G10	GND	GND
G11	DATA_OUT 11	$V_{CC}/2$
H1	C_BUS 9	F2
H2	V_{CC}	V_{CC}
H10	DATA_OUT 13	$V_{CC}/2$
H11	DATA_OUT 12	$V_{CC}/2$
J1	GND	GND
J2	C_BUS 7	F8
J5	OUT_SELH	F10
J6	GND	GND
J8	FIR_CK	F0
J10	DATA_OUT 16	$V_{CC}/2$
J11	DATA_OUT 14	$V_{CC}/2$
K1	C_BUS 8	F1
K2	C_BUS 5	F6
K3	C_BUS 4	F5
K4	C_BUS 1	F2

NOTES:

1. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5 ±0.5V.
4. 0.1μF (min) capacitor between V_{CC} and GND per position.
5. F0 = 100kHz ±10%, F1 = F0/2, F2 = F1/2 ..... F16 = F15/2, 40% - 60% Duty Cycle.
6. Input voltage limits: V_{IL} = 0.8 max, V_{IH} = 4.5V ±10%.

Burn-In Circuit (Continued)

PIN LEAD	PIN NAME	BURN-IN SIGNAL
K5	OUT_ENP#	F9
K6	V_{CC}	V_{CC}
K7	GND	GND
K8	DATA_OUT 22	$V_{CC}/2$
K9	DATA_OUT 19	$V_{CC}/2$
K10	DATA_OUT 17	$V_{CC}/2$

PIN LEAD	PIN NAME	BURN-IN SIGNAL
K11	DATA_OUT 15	$V_{CC}/2$
L1	C_BUS 6	F7
L2	C_BUS 3	F4
L3	C_BUS 2	F3
L4	C_BUS 0	F1
L5	OUT_ENX#	F9

PIN LEAD	PIN NAME	BURN-IN SIGNAL
L6	DATA_RDY#	$V_{CC}/2$
L7	V_{CC}	V_{CC}
L8	DATA_OUT 23	$V_{CC}/2$
L9	DATA_OUT 21	$V_{CC}/2$
L10	DATA_OUT 20	$V_{CC}/2$
L11	DATA_OUT 18	$V_{CC}/2$

NOTES:

1. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5 ±0.5V.
4. 0.1µF (min) capacitor between V_{CC} and GND per position.
5. F0 = 100kHz ±10%, F1 = F0/2, F2 = F1/2 ..... F16 = F15/2, 40% - 60% Duty Cycle.
6. Input voltage limits: V_{IL} = 0.8 max, V_{IH} = 4.5V ±10%.

Metal Topology

DIE DIMENSIONS:
348 x 349.2 x 19±1 mils

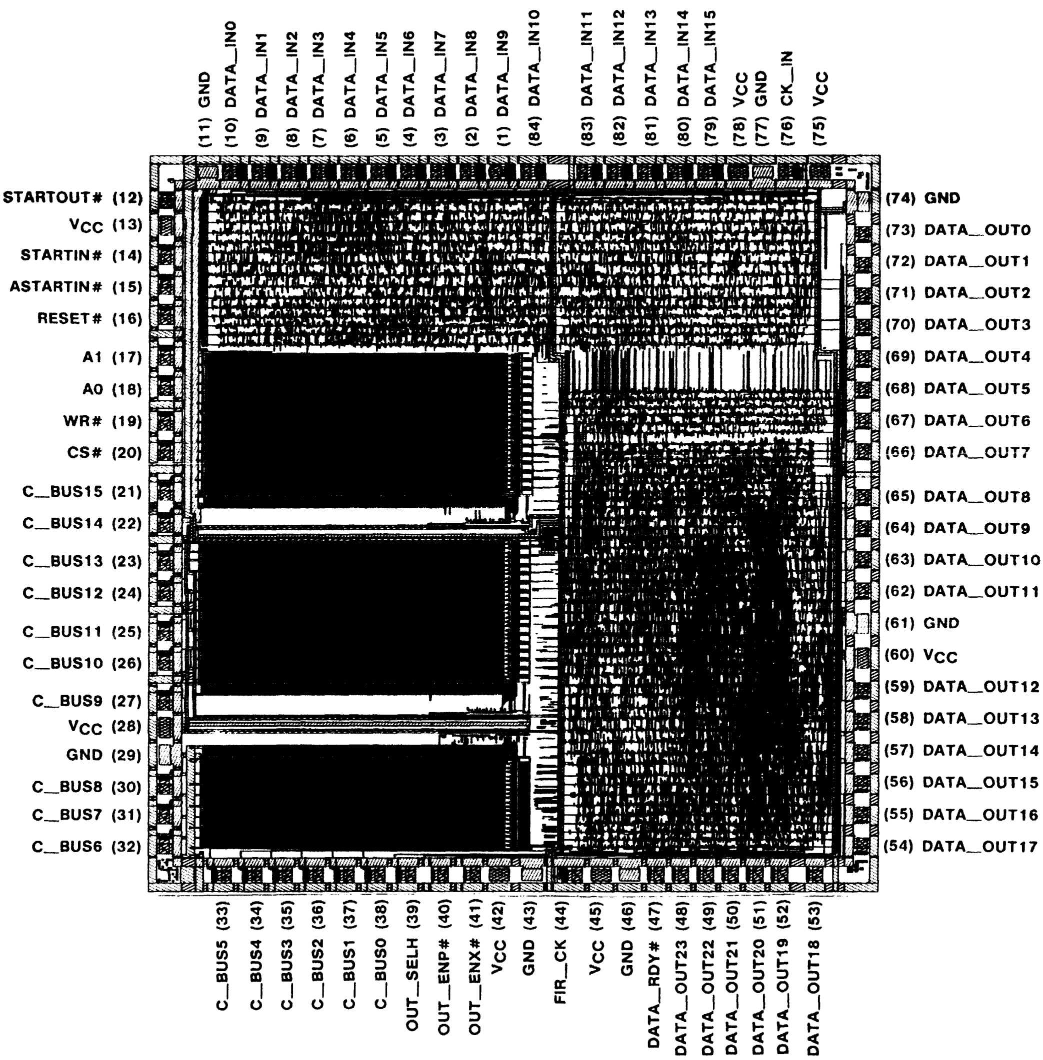
METALLIZATION:
Type: Si - Al or Si - Al - Cu
Thickness: 8kÅ

WORST CASE CURRENT DENSITY:
1.18 x $10^5 A/cm^2$

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

Metallization Mask Layout

HSP43220/883



HARRIS SEMICONDUCTOR

HSP43481

January 1994

Digital Filter

Features

- Four Filter Cells
- 0MHz to 30MHz Sample Rate
- 8-Bit Coefficients and Signal Data
- 26-Bit Accumulator per Stage
- Filter Lengths Up to 1032 Tap
- Expandable Coefficient Size, Data Size and Filter Length
- Decimation by 2, 3 or 4

Applications

- 1-D and 2-D FIR Filters
- Radar/Sonar
- Adaptive Filters
- Echo Cancellation
- Complex Multiply-Add
- Sample Rate Converters

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43481JC-20	0°C to +70°C	68 Lead PLCC
HSP43481JC-25	0°C to +70°C	68 Lead PLCC
HSP43481JC-30	0°C to +70°C	68 Lead PLCC
HSP43481GC-20	0°C to +70°C	68 Lead PGA
HSP43481GC-25	0°C to +70°C	68 Lead PGA
HSP43481GC-30	0°C to +70°C	68 Lead PGA

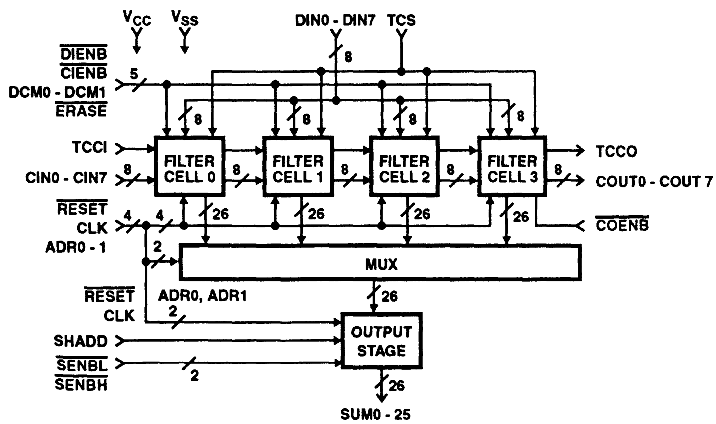
Description

The HSP43481 is a video-speed Digital Filter (DF) designed to efficiently implement vector operations such as FIR digital filters. It is comprised of four filter cells cascaded internally and a shift-and-add output stage, all in a single integrated circuit. Each filter cell contains an 8 x 8 multiplier, three decimation registers and a 26-bit accumulator which can add the contents of any filter cell accumulator to the output stage accumulator shifted right by eight-bits. The HSP43481 has a maximum sample rate of 30MHz. The effective multiply-accumulate (MAC) rate is 120MHz.

The HSP43481 can be configured to process expanded coefficient and word sizes. Multiple devices can be cascaded for larger filter lengths without degrading the sample rate or a single device can process larger filter lengths at less than 30MHz with multiple passes. The architecture permits processing filter lengths of over 1000 taps with the guarantee of no overflows. In practice, most filter coefficients are less than 1.0, making even larger filter lengths possible. The HSP43481 provides for unsigned or two's complement arithmetic, independently selectable for coefficients and signal data.

Each DF filter cell contains three resampling or decimation registers which permit output sample rate reduction at rates of $^1/_2$, $^1/_3$ or $^1/_4$ the input sample rate. These registers also provide the capability to perform 2-D operations such as N x N spatial correlations/convolutions for image processing applications.

Block Diagram



File Number **2759.3**

Pinouts

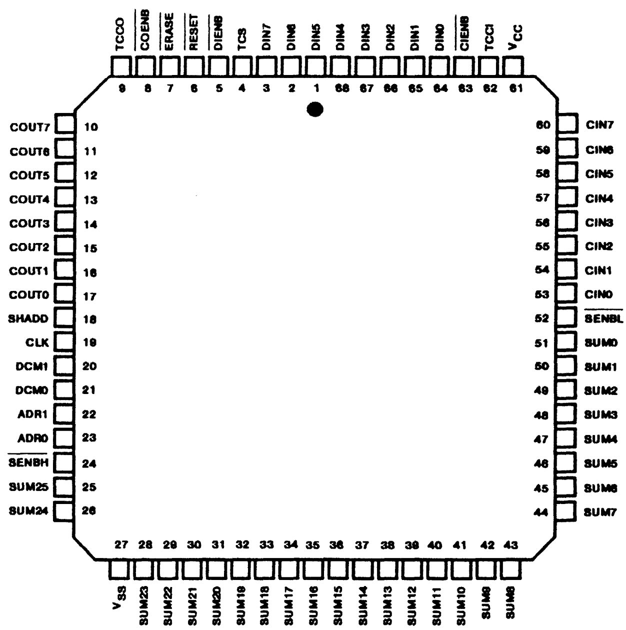
68 PIN CERAMIC PIN GRID ARRAY (PGA)
BOTTOM VIEW

	1	2	3	4	5	6	7	8	9	10	11
L		COUT7	COUT5	COUT3	COUT1	COUT0	CLK	ADDR1	ADDR0	SUM25	
K	TCCO	$\overline{\text{COENB}}$	COUT6	COUT4	COUT2	SHADD	DCM1	DCM0	$\overline{\text{SENBH}}$	SUM24	SUM23
J	$\overline{\text{ERASE}}$	V_{CC}								SUM21	SUM22
H	$\overline{\text{RESET}}$	$\overline{\text{DIENB}}$								SUM19	SUM20
G	TCS	DIN7								SUM17	SUM18
F	DIN5	DIN6				68 LEAD PIN GRID ARRAY BOTTON VIEW				SUM15	SUM16
E	DIN3	DIN4								V_{SS}	SUM14
D	DIN1	DIN2								SUM12	SUM13
C	DIN0	$\overline{\text{CIENB}}$								SUM10	SUM11
B	TCCI	CIN6	CIN4	CIN2	CIN0	SUM0	SUM2	SUM4	SUM6	SUM8	SUM9
A		CIN7	CIN5	CIN3	CIN1	$\overline{\text{SENBL}}$	SUM1	SUM3	SUM5	SUM7	

68 PIN CERAMIC PIN GRID ARRAY (PGA)
TOP VIEW

	11	10	9	8	7	6	5	4	3	2	1
L		SUM25	ADDR0	ADDR1	CLK	COUT0	COUT1	COUT3	COUT5	COUT7	
K	SUM23	SUM24	$\overline{\text{SENBH}}$	DCM0	DCM1	SHADD	COUT2	COUT4	COUT6	$\overline{\text{COENB}}$	TCCO
J	SUM22	SUM21								V_{CC}	$\overline{\text{ERASE}}$
H	SUM20	SUM19								$\overline{\text{DIENB}}$	$\overline{\text{RESET}}$
G	SUM18	SUM17								DIN7	TCS
F	SUM16	SUM15				68 LEAD PIN GRID ARRAY TOP VIEW				DIN6	DIN5
E	SUM14	V_{SS}								DIN4	DIN3
D	SUM13	SUM12								DIN2	DIN1
C	SUM11	SUM10								$\overline{\text{CIENB}}$	DIN0
B	SUM9	SUM8	SUM6	SUM4	SUM2	SUM0	CIN0	CIN2	CIN4	CIN6	TCCI
A		SUM7	SUM5	SUM3	SUM1	$\overline{\text{SENBL}}$	CIN1	CIN3	CIN5	CIN7	

68 PIN PLASTIC LEADED CHIP CARRIER (PLCC)
TOP VIEW



Pin Description

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
V_{CC}	61		+5V Power Supply Input
V_{SS}	27		Power Supply Ground Input
CLK	19	I	The CLK input provides the DF system sample clock. The maximum clock frequency is is 30MHz.
DIN0-7	64-68 1-3	I	These eight inputs are the data sample input bus. Eight bit data samples are synchronously loaded through these pins to the X register of each filter cell simultaneously. The $\overline{\text{DIENB}}$ signal enables loading, which is synchronous on the rising edge of the clock signal.
TCS	4	I	The TCS input determines the number system interpretation of the data input samples on pins DIN0-7 as follows: TCS = Low → Unsigned Arithmetic TCS = High → Two's Complement Arithmetic The TCS signal is synchronously loaded into the X register in the same way as the DIN0-7 inputs.
$\overline{\text{DIENB}}$	5	I	A low on this enables the data sample input bus (DIN0-7) to all the filter cells. A rising edge of the CLK signal occurring while $\overline{\text{DIENB}}$ is low will load the X register of every filter cell with the 8 bit value present on DIN0-7. A high on this input forces all the bits of the data sample input bus to zero; a rising CLK edge when $\overline{\text{DIENB}}$ is high will load the X register of every filter cell with all zeros. This signal is latched inside the DF, delaying its effect by one clock internal to the DF. Therefore, it must be low during the clock cycle immediately preceding presentation of the desired data on the DIN0-7 inputs. Detailed operation is shown in later timing diagrams.
CIN0-7	53-60	I	These eight inputs are used to input the 8 bit coefficients. The coefficients are synchronously synchronously loaded into the C register of filter Cell 0 if a rising edge of CLK occurs while $\overline{\text{CIENB}}$ is low. The $\overline{\text{CIENB}}$ signal is delayed by one clock as discussed below.
TCCI	62	I	The TCCI input determines the number system interpretation of the coefficient inputs on pins CIN0-7 as follows: TCCI = LOW → Unsigned Arithmetic TCCI = HIGH → Two's Complement Arithmetic The TCCI signal is synchronously loaded into the C register in the same way as the CIN0-7 inputs.
$\overline{\text{CIENB}}$	63	I	A low on this input enable the C register of every filter cell and the D registers (decimation) of every filter cell according to the state of the DCM0-1 inputs. A rising edge of the CLK signal occurring while $\overline{\text{CIENB}}$ is low will load the C register and appropriate D registers with the coefficient data present at their inputs. This privides the mechanism for shifting the coefficients from cell to cell through the device. A high on this input freezes the contents of the C register and the D registers, ignoring the CLK signal. This signal is latched and delayed by one clock internal to the DF. Therefore, it must be low during the clock cycle immediately preceding presentation of the desired coefficient on the CIN0-7 inputs. Detailed operation is shown in the Timing Diagrams section.
COUT0-7	10-17	O	These eight three-state outputs are used to output the 8 bit coefficients from filter cell 7. These outputs are enabled by the $\overline{\text{COENB}}$ signal low. These outputs may be tied to the CIN0-7 inputs of the same DF to recirculate the coefficients, or they may be tied to the CIN0-7 inputs of another DF to cascade DFs for longer filter lengths.
TCCO	9	O	The TCCO three-state output determines the number system representation of the coefficients output on COUT0-7. It tracks the TCCI signal to this same DF. It should be tied to the TCCI input of the next DF in a cascade of DFs for increased filter lengths. This signal is enabled by $\overline{\text{COENB}}$ low.

Pin Descriptions

SYMBOL	PIN NUMBER	TYPE	NAME FUNCTION
$\overline{\text{COENB}}$	8	I	A low on the $\overline{\text{COENB}}$ input enables the COUT0-7 and the TCCO output. A high on this input places all these outputs in their high impedance state.
DCM0-1	20 - 21	I	These two inputs determine the use of the internal decimation registers as follows: DCM1 / DCM0 / Decimation Function 0 / 0 / Decimation registers not used 0 / 1 / One decimation register is used 1 / 0 / Two decimation registers are used 1 / 1 / Three decimation registers are used The coefficients pass from cell to cell at a rate determined by the number of decimation registers used. When no decimation registers are used, coefficients move from cell to cell on each clock. When one decimation register is used, coefficients move from cell to cell on every other clock, etc. These signals are latched and delayed by one clock internal to the DF.
SUM0-25	25, 26, 28-51	O	These 26 three-state outputs are used to output the results of the internal filter cell computations. Individual filter cell results or the result of the shift-and-add output stage can be output. If an individual filter cell result is to be output, the ADR0-1 signals select the filter cell result. The SHADD signal determines whether the selected filter cell result or the output stage adder result is output. The signals $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ enable the most significant and least significant bits of the SUM0-25 result, respectively. Both $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ may be enabled simultaneously if the system has a 26 bit or larger bus. However, individual enables are provided to facilitate use with a 16 bit bus.
$\overline{\text{SENBH}}$	24	I	A low on this input enables result bits SUM16-25. A high on this input places these bits in their high impedance state.
$\overline{\text{SENBL}}$	52	I	A low on this input enables result bits SUM0-15. A high on this input places these bits on their high impedance state.
ADR0-1	22, 23	I	These two inputs select the one cell whose accumulator will be read through the output bus (SUM0-25) or added to the output stage accumulator. They also determine which accumulator will be cleared when $\overline{\text{ERASE}}$ is low. For selection of which accumulator to read through the output bus (SUM0-25) or which to add of the output stage accumulator, these inputs are latched in the DF and delayted by one clock internal to the device. If the ADR0-1 lines remain at the same address for more than one clock, the output at SUM0-25 will not change to reflect any subsequent accumulator updates in the addressed cell. Only the result available during the first clock, when ADR0-1 selects the cell, will be output. This does not hinder normal operation since the ADR0-1 lines are changed sequentially. This feature facilitates the interface with slow memories where the output is required to be fixed for more than one clock.
SHADD	18	I	The SHADD input controls the activation of the shift-and-add operation in the output stage. This signal is latched in the DF and delayed by one clock internal to the device. A detailed explanation is given in the DF Output Stage section.
$\overline{\text{RESET}}$	6	I	A low on this input synchronously clears all the internal registers, except the cell accumulators. It can be used with $\overline{\text{ERASE}}$ to also clear all the accumulators simultaneously. This signal is latched in the DF and delayed by one clock internal to the DF.
$\overline{\text{ERASE}}$	7	I	A low on this input synchronously clears the cell accumulator selected by the ADR0-1 signals. If $\overline{\text{RESET}}$ is also low simultaneously, all cell accumulators are cleared.

Functional Description

The Digital Filter (DF) is composed of four filter cells cascaded together and an output stage for combining or selecting filter cell outputs (see Block Diagram). Each filter cell contains a multiplier-accumulator and several registers (Figure 1). Each 8 bit coefficient is multiplied by a 8 bit data sample, with the result added to the 26 bit accumulator contents. The coefficient output of each cell is cascaded to the coefficient input of the next cell to its right.

DF Filter Cell

An 8 bit coefficient (CIN0-7, TCCI) enters each cell through the C register on the left and exits the cell on the right as signals COUT0-7 and TCCO. With no decimation, the coefficient moves directly from the C register to the output, and is valid on the clock following its entrance. When decimation is selected the coefficient exit is delayed by 1, 2 or 3 clocks by passing through one or more decimation registers (D1, D2 or D3).

The combination of D registers through which the coefficient passes is determined by the state of DCM0 and DCM1. The output signals (COUT0-7, TCCO) are connected to the CIN0-7 and TCCI of the next cell to its right. The $\overline{\text{COENB}}$ input signal enables the COUT0-7 and TCCO outputs of the right-most cell to the COUT0-7 and TCCO pins of the DF.

The C and D registers are enabled for loading by $\overline{\text{CIENB}}$. Loading is synchronous with CLK when $\overline{\text{CIENB}}$ is low. Note that $\overline{\text{CIENB}}$ is latched internally. It enables the register for loading after the next CLK following the onset of $\overline{\text{CIENB}}$ low. Actual loading occurs on the second CLK following the onset of $\overline{\text{CIENB}}$ low. Therefore, $\overline{\text{CIENB}}$ must be low during the clock cycle immediately preceding presentation of the coefficient on the CIN0-7 inputs. In most basic FIR operations, $\overline{\text{CIENB}}$ will be low throughout the process, so this latching and delay sequence is only important during the initialization phase. When $\overline{\text{CIENB}}$ is high, the coefficients are frozen.

These registers are cleared synchronously under control of $\overline{\text{RESET}}$, which is latched and delayed exactly like $\overline{\text{CIENB}}$.

The output of the C register is one input of the multiplier.

The other input of the multiplier comes from the output of the X register. This register is loaded with a data sample from the DF input signals. DIN0-7 and TCS discussed above. The X register is enabled for loading by $\overline{\text{DIENB}}$. Loading is synchronous with CLK when $\overline{\text{DIENB}}$ is low. Note that $\overline{\text{DIENB}}$ is latched internally. It enables the register for loading after the next CLK following the onset of $\overline{\text{DIENB}}$ low. Therefore, $\overline{\text{DIENB}}$ must be low during the clock cycle immediately preceding presentation of the sample on the DIN0-7 inputs. In most basic FIR operations, $\overline{\text{DIENB}}$ will be low throughout the process, so this latching and delay sequence is only important during the initialization phase. When $\overline{\text{DIENB}}$ is high, the X register is loaded with all zeros.

The multiplier is pipelined and is modeled as a multiplier core followed by two pipeline registers, MREG0 and MREG1. The multiplier output is sign extended and input as one operand of the 26 bit adder. The other adder operand is the output of the 26 bit accumulator. The adder output is loaded synchronously into both the accumulator and the TREG.

The TREG loading is disabled by the cell select signal, Celln, where n is the cell number. The cell select is decoded from the ADR0-1 signals to generate the TREG load enable. The cell select is inverted and applied as the load enable to the TREG. Operation is such that the TREG is loaded whenever the cell is not selected. Therefore, TREG is loaded every other clock except the clock following cell selection. The purpose of the TREG is to hold the result of a sum-of-products calculation during the clock when the accumulator is cleared to prepare for the next sum-of-products calculation. This allows continuous accumulation without wasting clocks.

The accumulator is loaded with the adder output every clock unless it is cleared. It is cleared synchronously in two ways. When $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ are both low, the accumulator is cleared along with all other registers in the DF. Since both $\overline{\text{ERASE}}$ and $\overline{\text{RESET}}$ are latched and delayed one clock internally, clearing occurs on the second CLK following the onset of both $\overline{\text{ERASE}}$ and $\overline{\text{RESET}}$ low.

The second accumulator clearing mechanism clears a single accumulator in a selected cell. The cell select signal, Celln, decoded from ADR0-1 and $\overline{\text{ERASE}}$ signal, Celln enable clearing of the accumulator on the next CLK.

The $\overline{\text{ERASE}}$ and $\overline{\text{RESET}}$ signals clear the DF internal registers and states as follows:

$\overline{\text{ERASE}}$	$\overline{\text{RESET}}$	CLEARING EFFECT
1	1	No clearing occurs, internal state remains same.
1	0	$\overline{\text{RESET}}$ only active, all registers except accumulators are cleared, including the internal pipeline registers.
0	1	$\overline{\text{ERASE}}$ only active, the accumulator whose address is given by the ADR0-1 inputs is cleared.
0	0	Both $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ active, all accumulators as well as all other registers are cleared.

The DF Output Stage

The output stage consists of a 26 bit adder, 26 bit register, feedback multiplexer from the register to the adder, an output multiplexer and a 26 bit three-state driver stage (Figure 2).

The 26 bit output adder can add any filter cell accumulator result to the 18 most significant bits of the outupt buffer. This operation takes place in one clock period. The eight LSBs are lost. The filter cell accumulator is selected by the ADR0-1 inputs.

The 18 MSBs of the output buffer actually pass through the zero mux on their way to the output adder input. The zero mux is controlled by the SHADD input signal and selects either the 18 MSBs of the output buffer or all zeros for the adder input. A low on the SHADD input selects zero. A high on the SHADD input selects the output buffer MSBs, thus activating the shift-and-add operation. SHADD signal is latched and delayed by one clock internally.

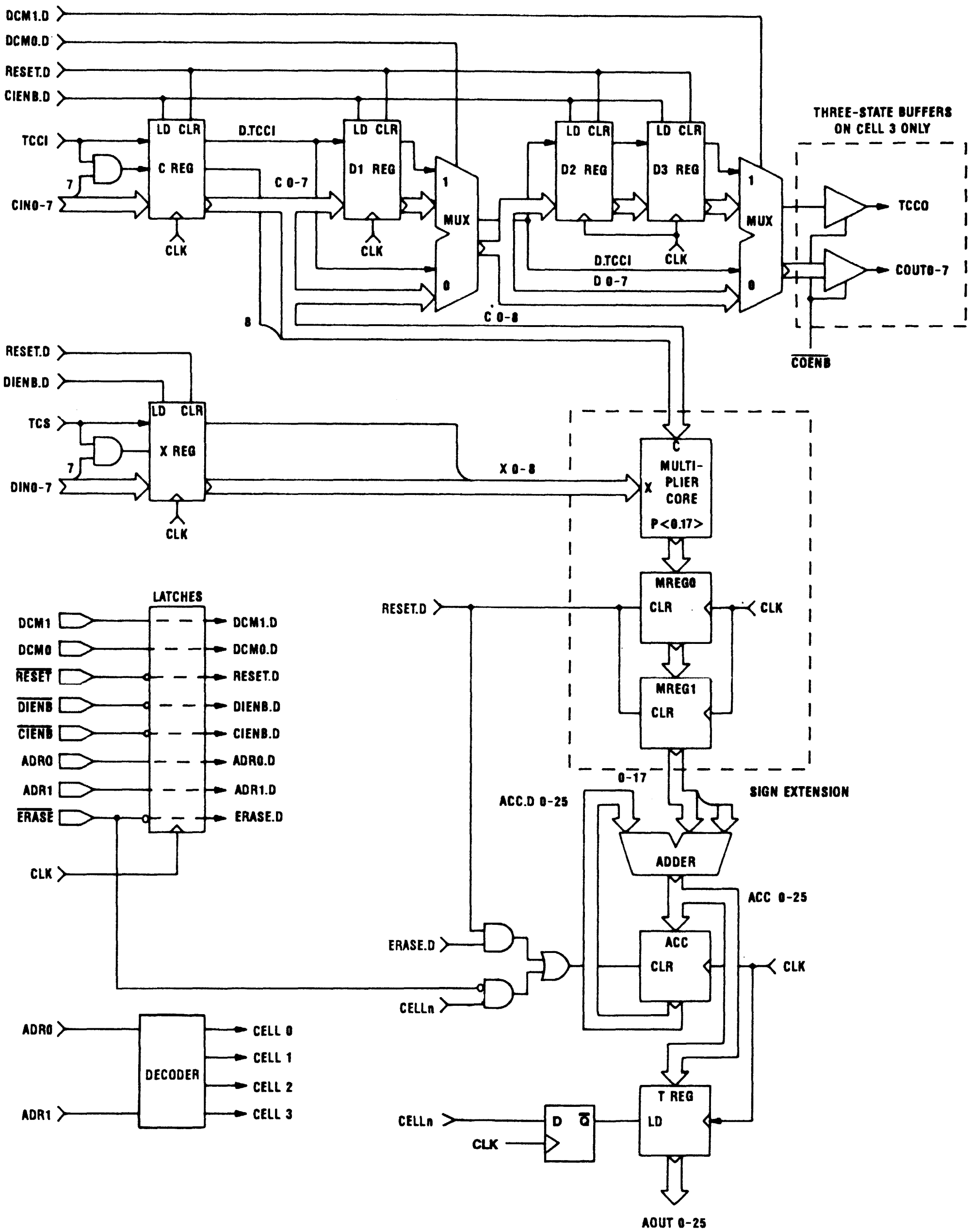


FIGURE 1. HSP43481 FILTER CELL

3

1D FILTERS

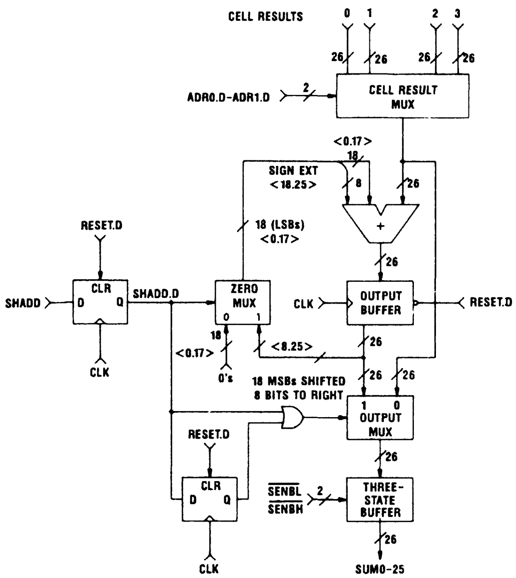


FIGURE 2. HSP43481 OUTPUT STAGE

The 26 Least Significant Bits (LSBs) from either a cell accumulator or the output buffer are output on the SUM0-25 bus. The output mux determines whether the cell accumulator selected by ADR0-1 or the output buffer is output to the bus. The mux is controlled by the SHADD input signal. Control is based on the state of the SHADD during two successive clocks; in other words, the output mux selection contains memory. If SHADD is low during a clock cycle and was low during the previous clock, the output mux selects the contents of the filter cell accumulator addressed by ADR0-1. Otherwise the output mux selects the contents of the output buffer.

If the ADR0-1 lines remain at the same address for more than one clock, the output at SUM0-25 will not change to reflect any subsequent accumulator updates in the addressed cell. Only the result available during the first clock when ADR0-1 selects the cell will be output. This does not hinder normal FIR operations since the ADR0-1 lines are changed sequentially. This feature facilitates the interface wtith slow memories where the output is required to be fixed for more than one clock.

The SUM0-25 output bus is controlled by the $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ signals. A low on $\overline{\text{SENBL}}$ enables bits SUM0-15. A low on $\overline{\text{SENBH}}$ enables bits SUM16-25. Thus all 26 bits can be output simultaneously if the external system has a 26 bit or larger bus. If the external system bus is only 16 bits, the bits can be enabled in two groups of 16 and 9 bits (sign extended).

DF Arithmetic

Both data samples and coefficients can be represented as either unsigned or two's complement numbers. The TCS and TCCI input signals determine the type of arithmetic representation. Internally all values are represented by a 9 bit two's complement number. The value of the additional ninth bit depends on arithmentic representation selected. For two's complement arithmetic, the sign is extended into the ninth bit. For unsigned arithmetic, bit 9 is 0.

The multiplier output is 18 bits and the accumulator is 26 bits. The accumulator width determines the maximum possible number of terms in the sum-of-products without overflow. The maximum number of terms depends also on the number system and the distribution of the coefficient and data values. As a worst case assume the coefficients and data samples are always at their absolute maximum values.

Then the maximum numbers of terms in the sum products are:

NUMBER SYSTEM	MAX # OF TERMS
Two unsigned vectors	1032
Two two's complement vectors:	
• Two positive vectors	2080
• Two negative vectors	2047
• One positive and one negative vector	2064
One unsigned and one two's complement vector:	
• Positive two's complement vector	1036
• Negative two's complement vector	1028

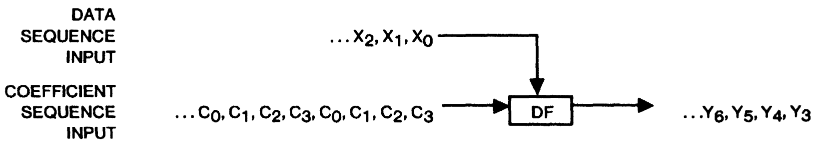
For practical FIR filters, the coefficients are never all near maximum value, so even larger vectors are possible in practice.

Basic FIR Operation

A simple 30MHz 4 tap filter example serves to illustrate more clearly the operation of the DF. Table 1 shows the results of the multiply accumulate in each cell after each clock. The coefficient sequence, Cn, enters the DF on the left and moves from left to right through the cells. The data sample sequence, Xn, enters the DF from the top, with each cell receiving the same sample simultaneously. Each cell accumulates the sum-of-products for one output point. Four sums-of-products are calculated simultaneously, but staggered in time so that a new output is available every system clock.

Detailed operation of the DF to perform a basic 4 tap, 8 bit coefficient, 8 bit data, 30MHz FIR filter is best understood by observing the schematic (Figure 3) and timing diagram

TABLE 1. 25MHz, 4 TAP FIR FILTER SEQUENCE



CLK	CELL 0	CELL 1	CELL 2	CELL 3	SUM/CLR
0	$C_3 \times X_0$	0	0	0	-
1	$+C_2 \times X_1$	$C_3 \times X_1$	0	0	-
2	$+C_1 \times X_2$	$+C_2 \times X_2$	$C_3 \times X_2$	0	-
3	$+C_0 \times X_3$	$+C_1 \times X_3$	$+C_2 \times X_3$	$C_3 \times X_3$	Cell 0 (Y_3)
4	$C_3 \times X_4$	$+C_0 \times X_4$	$+C_1 \times X_4$	$+C_2 \times X_4$	Cell 1 (Y_4)
5	$+C_2 \times X_5$	$C_3 \times X_5$	$+C_0 \times X_5$	$+C_1 \times X_5$	Cell 2 (Y_5)
6	$+C_1 \times X_6$	$+C_2 \times X_6$	$C_3 \times X_6$	$+C_0 \times X_6$	Cell 3 (Y_6)
7	$+C_0 \times X_7$	$+C_1 \times X_7$	$+C_2 \times X_7$	$C_3 \times X_7$	Cell 0 (Y_7)

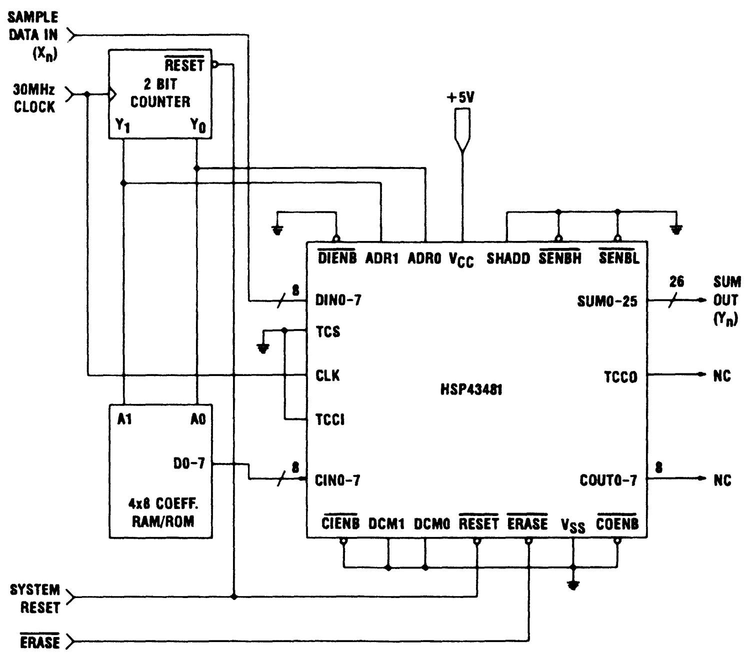


FIGURE 3. 30MHz, 4 TAP FIR FILTER APPLICATION SCHEMATIC

(Figure 4). The internal pipeline length of the DF is four (4) clock cycles, corresponding to the register levels CREG (or XREG), MREG0, MREG1, and TREG (Figures 1 and 2). Therefore, the delay from presentation of data and coefficients at the DIN0-7 and CIN0-7 inputs to a sum appearing at the SUM0-25 output is:

k + Td where

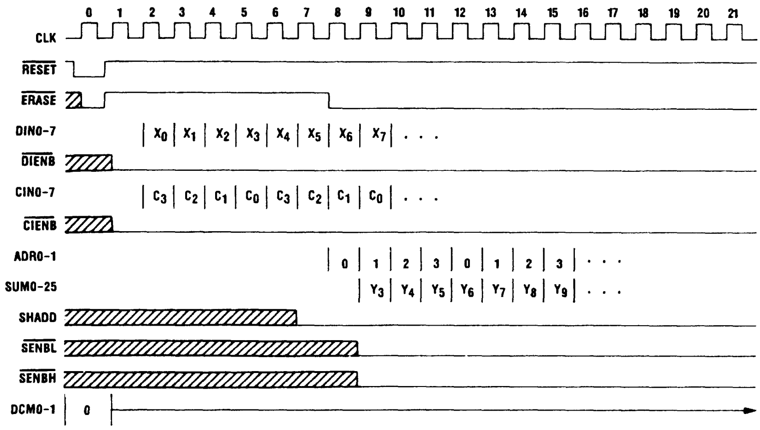
k = filter length

Td = 4, the internal pipeline delay of DF

After the pipeline has filled, a new output sample is available every clock. The delay to last sample output from last sample input is Td.

The output sums, Y(n), shown in the timing diagram are derived from the sum-of-products equation:

$Y(n) = C(0) \times X(n) + C(1) \times X(n-1) + C(2) \times X(n-2) + C(3) \times X(n-3)$



$$Y_N = \sum_{K=0}^{3} C_K \times X_{N-K}$$

FIGURE 4. 30MHz 4 TAP FILTER TIMING

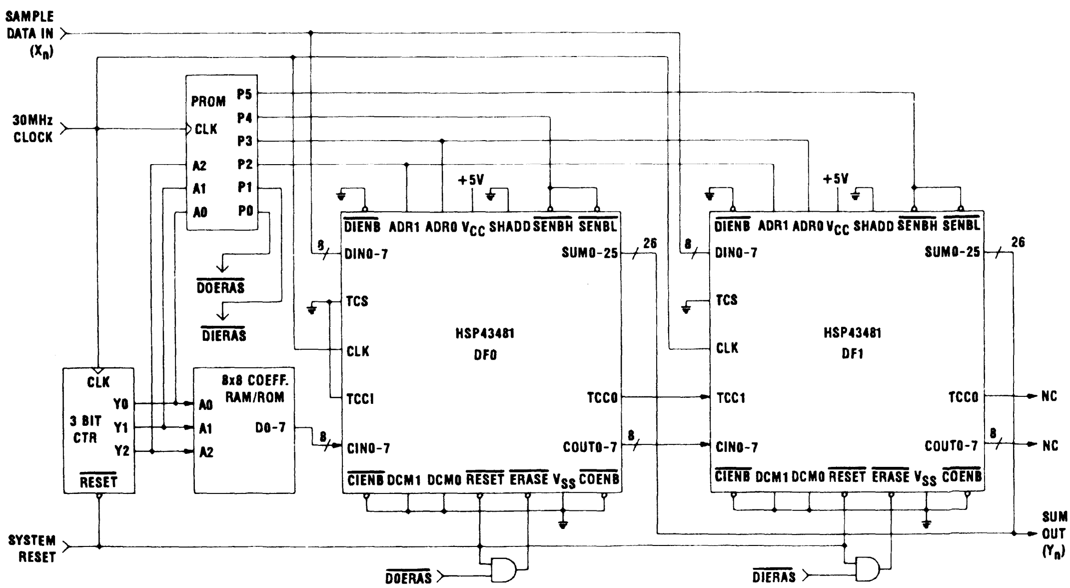


FIGURE 5. 30MHz 8 TAP FILTER USING TWO CASCADED HSP43481s

Extended FIR Filter Length

Filter lengths greater than four taps can be created by either cascading together multiple DFs or "reusing" a single DF. Using multiple devices, an FIR filter of over 1024 taps can be constructed to operate at a 30MHz sample rate. Using a single DF clocked at 30MHz, an FIR filter of over 1024 taps can be constructed to operate at less than a 30MHz sample rate. Combinations of these two techniques are also possible.

Cascade Configuration

To design a filter length L > 4, L/4 DFs are cascaded by connecting the COUT0-7 outputs of the (i)th DF to the CIN0-7 inputs of the (i + 1)th DF. The DIN0-7 inputs and SUM0-25 outputs of all the DFs are slso tied together. A specific example of two cascaded DFs illustrates the technique (Figure 5). Timing (Figure 6) is similar to the simple 4 tap FIR, except the $\overline{\text{ERASE}}$ and $\overline{\text{SENBL}}/\overline{\text{SENBH}}$ signals must be enabled independently of the two DFs in order to clear the correct accumulators and enable the SUM0-25 output signals at the proper times.

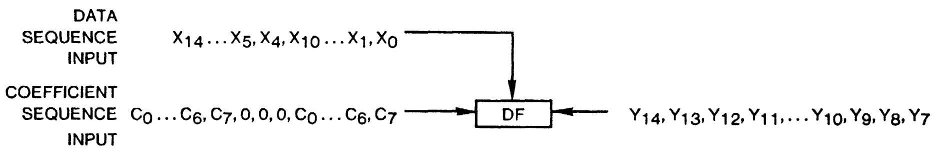
Single DF Configuration

Using a DF, a filter of length L > 4 can be constructed by processing in L/4 passes as illustrated in Table 2 for an 8 tap FIR. Each pass is composed of Tp = 7+L cycles and computes four output samples. In pass i, the samples with indices i x 4 to i x 4 + (L+2) enter the DIN0-7 inputs. The coefficients C_0-C_{L-1} enter the CIN0-7 inputs, followed by three zeros. As these zeros are entered, the result samples are output and the accumulators reset. Initial filling of the pipeline is not shown in this sequence table. Filter outputs can be put through a FIFO to even out the sample rate.

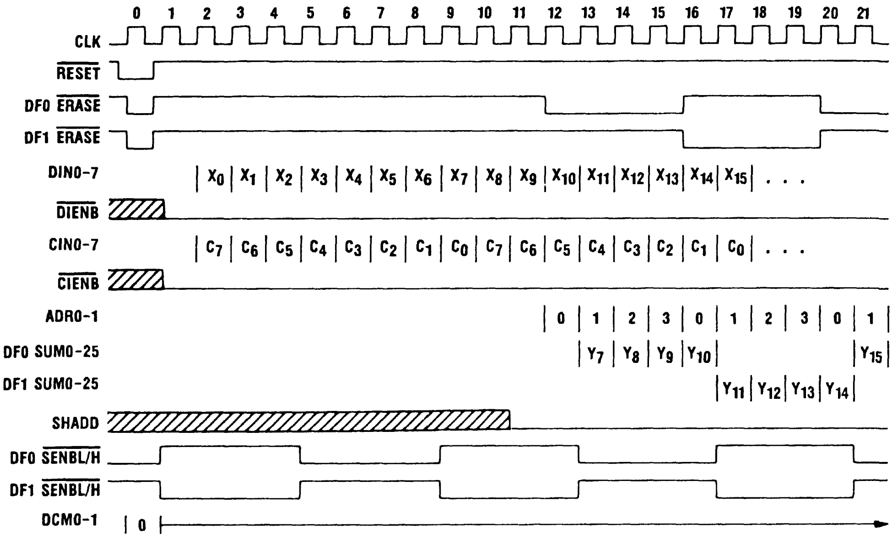
Extended Coefficient And Data Sample Word Size

The sample and coefficient word size can be extended by utilizing several DFs in parallel to get the maximum sample rate or a single DF with resulting lower sample rates. The technique is to compute partial products of 8x8 and combine these partial products by shifting and adding to obtain the final result. The shifting and adding can be accomplished with external adders (for full speed) or with the DFs shift-and-add mechanism contained in its output stage (at reduced speed).

TABLE 2. 8 TAP FIR FILTER SEQUENCE USING SINGLE DF



CLK	CELL 0	CELL 1	CELL 2	CELL 3	SUM/CLR
0	$C_7 \times X_0$	0	0	0	-
1	$+C_6 \times X_1$	$C_7 \times X_1$	0	0	-
2	$+C_5 \times X_2$	$+C_6 \times X_2$	$C_7 \times X_2$	0	-
3	$+C_4 \times X_3$	$+C_5 \times X_3$	$+C_6 \times X_3$	$C_7 \times X_3$	-
4	$+C_3 \times X_4$	$+C_4 \times X_4$	$+C_5 \times X_4$	$+C_6 \times X_4$	-
5	$+C_2 \times X_5$	$+C_3 \times X_5$	$+C_4 \times X_5$	$+C_5 \times X_5$	-
6	$+C_1 \times X_6$	$+C_2 \times X_6$	$+C_3 \times X_6$	$+C_4 \times X_6$	-
7	$+C_0 \times X_7$	$+C_1 \times X_7$	$+C_2 \times X_7$	$+C_3 \times X_7$	Cell 0 (Y_7)
8	0	$+C_0 \times X_8$	$+C_1 \times X_8$	$+C_2 \times X_8$	Cell 1 (Y_8)
9	0	0	$+C_0 \times X_9$	$+C_1 \times X_9$	Cell 2 (Y_9)
10	0	0	0	$+C_0 \times X_{10}$	Cell 3 (Y_{10})
11	$C_7 \times X_4$	0	0	0	-
12	$+C_6 \times X_5$	$C_7 \times X_5$	0	0	-
13	$+C_5 \times X_6$	$+C_6 \times X_6$	$C_7 \times X_6$	0	-
14	$+C_4 \times X_7$	$+C_5 \times X_7$	$+C_6 \times X_7$	$C_7 \times X_7$	-
15	$+C_3 \times X_8$	$+C_4 \times X_8$	$+C_5 \times X_8$	$+C_6 \times X_8$	-
16	$+C_2 \times X_9$	$+C_3 \times X_9$	$+C_4 \times X_9$	$+C_5 \times X_9$	-
17	$+C_1 \times X_{10}$	$+C_2 \times X_{10}$	$+C_3 \times X_{10}$	$+C_4 \times X_{10}$	-
18	$+C_0 \times X_{11}$	$+C_1 \times X_{11}$	$+C_2 \times X_{11}$	$+C_3 \times X_{11}$	Cell 0 (Y_{11})
19	0	$+C_0 \times X_{12}$	$+C_1 \times X_{12}$	$+C_2 \times X_{12}$	Cell 1 (Y_{12})
20	0	0	$+C_0 \times X_{13}$	$+C_1 \times X_{13}$	Cell 2 (Y_{13})
21	0	0	0	$+C_0 \times X_{14}$	Cell 3 (Y_{14})



$$Y_N = \sum_{K=0}^{7} C_K \times X_{N-K}$$

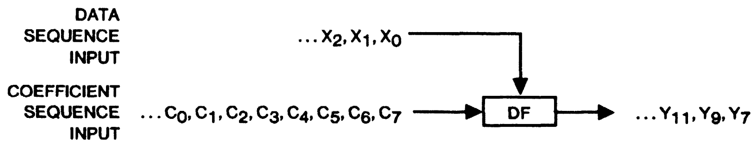
FIGURE 6. 30MHz 8 TAP FIR FILTER TIMING

Decimation/Resampling

The HSP43481 provides a mechanism for decimating by factors of 2, 3 or 4. From the DF filter cell block diagram (Figure 1), note the three D registers and two multiplexers in the coefficient pass through the cell. These allow the coefficients to be delayed by 1, 2 or 3 clocks through the cell. The sequence table (Table 3) for a decimate-by-two filter illustrates the technique.

Detailed timing for a 30MHz input sample rate, 15MHz output sample rate (i.e., decimate-by-two), 8 tap FIR filter, including pipelining, is shown in Figure 7.

TABLE 3. 8 TAP DECIMATE-BY-TWO FIR FILTER SEQUENCE, 30MHz IN, 15MHz OUT



CLK	CELL 0	CELL 1	CELL 2	CELL 3	SUM/CLR
0	$C_7 \times X_0$	0			-
1	$+C_6 \times X_1$	0			-
2	$+C_5 \times X_2$	$C_7 \times X_2$			-
3	$+C_4 \times X_3$	$+C_6 \times X_3$			-
4	$+C_3 \times X_4$	$+C_5 \times X_4$	$C_7 \times X_4$		-
5	$+C_2 \times X_5$	$+C_4 \times X_5$	$+C_6 \times X_5$		-
6	$+C_1 \times X_6$	$+C_3 \times X_6$	$+C_5 \times X_6$	$+C_7 \times X_6$	-
7	$+C_0 \times X_7$	$+C_2 \times X_7$	$+C_4 \times X_7$	$+C_6 \times X_7$	Cell 0 (Y_7)
8	$C_7 \times X_8$	$+C_1 \times X_8$	$+C_3 \times X_8$	$+C_5 \times X_8$	Cell 0 (Y_7)
9	$+C_6 \times X_9$	$+C_0 \times X_9$	$+C_2 \times X_9$	$+C_4 \times X_9$	Cell 1 (Y_9)
10	$+C_5 \times X_{10}$	$C_7 \times X_{10}$	$+C_1 \times X_{10}$	$+C_3 \times X_{10}$	Cell 1 (Y_9)
11	$+C_4 \times X_{11}$	$+C_6 \times X_{11}$	$+C_0 \times X_{11}$	$+C_2 \times X_{11}$	Cell 2 (Y_{11})
12	$+C_3 \times X_{12}$	$+C_5 \times X_{12}$	$C_7 \times X_{12}$	$+C_1 \times X_{12}$	Cell 2 (Y_{11})
13	$+C_2 \times X_{13}$	$+C_4 \times X_{13}$	$+C_6 \times X_{13}$	$+C_0 \times X_{13}$	Cell 3 (Y_{13})
14	$+C_1 \times X_{14}$	$+C_3 \times X_{14}$	$+C_5 \times X_{14}$	$C_7 \times X_{14}$	Cell 3 (Y_{13})
15	$+C_0 \times X_{15}$	$+C_2 \times X_{15}$	$+C_4 \times X_{15}$	$+C_6 \times X_{15}$	Cell 0 (Y_{15})

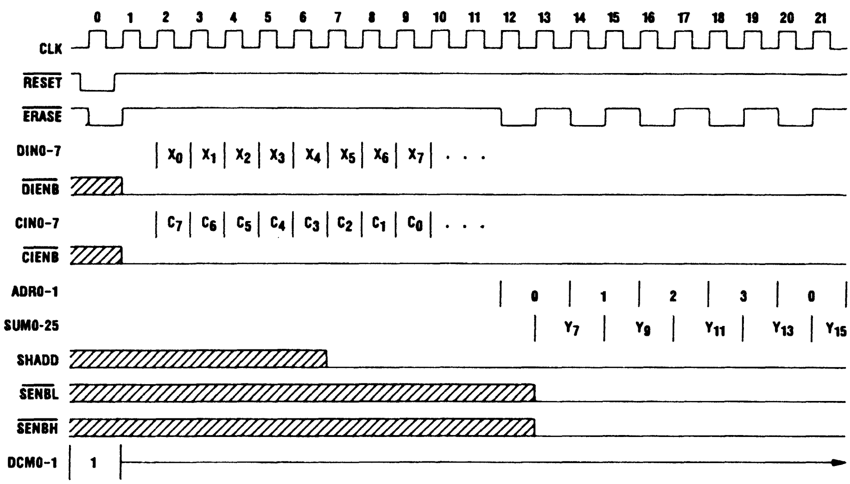


FIGURE 7. 8 TAP DECIMATE-BY-TWO FIR FILTER TIMING, 30MHz IN, 15MHz OUT

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output Voltage .... GND -0.5V to V_{CC} +0.5V
Storage Temperature .... -65°C to +150°C
ESD .... Class 1
Maximum Package Power Dissipation at 70°C .... 1.9W (PLCC), 2.6W (PGA)
θ_{jc} .... 15.0W/°C (PLCC), 9.92W/°C (PGA)
θ_{ja} .... 43.0W/°C (PLCC), 38.44W/°C (PGA)
Gate Count 9371
Junction Temperature .... 150°C (PLCC), 175°C (PGA)
Lead Temperature (Soldering 10s) .... 300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... 5V ±5%
Operating Temperature Ranges .... 0°C to +70°C

D.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
I_{CCOP}	Power Supply Current	-	110	mA	V_{CC} = Max CLK Frequency 20MHz Note 1, Note 3
I_{CCSB}	Standby Power Supply Current	-	500	µA	V_{CC} = Max, Note 3
I_I	Input Leakage Current	-10	10	µA	V_{CC} = Max, Input = 0V or V_{CC}
I_O	Output Leakage Current	-10	10	µA	V_{CC} = Max, Input = 0V or V_{CC}
V_{IH}	Logical One Input Voltage	2.0	-	V	V_{CC} = Max
V_{IL}	Logical Zero Input Voltage		0.8	V	V_{CC} = Min
V_{OH}	Logical One	2.6	-	V	I_{OH} = -400µA, V_{CC} = Min
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} = 2mA, V_{CC} = Min
V_{IHC}	Clock Input High	3.0	-	V	V_{CC} = Max
V_{ILC}	Clock Input Low	-	0.8	V	V_{CC} = Min
C_{IN}	Input Capacitance PLCC PGA	- -	10 15	pF pF	CLK Frequency 1MHz All Measurements Referenced to GND T_A = +25°C Note 2
C_{OUT}	Output Capacitance PLCC PGA	- -	10 15	pF pF	

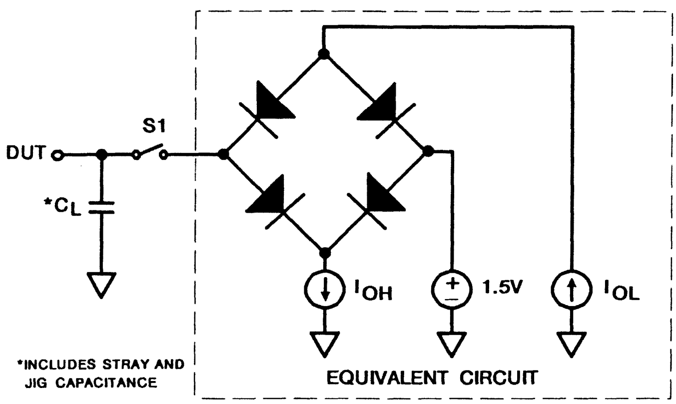
NOTES:
1. Operating supply current is proportional to frequency. Typical rating is 5.5mA/MHz.
2. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
3. Output load per test circuit and C_L = 40pF.

A.C. Electrical Specifications V_{CC} = +4.75V to +5.25V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	-20 (20MHz)		-25 (25.6MHz)		-30 (30MHz)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
T_{CP}	Clock Period	50	-	39	-	33	-	ns	
T_{CL}	Clock Low	20	-	16	-	13	-	ns	
T_{CH}	Clock High	20	-	16	-	13	-	ns	
T_{IS}	Input Setup	16	-	14	-	13	-	ns	
T_{IH}	Input Hold	0	-	0	-	0	-	ns	
T_{ODC}	CLK to Coefficient Output Delay	-	26	-	22	-	19	ns	
T_{OED}	Output Enable Delay	-	20	-	15	-	15	ns	
T_{ODD}	Output Disable Delay	-	20	-	15	-	15	ns	Note 1
T_{ODS}	CLK to SUM Output Delay	-	30	-	26	-	21	ns	
T_{OR}	Output Rise	-	6	-	6	-	6	ns	Note 1
T_{OF}	Output Fall	-	6	-	6	-	6	ns	Note 1

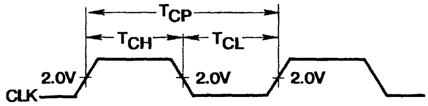
NOTE: 1. Controlled by design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

Test Load Circuit

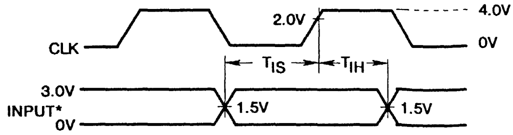


Switch S1 Open for I_{CCSB} and I_{CCOP} Tests

Waveforms

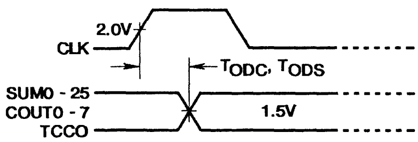


CLOCK AC PARAMETERS

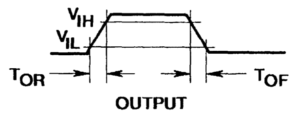


* Input includes: DIN0-7, CIN0-7, DIENB, CIENB, ERASE, RESET, DCM0-1, ADR0-1, TCS, TCCI, SHADD

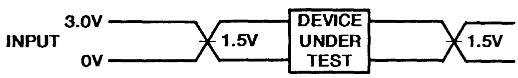
INPUT SETUP AND HOLD



SUM0-25, COUT0-7, TCCO OUTPUT DELAYS



RISE AND FALL TIMES



A.C. Testing: Inputs are driven at 3.0V for a Logic "1" and 0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a Logic "1" and "0". CLK is driven at 4.0V and 0.0V and measured at 2.0V.

A.C. TESTING INPUT, OUTPUT WAVEFORM

HARRIS SEMICONDUCTOR

HSP43481/883

January 1994

Digital Filter

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **0MHz to 25.6MHz Sample Rate**
- **Four Filter Cells**
- **8-Bit Coefficients and Signal Data**
- **Low Power CMOS Operation**
  - **I_{CCSB} = 500μA Maximum**
  - **I_{CCOP} = 110μA Maximum at 20MHz**
- **26-Bit Accumulator Per Stage**
- **Filter Lengths Up To 1032 Taps**
- **Expandable Coefficient Size, Data Size and Filter Length**
- **Decimation by 2, 3 or 4**

Applications

- **1-D and 2-D FIR Filters**
- **Radar/Sonar**
- **Adaptive Filters**
- **Echo Cancellation**
- **Complex Multiply-Add**
- **Sample Rate Converters**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43481GM-20/883	-55°C to +125°C	68 Lead PGA
HSP43481GM-25/883	-55°C to +125°C	68 Lead PGA

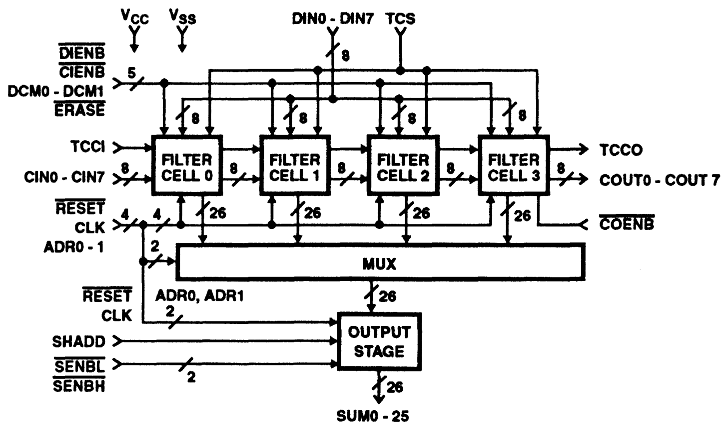
Description

The HSP43481/883 is a video-speed Digital Filter (DF) designed to efficiently implement vector operations such as FIR digital filters. It is comprised of four filter cells cascaded internally and a shift-and- add output stage, all in a single integrated circuit. Each filter cell contains an 8 x 8 multiplier, three decimation registers and a 26-bit accumulator which can add the contents of any filter cell accumulator to the output stage accumulator shifted right by eight-bits. The HSP43481/883 has a maximum sample rate of 25.6MHz. The effective multiply-accumulate (MAC) rate is 102MHz.

The HSP43481/883 can be configured to process expanded coefficient and word sizes. Multiple devices can be cascaded for larger filter lengths without degrading the sample rate or a single device can process larger filter lengths at less than 25.6MHz with multiple passes. The architecture permits processing filter lengths of over 1000 taps with the guarantee of no overflows. In practice, most filter coefficients are less than 1.0, making even larger filter lengths possible. The HSP43481/883 provides for unsigned or two's complement arithmetic, independently selectable for coefficients and signal data.

Each DF filter cell contains three resampling or decimation registers which permit output sample rate reduction at rates of $^1/_2$, $^1/_3$ or $^1/_4$ the input sample rate. These registers also provide the capability to perform 2-D operations such as N x N spatial correlations/convolutions for image processing applications.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2450.3**

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output Voltage Applied .... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering, Ten Seconds) .... +300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
Ceramic PGA Package .... 38.44°C/W 9.92°C/W
Maximum Package Power Dissipation at +125°C
Ceramic PGA Package .... 1.30 Watt
Gate Count .... 9370 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range .... -55°C to +125°C

TABLE 1. HSP43481/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA V_{CC} = 4.5V (Note 1)	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC} = 4.5V (Note 1)	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	0.4	V
Input Leakage Current	I_I	$V_{IN} = V_{CC}$ or GND V_{CC} = 5.5V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-10	+10	µA
Output Leakage Current	I_O	$V_{OUT} = V_{CC}$ or GND V_{CC} = 5.5V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-10	+10	µA
Clock Input High	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	0.8	V
Standby Power Supply Current	I_{CCSB}	$V_{IN} = V_{CC}$ or GND V_{CC} = 5.5 V, Outputs Open	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 20.0MHz V_{CC} = 5.5V (Note 2)	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	110.0	mA
Functional Test	FT	(Note 3)	7, 8	$-55^oC \leq T_A \leq +125^oC$	-	-	

NOTES: 1. Interchanging of force and sense conditions is permitted.

2. Operating Supply Current is proportional to frequency, typical rating is 5.5mA/MHz.

3. Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, $V_{OH} \geq$ 1.5V, $V_{OL} \leq$ 1.5V, V_{IHC} = 3.4V and V_{ILC} = 0.4V.

TABLE 2. HSP43481/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	-20 (20MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
Clock Period	T_{CP}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	39	-	ns
Clock Low	T_{CL}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	16	-	ns
Clock High	T_{CH}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	16	-	ns
Input Setup	T_{IS}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	17	-	ns
Input Hold	T_{IH}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
CLK to Coefficient Output Delay	T_{ODC}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	24	-	20	ns
Output Enable Delay	T_{OED}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	20	-	15	ns
CLK to SUM Output Delay	T_{ODS}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	31	-	25	ns

NOTE: 1. A.C. Testing: V_{CC} = 4.5V and 5.5V. Inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a Logic "1" and "0". CLK is driven at 4.0V and 0V and measured at 2.0V.

TABLE 3. HSP43481/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	-20 (20MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	V_{CC}=Open, f=1MHz All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	15	-	15	pF
Output Capacitance	COUT		1	$T_A = +25^oC$	-	15	-	15	pF
Output Disable Delay	T_{ODD}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	20	-	15	ns
Output Rise Time	T_{OR}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	7	-	6	ns
Output Fall Time	T_{OF}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	7	-	6	ns

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. Loading is as specified in the test load circuit, C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Burn-In Circuit

	1	2	3	4	5	6	7	8	9	10	11
L		COUT7	COUT5	COUT3	COUT1	COUT0	CLK	ADDR1	ADDR0	SUM25	
K	TCCO	COENB	COUT6	COUT4	COUT2	SHADD	DCM1	DCM0	SENBH	SUM24	SUM23
J	ERASE	V_{CC}								SUM21	SUM22
H	RESET	DIENB								SUM19	SUM20
G	TCS	DIN7								SUM17	SUM18
F	DIN5	DIN6								SUM15	SUM16
E	DIN3	DIN4								V_{SS}	SUM14
D	DIN1	DIN2								SUM12	SUM13
C	DIN0	CIENB								SUM10	SUM11
B	TCCI	CIN6	CIN4	CIN2	CIN0	SUM0	SUM2	SUM4	SUM6	SUM8	SUM9
A		CIN7	CIN5	CIN3	CIN1	SENBL	SUM1	SUM3	SUM5	SUM7	

68 LEAD
PIN GRID ARRAY
BOTTOM VIEW

PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
K1	TCCO	$V_{CC}/2$	C2	$\overline{\text{CIENB}}$	F10	B6	SUM0	$V_{CC}/2$	H10	SUM19	$V_{CC}/2$
J1	$\overline{\text{ERASE}}$	F10	B2	CIN6	F6	A6	$\overline{\text{SENBL}}$	F10	G10	SUM17	$V_{CC}/2$
H1	$\overline{\text{RESET}}$	F11	A2	CIN7	F7	L7	CLK	F0	F10	SUM15	$V_{CC}/2$
G1	TCS	F7	L3	COUT5	$V_{CC}/2$	K7	DCM1	F6	E10	V_{SS}	GND
F1	DIN5	F5	K3	COUT6	$V_{CC}/2$	B7	SUM2	$V_{CC}/2$	D10	SUM12	$V_{CC}/2$
E1	DIN3	F3	B3	CIN4	F4	A7	SUM1	$V_{CC}/2$	C10	SUM10	$V_{CC}/2$
D1	DIN1	F1	A3	CIN5	F5	L8	ADDR1	F1	B10	SUM8	$V_{CC}/2$
C1	DIN0	F0	L4	COUT3	$V_{CC}/2$	K8	DCM0	F5	A10	SUM7	$V_{CC}/2$
B1	TCCI	F8	K4	COUT4	$V_{CC}/2$	B8	SUM4	$V_{CC}/2$	K11	SUM23	$V_{CC}/2$
L2	COUT7	$V_{CC}/2$	B4	CIN2	F2	A8	SUM3	$V_{CC}/2$	J11	SUM22	$V_{CC}/2$
K2	$\overline{\text{COENB}}$	F10	A4	CIN3	F3	L9	ADDR0	F0	H11	SUM20	$V_{CC}/2$
J2	V_{CC}	V_{CC}	L5	COUT1	$V_{CC}/2$	K9	$\overline{\text{SENBH}}$	F10	G11	SUM18	$V_{CC}/2$
H2	$\overline{\text{DIENB}}$	F10	K5	COUT2	$V_{CC}/2$	B9	SUM6	$V_{CC}/2$	F11	SUM16	$V_{CC}/2$
G2	DIN7	F8	B5	CIN0	F0	A9	SUM5	$V_{CC}/2$	E11	SUM14	$V_{CC}/2$
F2	DIN6	F6	A5	CIN1	F1	L10	SUM25	$V_{CC}/2$	D11	SUM13	$V_{CC}/2$
E2	DIN4	F4	L6	COUT0	$V_{CC}/2$	K10	SUM24	$V_{CC}/2$	C11	SUM11	$V_{CC}/2$
D2	DIN2	F2	K6	SHADD	F9	J10	SUM21	$V_{CC}/2$	B11	SUM9	$V_{CC}/2$

NOTES:
1. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5 ±0.5V.
4. 0.1μF (min) capacitor between V_{CC} and GND per position.
5. F0 = 100KHz ±10%, F1 = F0/2, F2 = F1/2 . . . . . , F11 = F10/2, 40% - 60% Duty Cycle.
6. Input voltage limits: V_{IL} = 0.8V max., V_{IH} = 4.5V ±10%.

Metallization Topology

DIE DIMENSIONS:
253 x 230 x 19 ±1 mils

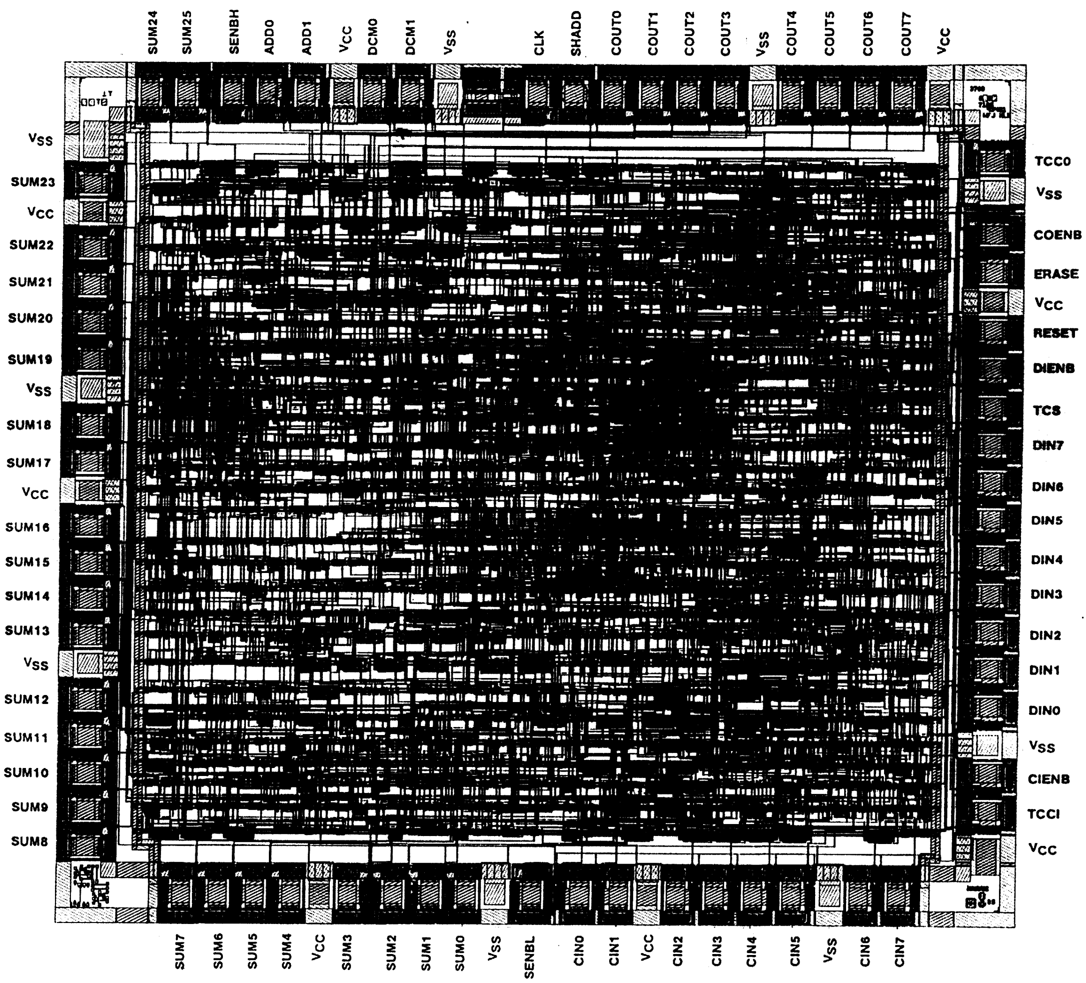
METALLIZATION:
Type: Si - Al or Si - Al - Cu
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:
$1.2 \times 10^5 A/cm^2$

Metallization Mask Layout

HSP43481/883



HARRIS SEMICONDUCTOR

HSP43881

January 1994

Digital Filter

Features

- Eight Filter Cells
- 0 to 30MHz Sample Rate
- 8-Bit Coefficients and Signal Data
- 26-Bit Accumulator Per Stage
- Filter Lengths Over 1000 Taps
- Expandable Coefficient Size, Data Size and Filter Length
- Decimation by 2, 3 or 4

Applications

- 1-D and 2-D FIR Filters
- Radar/Sonar
- Adaptive Filters
- Echo Cancellation
- Complex Multiply-Add
- Sample Rate Converters

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43881JC-20	0°C to +70°C	84 Lead PLCC
HSP43881JC-25	0°C to +70°C	84 Lead PLCC
HSP43881JC-30	0°C to +70°C	84 Lead PLCC
HSP43881GC-20	0°C to +70°C	85 Lead PGA
HSP43881GC-25	0°C to +70°C	85 Lead PGA
HSP43881GC-30	0°C to +70°C	85 Lead PGA

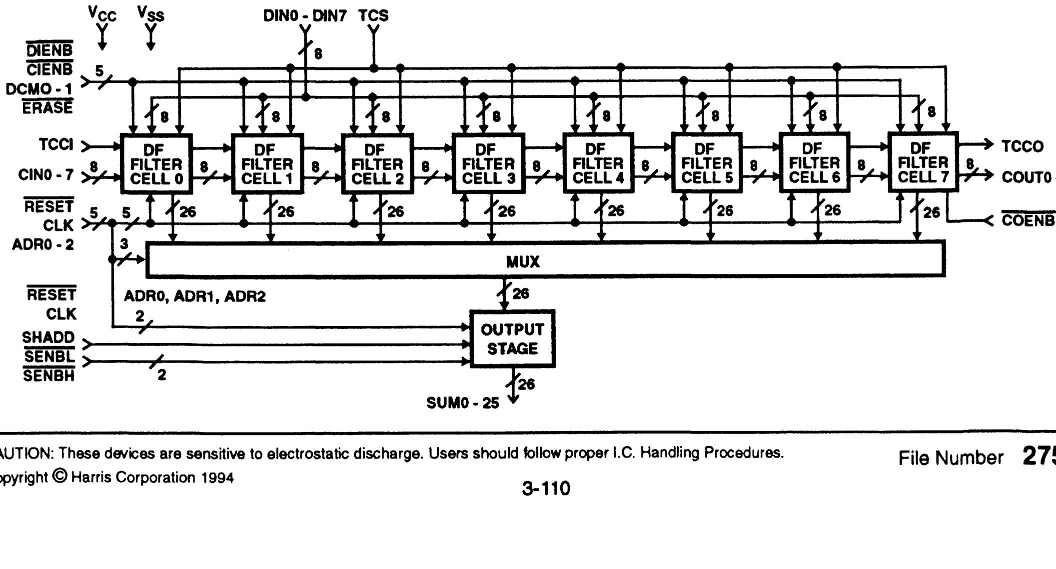
Description

The HSP43881 is a video speed Digital Filter (DF) designed to efficiently implement vector operations such as FIR digital filters. It is comprised of eight filter cells cascaded internally and a shift and add output stage, all in a single integrated circuit. Each filter cell contains a 8 x 8-bit multiplier, three decimation registers and a 26-bit accumulator. The output stage contains an additional 26-bit accumulator which can add the contents of any filter cell accumulator to the output stage accumulator shifted right by 8-bits. The HSP43881 has a maximum sample rate of 30MHz. The effective multiply accumulate (mac) rate is 240MHz.

The HSP43881 DF can be configured to process expanded coefficient and word sizes. Multiple DFs can be cascaded for larger filter lengths without degrading the sample rate or a single DF can process larger filter lengths at less than 30MHz with multiple passes. The architecture permits processing filter lengths of over 1000 taps with the guarantee of no overflows. In practice, most filter coefficients are less than 1.0, making even larger filter lengths possible. The DF provides for 8-bit unsigned or two's complement arithmetic, independently selectable for coefficients and signal data.

Each DF filter cell contains three resampling or decimation registers which permit output sample rate reduction at rates of $^1/_2$, $^1/_3$ or $^1/_4$ the input sample rate. These registers also provide the capability to perform 2-D operations such as matrix multiplication and NxN spatial correlations/convolutions for image processing applications.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

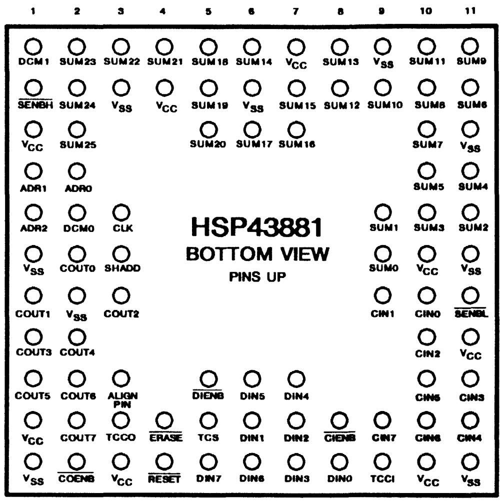
File Number 2758.3

Pinouts

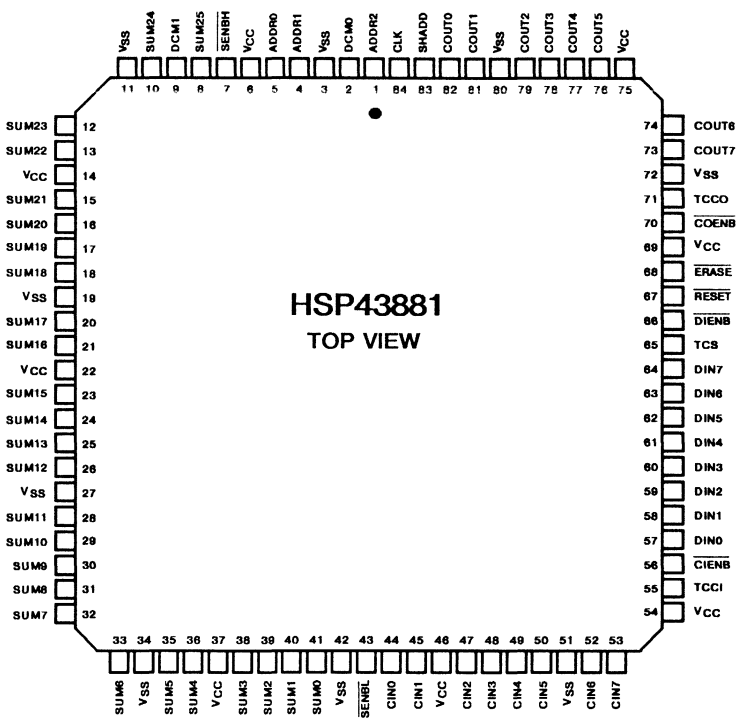
85 PIN GRID ARRAY (PGA)

	1	2	3	4	5	6	7	8	9	10	11
A	V_{SS}	COENB	V_{CC}	RESET	DIN7	DIN6	DIN3	DIN0	TCCI	V_{CC}	V_{SS}
B	V_{CC}	COUT7	TCCO	ERASE	TCS	DIN1	DIN2	CIENB	CIN7	CIN6	CIN4
C	COUT5	COUT6	ALIGN PIN		DIENB	DIN5	DIN4			CIN5	CIN3
D	COUT3	COUT4								CIN2	V_{CC}
E	COUT1	V_{SS}	COUT2						CIN1	CIN0	SENBL
F	V_{SS}	COUT0	SHADD						SUM0	V_{CC}	V_{SS}
G	ADR2	DCM0	CLK						SUM1	SUM3	SUM2
H	ADR1	ADR0								SUM5	SUM4
J	V_{CC}	SUM25			SUM20	SUM17	SUM16			SUM7	V_{SS}
K	SENBH	SUM24	V_{SS}	V_{CC}	SUM19	V_{SS}	SUM15	SUM12	SUM10	SUM8	SUM6
L	DCM1	SUM23	SUM22	SUM21	SUM18	SUM14	V_{CC}	SUM13	V_{SS}	SUM11	SUM9

HSP43881
TOP VIEW
PINS DOWN



84 LEAD PLCC PACKAGE



NOTE: An overbar on a signal name represents an active LOW signal.

3

1D FILTERS

Pin Description

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
V_{CC}	A3, A10, B1, D11, F10, J1, K4, L7		+5V Power Supply Input
V_{SS}	A1, A11, E2, F1, E11, H11, K3, K6, L9		Power Supply Ground Input
CLK	G3	I	The CLK input provides the DF system sample clock. The maximum clock frequency is is 30MHz.
DIN0-7	A5-8, B6-7, C6-7	I	These eight inputs are the data sample input bus. Eight bit data samples are synchronously loaded through these pins to the X register of each filter cell simultaneously. The $\overline{\text{DIENB}}$ signal enables loading, which is synchronous on the rising edge of the clock signal.
TCS	B5	I	The TCS input determines the number system interpretation of the data input samples on pins DIN0-7 as follows: TCS = Low → Unsigned Arithmetic TCS = High → Two's Complement Arithmetic The TCS signal is synchronously loaded into the X register in the same way as the DIN0-7 inputs.
$\overline{\text{DIENB}}$	C5	I	A low on this enables the data sample input bus (DIN0-7) to all the filter cells. A rising edge of the CLK signal occurring while $\overline{\text{DIENB}}$ is low will load the X register of every filter cell with the 8 bit value present on DIN0-7. A high on this input forces all the bits of the data sample input bus to zero; a rising CLK edge when $\overline{\text{DIENB}}$ is high will load the X register of every filter cell with all zeros. This signal is latched inside the DF, delaying its effect by one clock internal to the DF. Therefore, it must be low during the clock cycle immediately preceding presentation of the desired data on the DIN0-7 inputs. Detailed operation is shown in later timing diagrams.
CIN0-7	B9-11, C10-11, D10, E9-10	I	These eight inputs are used to input the 8 bit coefficients. The coefficients are synchronously synchronously loaded into the C register of filter CELL 0 if a rising edge of CLK occurs while $\overline{\text{CIENB}}$ is low. The $\overline{\text{CIENB}}$ signal is delayed by one clock as discussed below.
TCCI	A9	I	The TCCI input determines the number system interpretation of the coefficient inputs on pins CIN0-7 as follows: TCCI = LOW → Unsigned Arithmetic TCCI = HIGH → Two's Complement Arithmetic The TCCI signal is synchronously loaded into the C register in the same way as the CIN0-7 inputs.
$\overline{\text{CIENB}}$	B8	I	A low on this input enable the C register of every filter cell and the D registers (decimation) of every filter cell according to the state of the DCM0-1 inputs. A rising edge of the CLK signal occurring while $\overline{\text{CIENB}}$ is low will load the C register and appropriate D registers with the coefficient data present at their inputs. This privides the mechanism for shifting the coefficients from cell to cell through the device. A high on this input freezes the contents of the C register and the D registers, ignoring the CLK signal. This signal is latched and delayed by one clock internal to the DF. Therefore, it must be low during the clock cycle immediately preceding presentation of the desired coefficient on the CIN0-7 inputs. Detailed operation is shown in the Timing Diagrams section.
COUT0-7	B2, C1-2, D1-2 E1, E3, F2	O	These eight three-state outputs are used to output the 8 bit coefficients from filter cell 7. These outputs are enabled by the $\overline{\text{COENB}}$ signal low. These outputs may be tied to the CIN0-7 inputs of the same DF to recirculate the coefficients, or they may be tied to the CIN0-7 inputs of another DF to cascade DFs for longer filter lengths.
TCCO	B3	O	The TCCO three-state output determines the number system representation of the coefficients output on COUT0-7. It tracks the TCCI signal to this same DF. It should be tied to the TCCI input of the next DF in a cascade of DFs for increased filter lengths. This signal is enabled by $\overline{\text{COENB}}$ low.
$\overline{\text{COENB}}$	A2	I	A low on the $\overline{\text{COENB}}$ input enables the COUT0-7 and the TCCO output. A high on this input places all these outputs in their high impedance state.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	NAME FUNCTION
DCM0-1	G2, L1	I	These two inputs determine the use of the internal decimation registers as follows: DCM1 DCM0 Decimation Function 0 0 Decimation registers not used 0 1 One decimation register is used 1 0 Two decimation registers are used 1 1 Three decimation registers are used The coefficients pass from cell to cell at a rate determined by the number of decimation registers used. When no decimation registers are used, coefficients move from cell to cell on each clock. When one decimation register is used, coefficients move from cell to cell on every other clock, etc. These signals are latched and delayed by one clock internal to the DF.
SUM0-25	J2, J5-8, J10, K2, K5-11, L2-6, L8, L10-11	O	These 26 three-state outputs are used to output the results of the internal filter cell computations. Individual filter cell results or the result of the shift-and-add output stage can be output. If an individual filter cell result is to be output, the ADR0-2 signals select the filter cell result. The SHADD signal determines whether the selected filter cell result or the output stage adder result is output. The signals $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ enable the most significant and least significant bits of the SUM0-25 result, respectively. Both $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ may be enabled simultaneously if the system has a 26 bit or larger bus. However, individual enables are provided to facilitate use with a 16 bit bus.
$\overline{\text{SENBH}}$	K1	I	A low on this input enables result bits SUM16-25. A high on this input places these bits in their high impedance state.
$\overline{\text{SENBL}}$	E11	I	A low on this input enables result bits SUM0-15. A high on this input places these bits in their high impedance state.
ADR0-2	G1, H1-2	I	These inputs select the one cell whose accumulator will be read through the output bus (SUM0-25) or added to the output stage accumulator. They also determine which accumulator will be cleared when $\overline{\text{ERASE}}$ is low. For selection of which accumulator to read through the output bus (SUM0-25) or which to add of the output stage accumulator, these inputs are latched in the DF and delayed by one clock internal to the device. If the ADR0-2 lines remain at the same address for more than one clock, the output at SUM0-25 will not change to reflect any subsequent accumulator updates in the addressed cell. Only the result available during the first clock, when ADR0-1 selects the cell, will be output. This does not hinder normal operation since the ADR0-1 lines are changed sequentially. This feature facilitates the interface with slow memories where the output is required to be fixed for more than one clock.
SHADD	F3	I	The SHADD input controls the activation of the shift-and-add operation in the output stage. This signal is latched in the DF and delayed by one clock internal to the device. A detailed explanation is given in the DF Output Stage section.
$\overline{\text{RESET}}$	A4	I	A low on this input synchronously clears all the internal registers, except the cell accumulators. It can be used with $\overline{\text{ERASE}}$ to also clear all the accumulators simultaneously. This signal is latched in the DF and delayed by one clock internal to the DF.
$\overline{\text{ERASE}}$	B4	I	A low on this input synchronously clears the cell accumulator selected by the ADR0-1 signals. If $\overline{\text{RESET}}$ is also low simultaneously, all cell accumulators are cleared.
ALIGN PIN	C3		Used for aligning chip in socket or printed circuit board. Must be left as a no connect in circuit.

Functional Description

The Digital Filter Processor (DF) is composed of eight filter cells cascaded together and an output stage for combining or selecting filter cell outputs (See Block Diagram). Each filter cell contains a multiplier-accumulator and several registers (Figure 1). Each 8-bit coefficient is multiplied by a 8- bit data sample, with the result added to the 26-bit accumulator contents. The coefficient output of each cell is cascaded to the coefficient input of the next cell to its right.

DF Filter Cell

A 8-bit coefficient (CIN0-7) enters each cell through the C register on the left and exits the cell on the right as signals COUT0-7. With no decimation, the coefficient moves directly from the C register to the output, and is valid on the clock following its entrance. When decimation is selected the coefficient exit is delayed by 1, 2 or 3 clocks by passing through one or more decimation registers (D1, D2 or D3).

The combination of D registers through which the coefficient passes is determined by the state of DCM0 and DCM1. The output signals (COUT0-7) are connected to the CIN0-7 inputs of the next cell to its right. The $\overline{\text{COENB}}$ input signal enables the COUT0-7 outputs of the right most cell to the COUT0-7 pins of the device.

The C and D registers are enabled for loading by $\overline{\text{CIENB}}$. Loading is synchronous with CLK when $\overline{\text{CIENB}}$ is low. Note that $\overline{\text{CIENB}}$ is latched internally. It enables the register for loading after the next CLK following the onset of $\overline{\text{CIENB}}$ low. Actual loading occurs on the second CLK following the onset of $\overline{\text{CIENB}}$ low. Therefore $\overline{\text{CIENB}}$ must be low during the clock cycle immediately preceding presentation of the coefficient on the CIN0-7 inputs. In most basic FIR operations, $\overline{\text{CIENB}}$ will be low throughout the process, so this latching and delay sequence is only important during the initialization phase. When $\overline{\text{CIENB}}$ is high, the coefficients are frozen.

These registers are cleared synchronously under control of $\overline{\text{RESET}}$, which is latched and delayed exactly like $\overline{\text{CIENB}}$.

The output of the C register (C0-8) is one input to 8 x 8 multiplier.

The other input to the 8x8 multiplier comes from the output of the X register. This register is loaded with a data sample from the device input signals DIN0-7 discussed above. The X register is enabled for loading by $\overline{\text{DIENB}}$. Loading is synchronous with CLK when $\overline{\text{DIENB}}$ is low. Note that $\overline{\text{DIENB}}$ is latched internally. It enables the register for loading after the next CLK following the onset of $\overline{\text{DIENB}}$ low. Actual loading occurs on the second CLK following the onset of $\overline{\text{DIENB}}$ low; therefore, $\overline{\text{DIENB}}$ must be low during the clock cycle immediately preceding presentation of the data sample on the DIN0-7 inputs. In most basic FIR operations, $\overline{\text{DIENB}}$ will be low throughout the process, so this latching and delay sequence is only important during the initialization phase. When $\overline{\text{DIENB}}$ is high, the X register is loaded with all zeros.

The multiplier is pipelined and is modeled as a multiplier core followed by two pipeline registers, MREG0 and MREG1 (Figure 1). The multiplier output is sign extended and input as one operand of the 26-bit adder. The other adder operand is the output of the 26-bit accumulator. The adder output is loaded synchronously into both the accumulator and the TREG.

The TREG loading is disabled by the cell select signal, CELLn, where n is the cell number. The cell select is decoded from the ADR0-2 signals to generate the TREG load enable. The cell select is inverted and applied as the load enable to the TREG. Operation is such that the TREG is loaded whenever the cell is not selected. Therefore, TREG is loaded every clock except the clock following cell selection. The purpose of the TREG is to hold the result of a sum-of-products calculation during the clock when the accumulator is cleared to prepare for the next sum-of-products calculation. This allows continuous accumulation without wasting clocks.

The accumulator is loaded with the adder output every clock unless it is cleared. It is cleared synchronously in two ways. When $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ are both low, the accumulator is cleared along with all other registers on the device. Since $\overline{\text{ERASE}}$ and $\overline{\text{RESET}}$ are latched and delayed one clock internally, clearing occurs on the second CLK following the onset of both $\overline{\text{ERASE}}$ and $\overline{\text{RESET}}$ low.

The second accumulator clearing mechanism clears a single accumulator in a selected cell. The cell select signal, CELLn, decoded from ADR0-2 and the $\overline{\text{ERASE}}$ signal enable clearing of the accumulator on the next CLK.

The $\overline{\text{ERASE}}$ and $\overline{\text{RESET}}$ signals clear the DF internal registers and states as follows:

$\overline{\text{ERASE}}$	$\overline{\text{RESET}}$	CLEARING EFFECT
1	1	No clearing occurs, internal state remains same
1	0	$\overline{\text{RESET}}$ only active, all registers except accumulators are cleared, including the internal pipeline registers.
0	1	$\overline{\text{ERASE}}$ only active, the accumulator whose address is given by the ADR0-2 inputs is cleared.
0	0	Both $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ active, all accumulators as well as all other registers are cleared.

The DF Output Stage

The output stage consists of a 26-bit adder, 26-bit register, feedback multiplexer from the register to the adder, an output multiplexer and a 26-bit three-state driver stage (Figure 2).

The 26-bit output adder can add any filter cell accumulator result to the 18 most significant bits of the output buffer. This result is stored back in the output buffer. This operation takes place in one clock period. The eight LSBs of the output buffer are lost. The filter cell accumulator is selected by the ADR0-2 inputs.

The 18 MSBs of the output buffer actually pass through the zero mux on their way to the output adder input. The zero mux is controlled by the SHADD input signal and selects either the output buffer 18 MSBs or all zeros for the adder input. A low on the SHADD input selects zero. A high on the SHADD input selects the output buffer MSBs, thus activating the shift-and-add operation. The SHADD signal is latched and delayed by one clock internally.

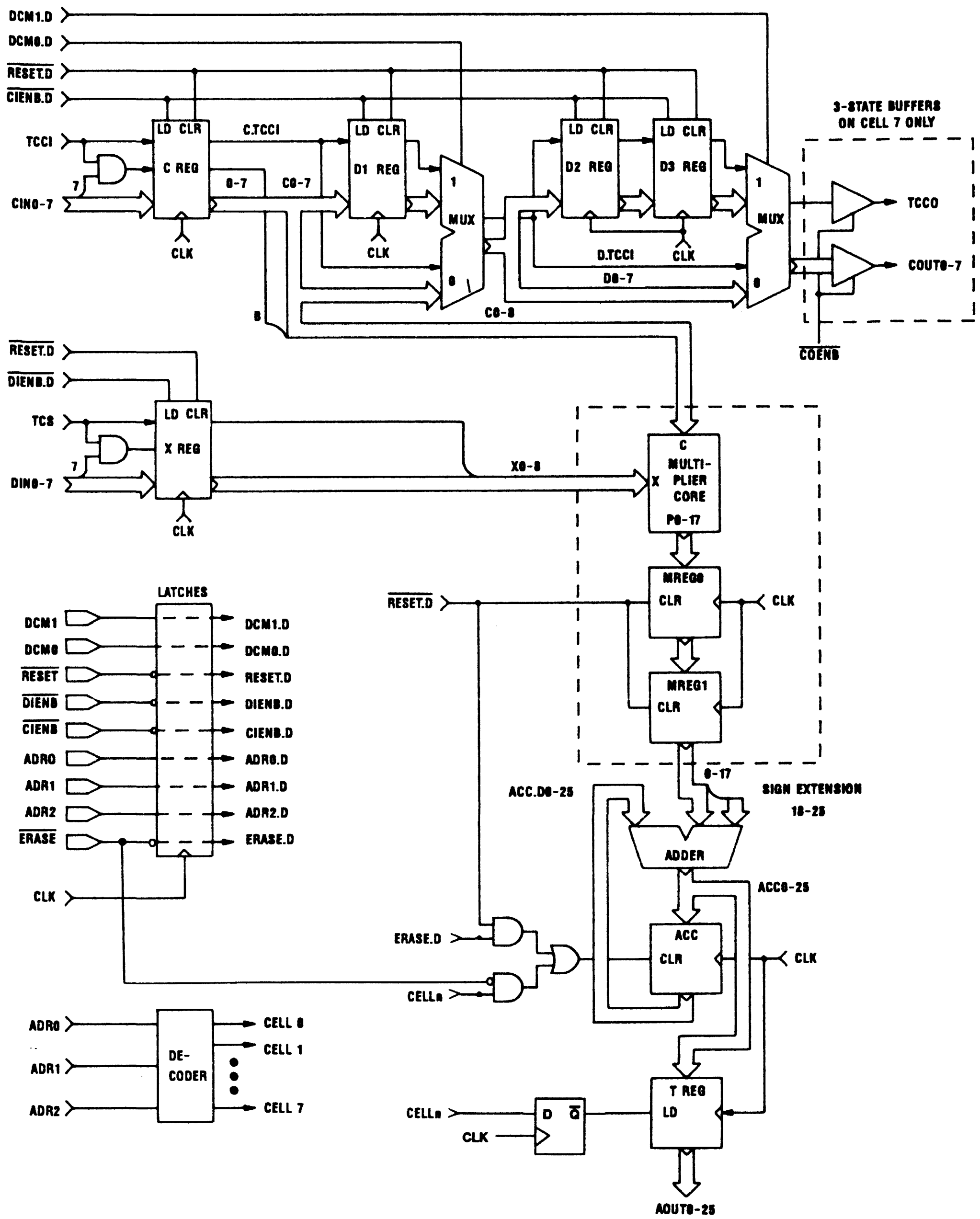


FIGURE 1. HSP43881 FILTER CELL

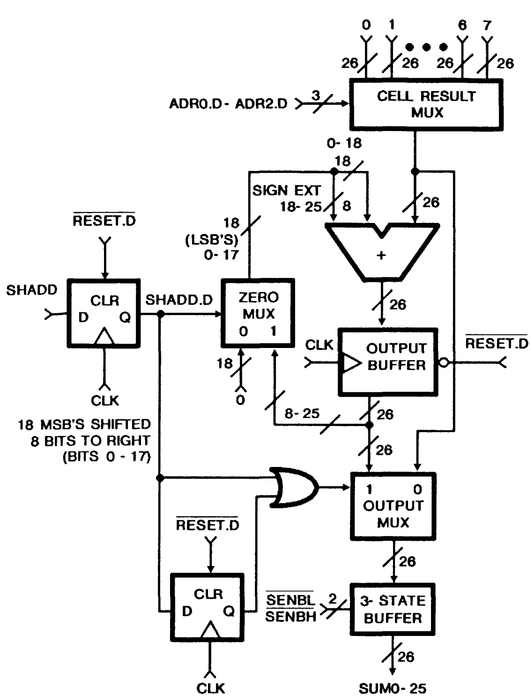


FIGURE 2. HSP43881 DF OUTPUT STAGE

The 26 least significant bits (LSBs) from either a cell accumulator or the output buffer are output on the SUM0-25 bus. The output mux determines whether the cell accumulator selected by ADR0-2 or the output buffer is output to the bus. This mux is controlled by the SHADD input signal. Control is based on the state of the SHADD during two successive clocks; in other words, the output mux selection contains memory. If SHADD is low during a clock cycle and was low during the previous clock, the output mux selects the contents of the filter cell accumulator addressed by ADR0-2. Otherwise the output mux selects the contents of the output buffer.

If the ADR0-2 lines remain at the same address for more than one clock, the output at SUM0-25 will not change to reflect any subsequent accumulator updates in the addressed cell. Only the result available during the first clock when ADR0-2 selects the cell will be output. This does not hinder normal FIR operation since the ADR0-2 lines are changed sequentially. This feature facilitates the interface with slow memories where the output is required to be fixed for more than one clock.

The SUM0-25 output bus is controlled by the SENBH and SENBL signals. A low on SENBL enables bits SUM0-15. A low on SENBH enables bits SUM16-25. Thus all 26 bits can be output simultaneously if the external system has a 26-bit or larger bus. If the external system bus is only 16 bits, the bits can be enabled in two groups of 16 and 10 bits (sign extended).

DF Arithmetic

Both data samples and coefficients can be represented as either unsigned or two's complement numbers. The TCS and TCCI inputs determine the type of arithmetic representation. Internally all values are represented by a 9-bit two's complement number. The value of the additional ninth bit depends on the arithmetic representation selected. For two's complement arithmetic, the sign is extended into the ninth bit. For unsigned arithmetic, bit 9 is 0.

The multiplier output is 18 bits and the accumulator is 26 bits. The accumulator width determines the maximum possible number of terms in the sum of products without overflow. The maximum number of terms depends also on the number system and the distribution of the coefficient and data values. Then maximum numbers of terms in the sum products are:

NUMBER SYSTEM	MAX # OF TERMS
Two unsigned vectors	1032
Two two's complement:	
• Two positive vectors	2080
• Negative vectors	2047
• One positive and one negative vector	2064
One unsigned and one two's complement vector:	
• Positive two's complement vector	1036
• Negative two's complement vector	1028

For practical FIR filters, the coefficients are never all near maximum value, so even larger vectors are possible in practice.

Basic FIR Operation

A simple, 30MHz 8-tap filter example serves to illustrate more clearly the operation of the DF. The sequence table (Table 1) shows the results of the multiply accumulate in each cell after each clock. The coefficient sequence, Cn, enters the DF on the left and moves from left to right through the cells. The data sample sequence, Xn, enters the DF from the top, with each cell receiving the same sample simultaneously. Each cell accumulates the sum of products for one output point. Eight sums of products are calculated simultaneously, but staggered in time so that a new output is available every system clock.

TABLE 1. HSP43881 30MHz, 8 TAP FIR FILTER SEQUENCE

$X_{15} \ldots X_9, X_8, X_7 \ldots X_1, X_0$ → HSP43881

$C_0 \ldots C_6, C_7, C_0 \ldots C_6, C_7$ → HSP43881 → $\ldots Y_{15}, Y_{14} \ldots Y_8, Y_7$

CLK	CELL 0	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7	SUM/CLR
0	$C_7 \times X_0$	0	0	0					-
1	$+C_6 \times X_1$	$C_7 \times X_1$	0	0					-
2	$+C_5 \times X_2$	$+C_6 \times X_2$	$C_7 \times X_2$	0					-
3	$+C_4 \times X_3$	$+C_5 \times X_3$	$+C_6 \times X_3$	$C_7 \times X_3$					-
4	$+C_3 \times X_4$	$+C_4 \times X_4$	$+C_5 \times X_4$	$+C_6 \times X_4$	$C_7 \times X_4$				-
5	$+C_2 \times X_5$	$C_3 \times X_5$	$+C_4 \times X_5$	$+C_5 \times X_5$	$+C_6 \times X_5$	$C_7 \times X_5$			-
6	$+C_1 \times X_6$	$+C_2 \times X_6$	$+C_3 \times X_6$	$+C_4 \times X_6$	$+C_5 \times X_6$	$+C_6 \times X_6$	$C_7 \times X_6$		-
7	$+C_0 \times X_7$	$+C_1 \times X_7$	$+C_2 \times X_7$	$+C_3 \times X_7$	$+C_4 \times X_7$	$+C_5 \times X_7$	$+C_6 \times X_7$	$C_7 \times X_7$	Cell 0 (Y7)
8	$C_7 \times X_8$	$+C_0 \times X_8$	$+C_1 \times X_8$	$+C_2 \times X_8$	$+C_3 \times X_8$	$+C_4 \times X_8$	$+C_5 \times X_8$	$+C_6 \times X_8$	Cell 1 (Y8)
9	$+C_6 \times X_9$	$C_7 \times X_9$	$+C_0 \times X_9$	$+C_1 \times X_9$	$+C_2 \times X_9$	$+C_3 \times X_9$	$+C_4 \times X_9$	$+C_5 \times X_9$	Cell 2 (Y9)
10	$+C_5 \times X_{10}$	$+C_6 \times X_{10}$	$C_7 \times X_{10}$	$+C_0 \times X_{10}$	$+C_1 \times X_{10}$	$+C_2 \times X_{10}$	$+C_3 \times X_{10}$	$+C_4 \times X_{10}$	Cell 3 (Y10)
11	$+C_4 \times X_{11}$	$+C_5 \times X_{11}$	$+C_6 \times X_{11}$	$C_7 \times X_{11}$	$+C_0 \times X_{11}$	$+C_1 \times X_{11}$	$+C_2 \times X_{11}$	$+C_3 \times X_{11}$	Cell 4 (Y11)
12	$+C_3 \times X_{12}$	$+C_4 \times X_{12}$	$+C_5 \times X_{12}$	$+C_6 \times X_{12}$	$C_7 \times X_{12}$	$+C_0 \times X_{12}$	$+C_1 \times X_{12}$	$+C_2 \times X_{12}$	Cell 5 (Y12)
13	$+C_2 \times X_{13}$	$+C_3 \times X_{13}$	$+C_4 \times X_{13}$	$+C_5 \times X_{13}$	$+C_6 \times X_{13}$	$C_7 \times X_{13}$	$+C_0 \times X_{13}$	$+C_1 \times X_{13}$	Cell 6 (Y13)
14	$+C_1 \times X_{14}$	$+C_2 \times X_{14}$	$+C_3 \times X_{14}$	$+C_4 \times X_{14}$	$+C_5 \times X_{14}$	$+C_6 \times X_{14}$	$+C_7 \times X_{14}$	$+C_0 \times X_{14}$	Cell 7 (Y14)
15	$+C_0 \times X_{15}$	$+C_1 \times X_{15}$	$+C_2 \times X_{15}$	$+C_3 \times X_{15}$	$+C_4 \times X_{15}$	$+C_5 \times X_{15}$	$+C_6 \times X_{15}$	$C_7 \times X_{15}$	Cell 0 (Y15)

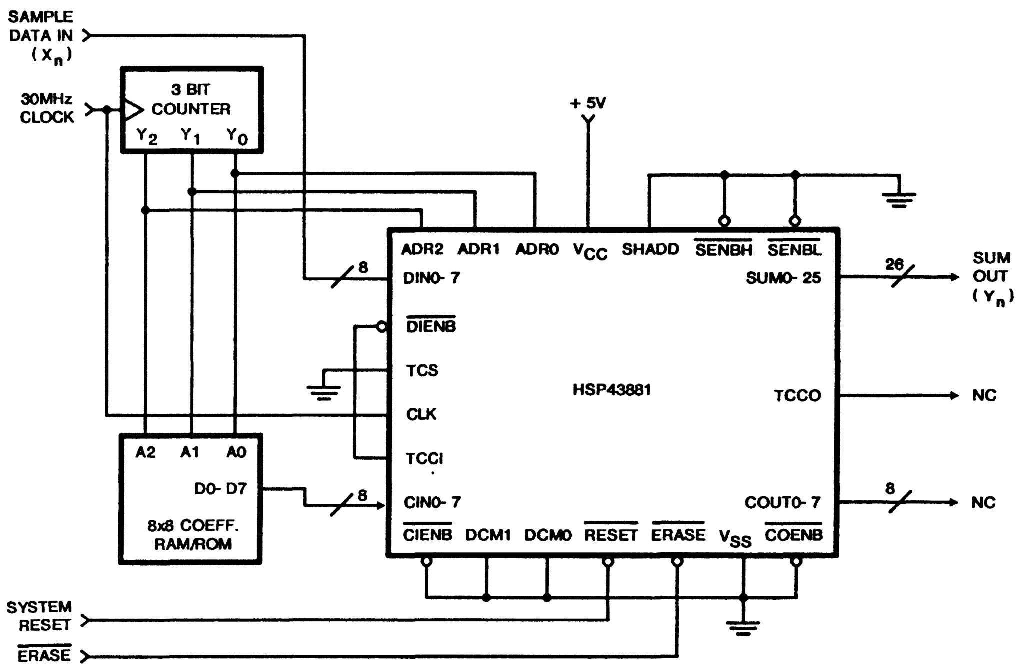


FIGURE 3. HSP43881 30MHz, 8 TAP FIR FILTER APPLICATION SCHEMATIC

Detailed operation of the DF to perform a basic 8-tap, 8-bit coefficient, 8-bit data, 30MHz FIR filter is best understood by observing the schematic (Figure 3) and timing diagram (Figure 4). The internal pipeline length of the DF is four (4) clock cycles, corresponding to the register levels CREG (or XREG), MREG0, MREG1, and TREG (Figures 1 and 2). Therefore the delay from presentation of data and coefficients at the DIN0-7 and CIN0-7 inputs to a sum appearing at the SUM0-25 output is:

k + Td

where

k = filter length

Td = 4, the internal pipeline delay of DF

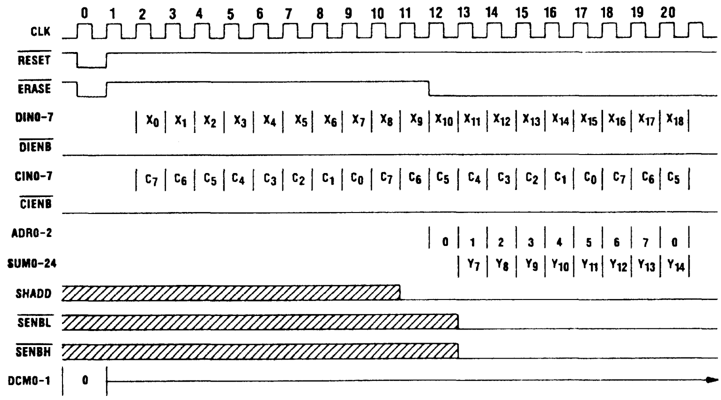
After the pipeline has filled, a new output sample is available every clock. The delay to last sample output from last sample input is Td.

The output sums, Yn, shown in the timing diagram are derived from the sum-of-products equation:

Y(n) = C(0) x X(n) + C(1) x X(n-1) + C(2) x X(n-2) + C(3) x X(n-3) + C(4) x X(n-4) + C(5) x X(n-5) + C(6) x X(n-6) + C(7) x X(n-7)

Extended FIR Filter Length

Filter lengths greater that eight taps can be created by either cascading together multiple DF devices or "reusing" a single device. Using multiple devices, an FIR filter of over 1000 taps can be constructed to operate at a 30MHz sample rate. Using a single device clocked at 30MHz, an FIR filter of over 1000 taps can be constructed to operate at less than a 30MHz sample rate. Combinations of these two techniques are also possible.



$$Y_N = \sum_{K=0}^{7} C_K \times X_{N-K}$$

FIGURE 4. HSP43881 30MHz, 8 TAP FIR FILTER TIMING

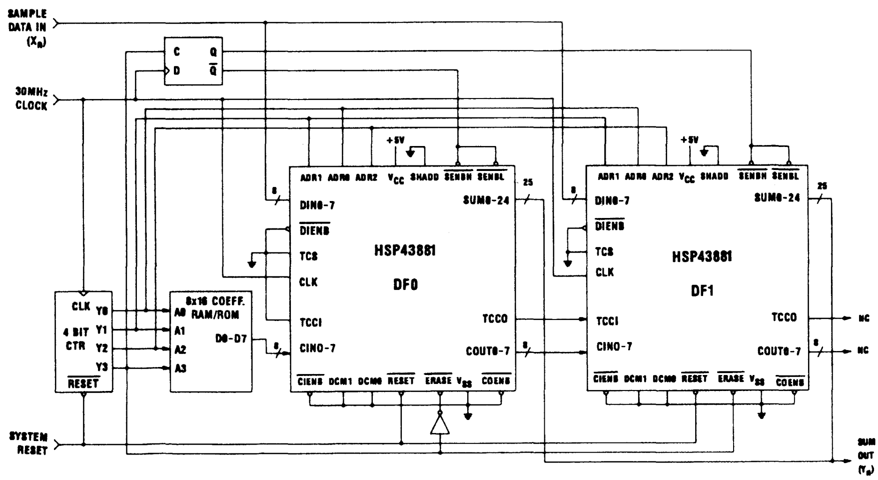


FIGURE 5. HSP43881 30MHz, 16 TAP FIR FILTER CASCADE APPLICATION SCHEMATIC.

Cascade Configuration

To design a filter length L>8, L/8 DFs are cascaded by connecting the COUT0-7 outputs of the (i)th DF to the CIN0-7 inputs of the (i+1)th DF. The DIN0-7 inputs and SUM0-25 outputs of all the DFs are also tied together. A specific example of two cascaded DFs illustrates the technique (Figure 5). Timing (Figure 6) is similar to the simple 8-tap FIR, except the $\overline{\text{ERASE}}$ and $\overline{\text{SENBL}}/\overline{\text{SENBH}}$ signals must be enabled independently for the two DFs in order to clear the correct accumulators and enable the SUM0-25 output signals at the proper times.

Single DF Configuration

Using a single DF, a filter of length L>8 can be constructed by processing in L/8 passes as illustrated in the following table (Table 2) for a 16-tap FIR. Each pass is composed of

TABLE 2. HSP43881 16-TAP FIR FILTER SEQUENCE USING A SINGLE DF

Data Sequence Input: $X_{30} \ldots X_9, X_8, X_{22} \ldots X_1, X_0$

Coefficient Sequence Input: $C_0 \ldots C_{14}, C_{15}, 0 \ldots 0, C_0 \ldots C_{14}, C_{15}$ → HSP43881 → $\ldots 0, Y_{30} \ldots Y_{23}, 0 \ldots 0, Y_{22} \ldots Y_{15}, 0 \ldots 0$

CLK	CELL 0	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7	SUM/CLR
6	$C_{15} \times X_0$	0	0	0					-
7	$+C_{14} \times X_1$	$C_{15} \times X_1$	0	0					-
8	$+C_{13} \times X_2$		$C_{15} \times X_2$	0					-
9	$+C_{12} \times X_3$			$C_{15} \times X_3$					-
10	$+C_{11} \times X_4$			$+C_{14} \times X_4$	$C_{15} \times X_4$				-
11	$+C_{10} \times X_5$			$+C_{13} \times X_5$		$C_{15} \times X_5$			-
12	$+C_9 \times X_6$			$+C_{12} \times X_6$			$C_{15} \times X_6$		-
13	$+C_8 \times X_7$			$+C_{11} \times X_7$				$C_{15} \times X_7$	-
14	$+C_7 \times X_8$			$+C_{10} \times X_8$				$+C_{14} \times X_8$	-
15	$+C_6 \times X_9$			$+C_9 \times X_9$				$+C_{13} \times X_9$	-
16	$+C_5 \times X_{10}$			$+C_8 \times X_{10}$				$+C_{12} \times X_{10}$	-
17	$+C_4 \times X_{11}$			$+C_7 \times X_{11}$				$+C_{11} \times X_{11}$	-
18	$+C_3 \times X_{12}$			$+C_6 \times X_{12}$				$+C_{10} \times X_{12}$	-
19	$+C_2 \times X_{13}$			$+C_5 \times X_{13}$				$+C_9 \times X_{13}$	-
20	$+C_1 \times X_{14}$			$+C_4 \times X_{14}$				$+C_8 \times X_{14}$	-
21	$+C_0 \times X_{15}$			$+C_3 \times X_{15}$				$+C_7 \times X_{15}$	CELL 0 (Y15)
22	0	$C_0 \times X_{16}$		$+C_2 \times X_{16}$				$+C_6 \times X_{16}$	CELL 1 (Y16)
23	0	0	$C_0 \times X_{17}$	$+C_1 \times X_{17}$				$+C_5 \times X_{17}$	CELL 2 (Y17)
24	0	0	0	$+C_0 \times X_{18}$				$+C_4 \times X_{18}$	CELL 3 (Y18)
25	0	0	0	0	$C_0 \times X_{19}$			$+C_3 \times X_{19}$	CELL 4 (Y19)
26	0	0	0	0	0	$C_0 \times X_{20}$		$+C_2 \times X_{20}$	CELL 5 (Y20)
27	0	0	0	0	0	0	$C_0 \times X_{21}$	$+C_1 \times X_{21}$	CELL 6 (Y21)
28	0	0	0	0	0	0	0	$+C_0 \times X_{22}$	CELL 7 (Y22)
29	$C_{15} \times X_8$	0	0	0	0	0	0	0	-
30	$+C_{14} \times X_9$	$C_{15} \times X_9$	0	0	0	0	0	0	-
31	$+C_{13} \times X_{10}$		$C_{15} \times X_{10}$	0	0	0	0	0	-
32	$+C_{12} \times X_{11}$			$C_{15} \times X_{11}$	0	0	0	0	-
33	$+C_{11} \times X_{12}$				$C_{15} \times X_{12}$	0	0	0	-
34	$+C_{10} \times X_{13}$					$C_{15} \times X_{13}$	0	0	-
35	$+C_9 \times X_{14}$						$C_{15} \times X_{14}$	0	-
36	$+C_8 \times X_{15}$							$C_{15} \times X_{15}$	-
37	$+C_7 \times X_{16}$							$+C_{14} \times X_{16}$	-
38	$+C_6 \times X_{17}$							$+C_{13} \times X_{17}$	-
39	$+C_5 \times X_{18}$							$+C_{12} \times X_{18}$	-
40	$+C_4 \times X_{19}$							$+C_{11} \times X_{19}$	-
41	$+C_3 \times X_{20}$							$+C_{10} \times X_{20}$	-
42	$+C_2 \times X_{21}$							$+C_9 \times X_{21}$	-
43	$+C_1 \times X_{22}$							$+C_8 \times X_{22}$	-
44	$+C_0 \times X_{23}$							$+C_7 \times X_{23}$	CELL 0 (Y23)
45	0	$C_0 \times X_{24}$						$+C_6 \times X_{24}$	CELL 1 (Y24)
46	0	0	$C_0 \times X_{25}$					$+C_5 \times X_{25}$	CELL 2 (Y25)
47	0	0	0	$C_0 \times X_{26}$				$+C_4 \times X_{26}$	CELL 3 (Y26)
48	0	0	0	0	$C_0 \times X_{27}$			$+C_3 \times X_{27}$	CELL 4 (Y27)

3

1D FILTERS

Tp = 7 + L cycles and computes eight output samples. In pass i, the sample with indices i*8 to i*8 +(L-1) enter the DIN0-7 inputs. The coefficients C_0 - C_{L-1} enter the CIN0-7 inputs, followed by seven zeros. As these zeros are entered, the result samples are output and the accumulators reset. Initial filing of the pipeline is not shown in this sequence table. Filter outputs can be put through a FIFO to even out the sample rate.

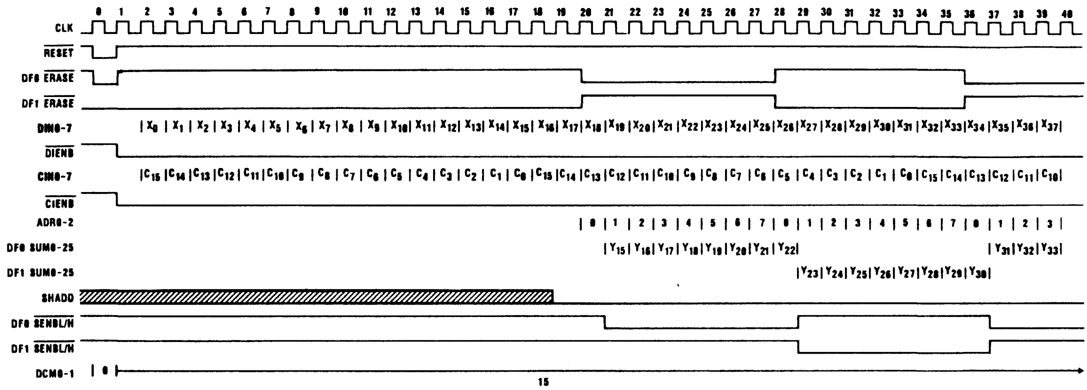
Extended Coefficient and Data Sample Word Size

The sample and coefficient word size can be extended by utilizing several DFs in parallel to get the maximum sample rate or a single DF with resulting lower sample rates. The technique is to compute partial products of 8x8 and combine these partial products by shifting and adding to obtain the final result. The shifting and adding can be accomplished with external adders (at full speed) or with the DF's shift-and-add mechanism contained in its output stage (at reduced speed).

Decimation/Resampling

The HSP43881 DF provides a mechanism for decimating by factors of 2, 3, or 4. From the DF filter cell block diagram (Figure 1), note the three D registers and two multiplexers in the coefficient path through the cell. These allow the coefficients to be delayed by 1, 2, or 3 clocks through the cell. The sequence table (Table 3) for a decimate-by-two- filter illustrates the technique (internal cell pipelining ignored for simplicity).

Detailed timing for a 30MHz input sample rate, 15MHz output sample rate (i.e., decimate-by-two), 16-tap FIR filter, including pipelining, is shown in Figure 7. This filter requires only a single HSP43881 DF.



$$Y_N = \sum_{K=0}^{15} C_K \times X_{N-K}$$

FIGURE 6. HSP43881 16-TAP 30MHz FIR FILTER TIMING USING TWO CASCADED HSP43881s

TABLE 3. HSP43881 16-TAP DECIMATE-BY-TWO FIR FILTER SEQUENCE; 30MHz IN, 15MHz OUT

Data Sequence Input . . . X_2, X_1, X_0 → HSP43881

Coefficient Sequence Input . . . $C_{15}, C_0 \ldots C_{13}, C_{14}, C_{15}$ → HSP43881 → . . . $Y_{19}, -, Y_{17}, -, Y_{15}$

CLK	CELL 0	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7	SUM/CLR
6	$C_{15} \times X_0$	0	0	0	0	0	0	0	-
7	$+C_{14} \times X_1$	0	0	0	0	0	0	0	-
8	$+C_{13} \times X_2$	$C_{15} \times X_2$	0	0	0	0	0	0	-
9	$+C_{12} \times X_3$		0	0	0	0	0	0	-
10	$+C_{11} \times X_4$		$C_{15} \times X_4$	0	0	0	0	0	-
11	$+C_{10} \times X_5$			0	0	0	0	0	-
12	$+C_9 \times X_6$			$C_{15} \times X_6$	0	0	0	0	-
13	$+C_8 \times X_7$				0	0	0	0	-
14	$+C_7 \times X_8$				$C_{15} \times X_8$	0	0	0	-
15	$+C_6 \times X_9$					0	0	0	-
16	$+C_5 \times X_{10}$					$C_{15} \times X_{10}$	0	0	-
17	$+C_4 \times X_{11}$						0	0	-
18	$+C_3 \times X_{12}$						$C_{15} \times X_{12}$	0	-
19	$+C_2 \times X_{13}$							0	-
20	$+C_1 \times X_{14}$							$C_{15} \times X_{14}$	-
21	$+C_0 \times X_{15}$							$+C_{14} \times X_{15}$	CELL 0 (Y15)
22	$C_{15} \times X_{16}$							$+C_{13} \times X_{16}$	-
23	$+C_{14} \times X_{17}$							$+C_{12} \times X_{17}$	CELL 1 (Y17)
24	$+C_{13} \times X_{18}$							$+C_{11} \times X_{18}$	-
25	$+C_{12} \times X_{19}$							$+C_{10} \times X_{19}$	CELL 2 (Y19)
26	$+C_{11} \times X_{20}$							$+C_9 \times X_{20}$	-
27	$+C_{10} \times X_{21}$							$+C_8 \times X_{21}$	CELL 3 (Y21)
28	$+C_9 \times X_{22}$							$+C_7 \times X_{22}$	-
29	$+C_8 \times X_{23}$							$+C_6 \times X_{23}$	CELL 4 (Y23)
30	$+C_7 \times X_{24}$							$+C_5 \times X_{24}$	-
31	$+C_6 \times X_{25}$							$+C_4 \times X_{25}$	CELL 5 (Y25)
32	$+C_5 \times X_{26}$							$+C_3 \times X_{26}$	-
33	$+C_4 \times X_{27}$							$+C_2 \times X_{27}$	CELL 6 (Y27)
34	$+C_3 \times X_{28}$							$+C_1 \times X_{28}$	-
35	$+C_2 \times X_{29}$							$+C_0 \times X_{29}$	CELL 7 (Y29)
36	$+C_1 \times X_{30}$							$C_{15} \times X_{30}$	-
37	$+C_0 \times X_{31}$	$+C_{14} \times X_{31}$	$+C_{14} \times X_{31}$	$+C_{14} \times X_{31}$	$+C_{14} \times X_{31}$	$+C_{14} \times X_{31}$	$+C_{14} \times X_{31}$	$+C_{14} \times X_{31}$	CELL 8 (Y31)
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓

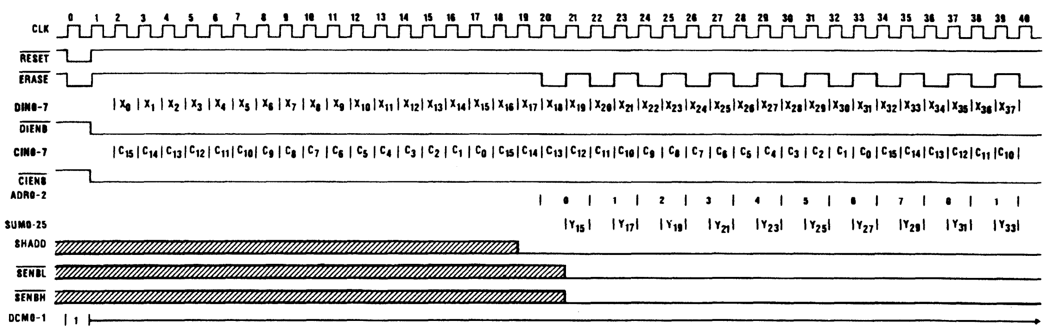


FIGURE 7. HSP43881 16-TAP DECIMATE-BY-TWO FIR FILTER TIMING; 30MHz IN, 15MHz OUT

3

1D FILTERS

Absolute Maximum Ratings

Supply Voltage	+8.0V
Input, Output Voltage	GND -0.5V to V_{CC} +0.5V
Storage Temperature	-65°C to +150°C
ESD	Class 1
Maximum Package Power Dissipation at 70°C	2.4W (PLCC), 2.88W (PGA)
θ_{jc}	11.1°C/W (PLCC), 7.78°C/W (PGA)
θ_{ja}	33.7°C/W (PLCC), 34.66°C/W (PGA)
Gate Count	17763
Junction Temperature	150°C (PLCC), 175°C (PGA)
Lead Temperature (Soldering 10s)	300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range	5V ±5%
Operating Temperature Range	0°C to +70°C

D.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
I_{CCOP}	Power Supply Current	-	140	mA	V_{CC} = Max CLK Frequency 20MHz Note 1, Note 3
I_{CCSB}	Standby Power Supply Current	-	500	μA	V_{CC} = Max, Note 3
I_I	Input Leakage Current	-10	10	μA	V_{CC} = Max, Input = 0V or V_{CC}
I_O	Output Leakage Current	-10	10	μA	V_{CC} = Max, Input = 0V or V_{CC}
V_{IH}	Logical One Input Voltage	2.0	-	V	V_{CC} = Max
V_{IL}	Logical Zero Input Voltage		0.8	V	V_{CC} = Min
V_{OH}	Logical One Output Voltage	2.6	-	V	I_{OH} = -400μA, V_{CC} = Min
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} = 2mA, V_{CC} = Min
V_{IHC}	Clock Input High	3.0	-	V	V_{CC} = Max
V_{ILC}	Clock Input Low	-	0.8	V	V_{CC} = Min
C_{IN}	Input Capacitance PLCC PGA	- -	10 15	pF pF	CLK Frequency 1MHz All measurements referenced to GND T_A = +25°C, Note 2
C_{OUT}	Output Capacitance PLCC PGA	- -	10 15	pF pF	

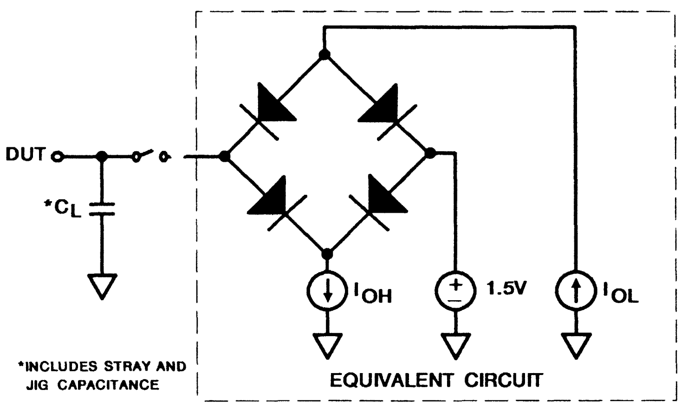
NOTES:
1. Operating supply current is proportional to frequency. Typical rating is 7mA/MHz.
2. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
3. Output load per test load circuit and C_L = 40pF.

A.C. Electrical Specifications V_{CC} = 5V ±5%, T_A = 0°C to +70°C

SYMBOL	PARAMETER	-20 (20MHz)		-25 (25.6MHz)		-30 (30MHz)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
T_{CP}	Clock Period	50	-	39	-	33	-	ns	
T_{CL}	Clock Low	20	-	16	-	13	-	ns	
T_{CH}	Clock High	20	-	16	-	13	-	ns	
T_{IS}	Input Setup	16	-	14	-	13	-	ns	
T_{IH}	Input Hold	0	-	0	-	0	-	ns	
T_{ODC}	CLK to Coefficient Output Delay	-	24	-	20	-	18	ns	
T_{OED}	Output Enable Delay	-	20	-	15	-	15	ns	
T_{ODD}	Output Disable Delay	-	20	-	15	-	15	ns	Note 1
T_{ODS}	CLK to SUM Output Delay	-	27	-	25	-	21	ns	
T_{OR}	Output Rise	-	6	-	6	-	6	ns	Note 1
T_{OF}	Output Fall	-	6	-	6	-	6	ns	Note 1

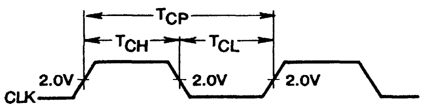
NOTE:
1. Controlled by design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

Test Load Circuit

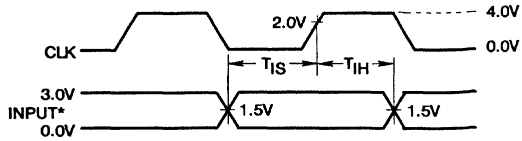


Switch S1 Open for I_{CCSB} and I_{CCOP} Tests

Waveforms

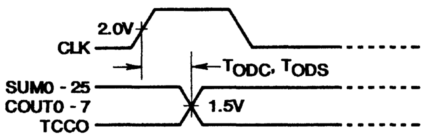


CLOCK AC PARAMETERS



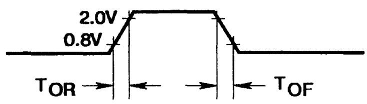
* Input includes: DIN0-7, CIN0-7, DIENB, CIENB, ERASE, RESET, DCM0-1, ADR0-2, TCS, TCCI, SHADD

INPUT SETUP AND HOLD

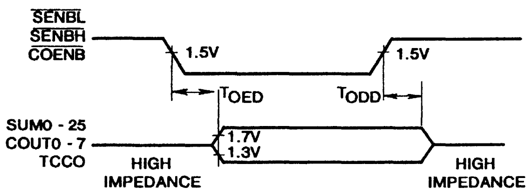


* SUM0-25, COUT0-7, TCCO are assumed not to be in high-impedance state

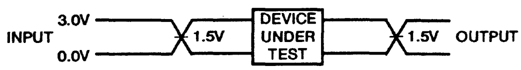
SUM0-25, COUT0-7, TCCO OUTPUT DELAYS



OUTPUT RISE AND FALL TIMES



OUTPUT ENABLE, DISABLE TIMING



A.C. Testing: Inputs are driven at 3.0V for Logic "1" and 0.0V for Logic "0". Input and output timing measurements are made at 1.5V for both a Logic "1" and "0". CLK is driven at 4.0V and 0V and measured at 2.0V.

A.C. TESTING INPUT, OUTPUT WAVEFORM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **0MHz to 25.6MHz Sample Rate**
- **Eight Filter Cells**
- **8-Bit Coefficients and Signal Data**
- **Low Power CMOS Operation**
  - **I_{CCSB} 500μA Maximum**
  - **I_{CCOP} 160mA Maximum at 20MHz**
- **26-Bit Accumulator Per Stage**
- **Filter Lengths Up to 1032 Taps**
- **Expandable Coefficient Size, Data Size and Filter Length**
- **Decimation by 2, 3 or 4**

Applications

- **1-D and 2-D FIR Filters**
- **Radar/Sonar**
- **Adaptive Filters**
- **Echo Cancellation**
- **Complex Multiply-Add**
- **Sample Rate Converters**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43881GM-20/883	-55°C to +125°C	85 Lead PGA
HSP43881GM-25/883	-55°C to +125°C	85 Lead PGA

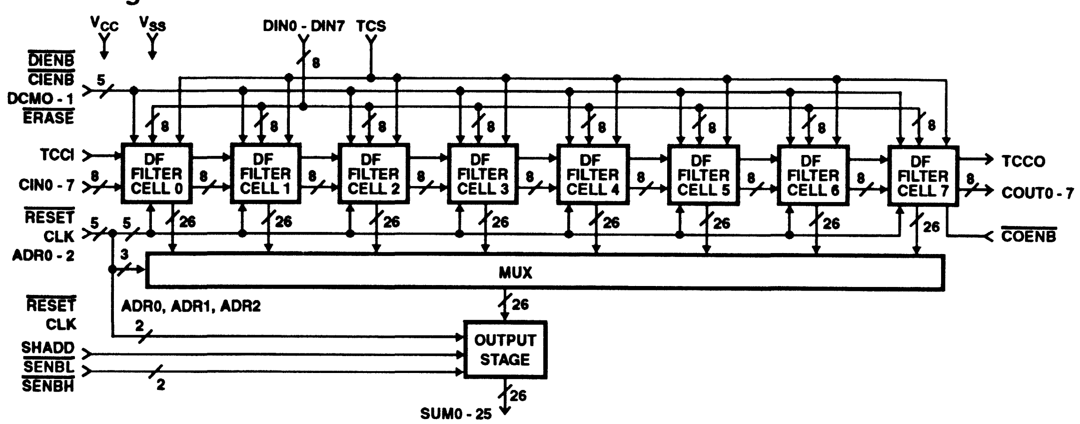
Description

The HSP43881/883 is a video speed Digital Filter (DF) designed to efficiently implement vector operations such as FIR digital filters. It is comprised of eight filter cells cascaded internally and a shift and add output stage, all in a single integrated circuit. Each filter cell contains a 8 x 8-bit multiplier, three decimation registers and a 26-bit accumulator. The output stage contains an additional 26-bit accumulator which can add the contents of any filter cell accumulator to the output stage accumulator shifted right by 8-bits. The HSP43881/883 has a maximum sample rate of 25.6MHz. The effective multiply accumulate (mac) rate is 204MHz.

The HSP43881/883 DF can be configured to process expanded coefficient and word sizes. Multiple DFs can be cascaded for larger filter lengths without degrading the sample rate or a single DF can process larger filter lengths at less than 25.6MHz with multiple passes. The architecture permits processing filter lengths of over 1000 taps with the guarantee of no overflows. In practice, most filter coefficients are less than 1.0, making even larger filter lengths possible. The DF provides for 8-bit unsigned or two's complement arithmetic, independently selectable for coefficients and signal data.

Each DF filter cell contains three resampling or decimation registers which permit output sample rate reduction at rates of $^1/_2$, $^1/_3$ or $^1/_4$ the input sample rate. These registers also provide the capability to perform 2-D operations such as matrix multiplication and N x N spatial correlations/convolutions for image processing applications.

Block Diagram



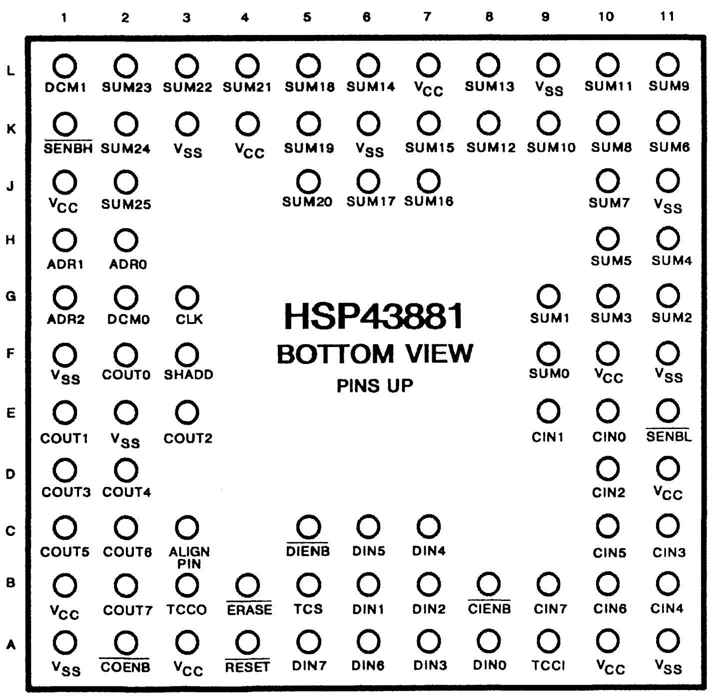
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

Pinouts

85 PIN GRID ARRAY (PGA)

	1	2	3	4	5	6	7	8	9	10	11
A	V_{SS}	$\overline{\text{COENB}}$	V_{CC}	$\overline{\text{RESET}}$	DIN7	DIN6	DIN3	DIN0	TCCI	V_{CC}	V_{SS}
B	V_{CC}	COUT7	TCCO	$\overline{\text{ERASE}}$	TCS	DIN1	DIN2	$\overline{\text{CIENB}}$	CIN7	CIN6	CIN4
C	COUT5	COUT6	ALIGN PIN		$\overline{\text{DIENB}}$	DIN5	DIN4			CIN5	CIN3
D	COUT3	COUT4								CIN2	V_{CC}
E	COUT1	V_{SS}	COUT2						CIN1	CIN0	$\overline{\text{SENBL}}$
F	V_{SS}	COUT0	SHADD						SUM0	V_{CC}	V_{SS}
G	ADR2	DCM0	CLK						SUM1	SUM3	SUM2
H	ADR1	ADR0								SUM5	SUM4
J	V_{CC}	SUM25			SUM20	SUM17	SUM16			SUM7	V_{SS}
K	$\overline{\text{SENBH}}$	SUM24	V_{SS}	V_{CC}	SUM19	V_{SS}	SUM15	SUM12	SUM10	SUM8	SUM6
L	DCM1	SUM23	SUM22	SUM21	SUM18	SUM14	V_{CC}	SUM13	V_{SS}	SUM11	SUM9

HSP43881/883
TOP VIEW
PINS DOWN



Note: An overbar on a signal name represents an active LOW signal.

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output Voltage Applied .... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering, Ten Seconds) .... +300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
Ceramic PGA Package .... 34.66°C/W 7.78°C/W
Maximum Package Power Dissipation at +125°C
Ceramic PGA Package .... 1.44 Watt
Gate Count .... 17762 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range .... -55°C to +125°C

TABLE 1. HSP43881/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	+10	µA
Output Leakage Current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	+10	µA
Clock Input High	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V, Outputs Open	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 20.0MHz V_{CC} = 5.5V (Note 2)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	160.0	mA
Functional Test	FT	(Note 3)	7, 8	-55°C ≤ T_A ≤ +125°C	-	-	

NOTES:
1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 8.0mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, VOH ≥ 1.5V, V_{OL} ≤ 1.5V, V_{IHC} = 3.4V, and V_{ILC} = 0.4V.

3

1D FILTERS

TABLE 2. HSP43881/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	-20 (20MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
Clock Period	T_{CP}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	39	-	ns
Clock Low	T_{CL}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	16	-	ns
Clock High	T_{CH}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	16	-	ns
Input Setup	T_{IS}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	17	-	ns
Input Hold	T_{IH}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
CLK to Coefficient Output Delay	T_{ODC}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	24	-	20	ns
Output Enable Delay	T_{OED}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	20	-	15	ns
CLK to SUM Output Delay	T_{ODS}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	31	-	25	ns

NOTE: 1. A.C. Testing: V_{CC} = 4.5V and 5.5V. Inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a Logic "1" and "0". CLK is driven at 4.0V and 0V and measured at 2.0V.

TABLE 3. HSP43881/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	-20		-25		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	V_{CC}=Open, f=1MHz All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	15	-	15	pF
Output Capacitance	C_{OUT}		1	$T_A = +25^oC$	-	15	-	15	pF
Output Disable Delay	T_{ODD}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	20	-	15	ns
Output Rise Time	T_{OR}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	7	-	6	ns
Output Fall Time	T_{OF}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	7	-	6	ns

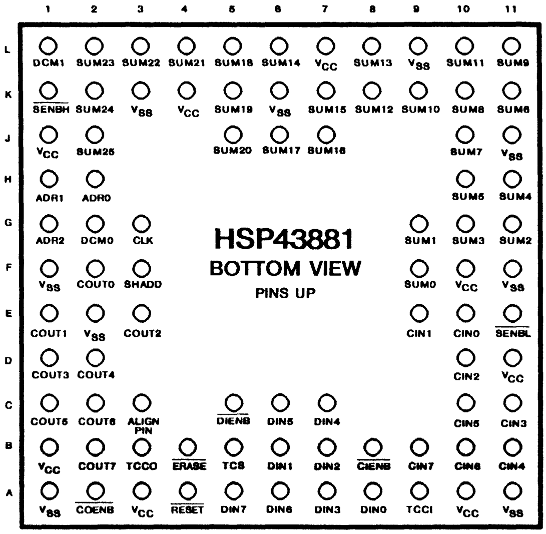
NOTES:
1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Loading is as specified in the test load circuit, C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Burn-In Circuit

HSP43881/883 PIN GRID ARRAY (PGA)



PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	V_{SS}	GND	C1	COUT5	$V_{CC}/2$	F10	V_{CC}	V_{CC}	K4	V_{CC}	V_{CC}
A2	$\overline{\text{COENB}}$	F10	C2	COUT6	$V_{CC}/2$	F11	V_{SS}	GND	K5	SUM19	$V_{CC}/2$
A3	V_{CC}	V_{CC}	C3	ALIGN	NC	G1	ADR2	F2	K6	V_{SS}	GND
A4	$\overline{\text{RESET}}$	F11	C5	$\overline{\text{DIENB}}$	F10	G2	DCM0	F5	K7	SUM15	$V_{CC}/2$
A5	DIN7	F8	C6	DIN5	F5	G3	CLK	F0	K8	SUM12	$V_{CC}/2$
A6	DIN6	F6	C7	DIN4	F4	G9	SUM1	$V_{CC}/2$	K9	SUM10	$V_{CC}/2$
A7	DIN3	F3	C10	CIN5	F5	G10	SUM3	$V_{CC}/2$	K10	SUM8	$V_{CC}/2$
A8	DIN0	F0	C11	CIN3	F3	G11	SUM2	$V_{CC}/2$	K11	SUM6	$V_{CC}/2$
A9	CIN8/TCCI	F8	D1	COUT3	$V_{CC}/2$	H1	ADR1	F1	L1	DCM1	F6
A10	V_{CC}	V_{CC}	D2	COUT4	$V_{CC}/2$	H2	ADR0	F0	L2	SUM23	$V_{CC}/2$
A11	V_{SS}	GND	D10	CIN2	F2	H10	SUM5	$V_{CC}/2$	L3	SUM22	$V_{CC}/2$
B1	V_{CC}	V_{CC}	D11	V_{CC}	V_{CC}	H11	SUM4	$V_{CC}/2$	L4	SUM21	$V_{CC}/2$
B2	COUT7	$V_{CC}/2$	E1	COUT1	$V_{CC}/2$	J1	V_{CC}	V_{CC}	L5	SUM18	$V_{CC}/2$
B3	COUT8/TCCO	$V_{CC}/2$	E2	V_{SS}	GND	J2	SUM25	$V_{CC}/2$	L6	SUM14	$V_{CC}/2$
B4	$\overline{\text{ERASE}}$	F10	E3	COUT2	$V_{CC}/2$	J5	SUM20	$V_{CC}/2$	L7	V_{CC}	V_{CC}
B5	DIN8/TCS	F7	E9	CIN1	F1	J6	SUM17	$V_{CC}/2$	L8	SUM13	$V_{CC}/2$
B6	DIN1	F1	E10	CIN0	F0	J7	SUM16	$V_{CC}/2$	L9	V_{SS}	GND
B7	DIN2	F2	E11	$\overline{\text{SENBL}}$	F10	J10	SUM7	$V_{CC}/2$	L10	SUM11	$V_{CC}/2$
B8	$\overline{\text{CIENB}}$	F10	F1	V_{SS}	GND	J11	V_{SS}	GND	L11	SUM9	$V_{CC}/2$
B9	CIN7	F7	F2	COUT0	$V_{CC}/2$	K1	$\overline{\text{SENBH}}$	F10			
B10	CIN6	F6	F3	SHADD	F9	K2	SUM24	$V_{CC}/2$			
B11	CIN4	F4	F9	SUM0	VCC/2	K3	V_{SS}	GND			

NOTES:

1. $V_{CC}/2$ (2.7V ± 10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5V ± 0.5V.
4. 0.1μF (min) capacitor between V_{CC} and GND per device.
5. F0 = 100kHz ± 10%, F1 = F0/2, F2 = F1/2 . . . , F11 = F10/2, 40% - 60% Duty Cycle.
6. Input voltage Limits: V_{IL} = 0.8V Max, V_{IH} = 4.5V ±10%

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1D FILTERS

Die Characteristics

DIE DIMENSIONS:
328 x 283 x 19 ±1 mils

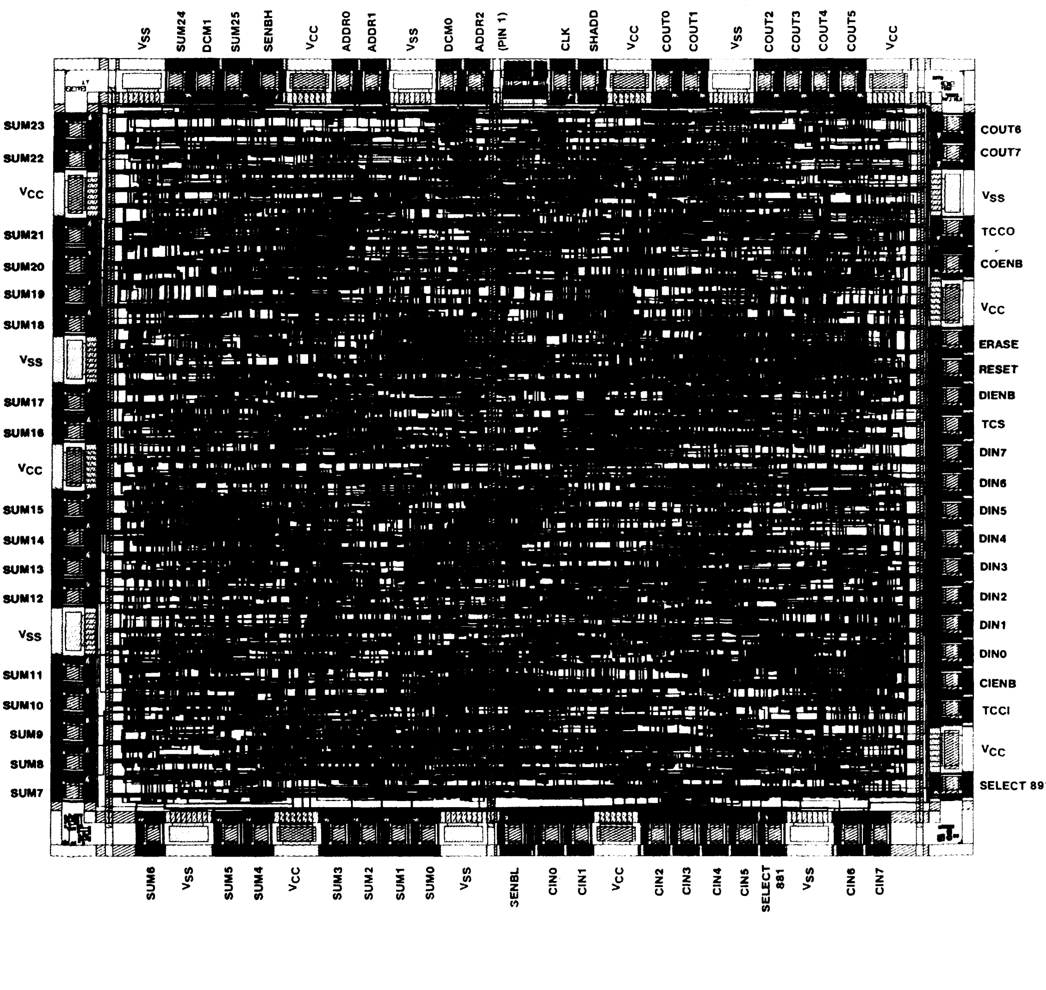
METALLIZATION:
Type: Si-Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY: 1.2 x 10^5A/cm^2

Metallization Mask Layout

HSP43881/883



HSP43891

January 1994

Digital Filter

Features

- Eight Filter Cells
- 0MHz to 30MHz Sample Rate
- 9-Bit Coefficients and Signal Data
- 26-Bit Accumulator per Stage
- Filter Lengths Over 1000 Taps
- Expandable Coefficient Size, Data Size and Filter Length
- Decimation by 2, 3 or 4

Applications

- 1-D and 2-D FIR Filters
- Radar/Sonar
- Digital Video
- Adaptive Filters
- Echo Cancellation
- Complex Multiply-Add
- Sample Rate Converters

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43891VC-20	0°C to +70°C	100 Lead MQFP
HSP43891VC-25	0°C to +70°C	100 Lead MQFP
HSP43891VC-30	0°C to +70°C	100 Lead MQFP
HSP43891JC-20	0°C to +70°C	84 Lead PLCC
HSP43891JC-25	0°C to +70°C	84 Lead PLCC
HSP43891JC-30	0°C to +70°C	84 Lead PLCC
HSP43891GC-20	0°C to +70°C	85 Lead PGA
HSP43891GC-25	0°C to +70°C	85 Lead PGA
HSP43891GC-30	0°C to +70°C	85 Lead PGA

Description

The HSP43891 is a video-speed Digital Filter (DF) designed to efficiently implement vector operations such as FIR digital filters. It is comprised of eight filter cells cascaded internally and a shift and add output stage, all in a single integrated circuit. Each filter cell contains a 9 x 9 two's complement multiplier, three decimation registers and a 26-bit accumulator. The output stage contains an additional 26-bit accumulator which can add the contents of any filter cell accumulator to the output stage accumulator shifted right by 8-bits. The HSP43891 has a maximum sample rate of 30MHz. The effective multiply-accumulate (mac) rate is 240MHz.

The HSP43891 DF can be configured to process expanded coefficient and word sizes. Multiple DFs can be cascaded for larger filter lengths without degrading the sample rate or a single DF can process larger filter lengths at less than 30MHz with multiple passes. The architecture permits processing filter lengths of over 1000 taps with the guarantee of no overflows. In practice, most filter coefficients are less than 1.0, making even larger filter lengths possible. The DF provides for 8-bit unsigned or 9-bit two's complement arithmetic, independently selectable for coefficients and signal data.

Each DF filter cell contains three re-sampling or decimation registers which permit output sample rate reduction at rates of 1/2, 1/3 or 1/4 the input sample rate. These registers also provide the capability to perform 2-D operations such as matrix multiplication and N x N spatial correlations/ convolutions for image processing applications.

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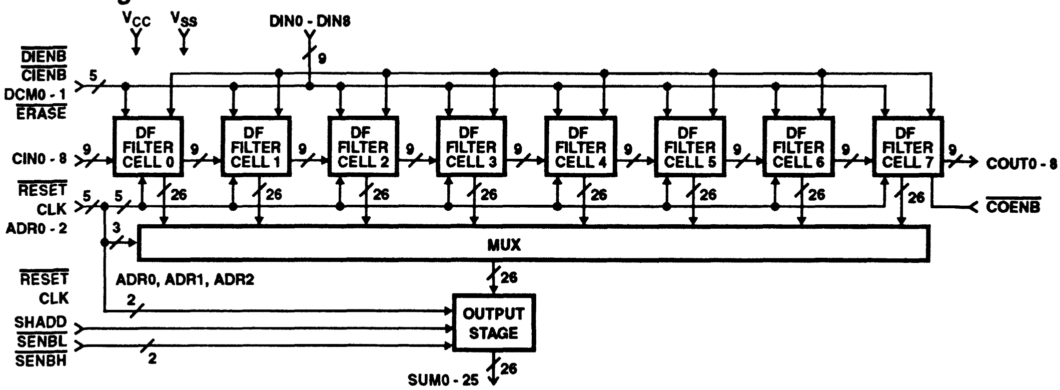
1D FILTERS

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

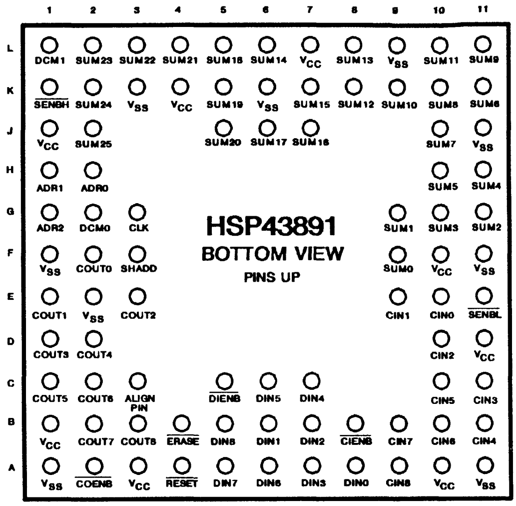
File Number 2785.3

Pinouts

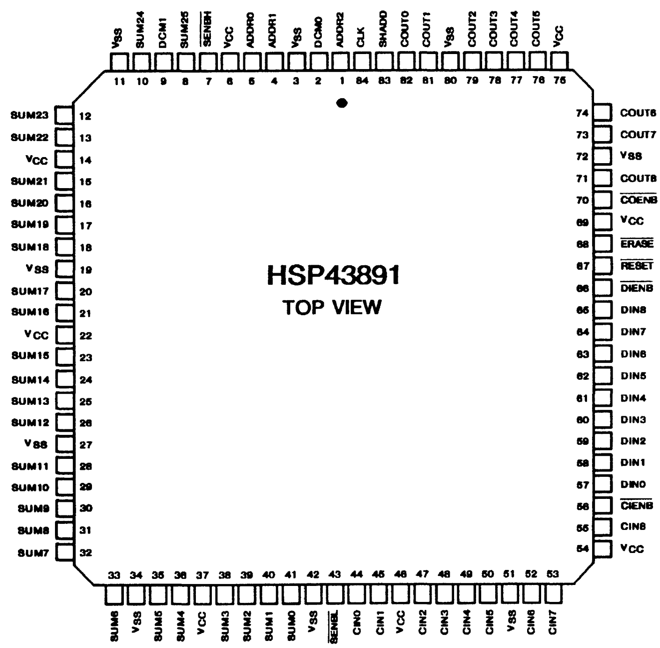
85 PIN GRID ARRAY (PGA)

	1	2	3	4	5	6	7	8	9	10	11
A	V_{SS}	$\overline{\text{COENB}}$	V_{CC}	$\overline{\text{RESET}}$	DIN7	DIN6	DIN3	DIN0	CIN8	V_{CC}	V_{SS}
B	V_{CC}	COUT7	COUT8	$\overline{\text{ERASE}}$	DIN8	DIN1	DIN2	$\overline{\text{CIENB}}$	CIN7	CIN6	CIN4
C	COUT5	COUT6	ALIGN PIN		$\overline{\text{DIENB}}$	DIN5	DIN4			CIN5	CIN3
D	COUT3	COUT4								CIN2	V_{CC}
E	COUT1	V_{SS}	COUT2						CIN1	CIN0	$\overline{\text{SENBL}}$
F	V_{SS}	COUT0	SHADD						SUM0	V_{CC}	V_{SS}
G	ADR2	DCM0	CLK						SUM1	SUM3	SUM2
H	ADR1	ADR0								SUM5	SUM4
J	V_{CC}	SUM25			SUM20	SUM17	SUM16			SUM7	V_{SS}
K	$\overline{\text{SENBH}}$	SUM24	V_{SS}	V_{CC}	SUM19	V_{SS}	SUM15	SUM12	SUM10	SUM8	SUM6
L	DCM1	SUM23	SUM22	SUM21	SUM18	SUM14	V_{CC}	SUM13	V_{SS}	SUM11	SUM9

HSP43891
TOP VIEW
PINS DOWN

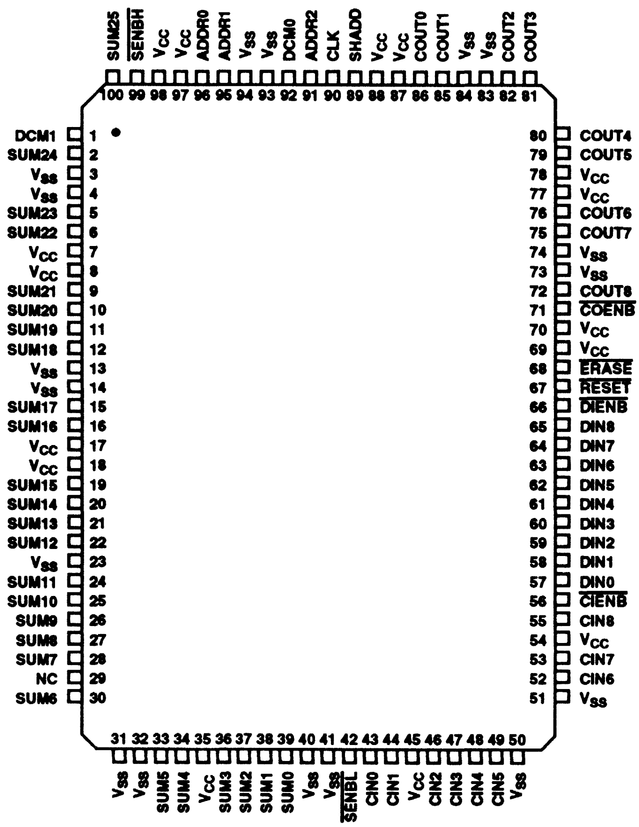


84 PIN PLASTIC LEADED CHIP CARRIER (PLCC)



Pinouts (Continued)

100 LEAD MQFP
TOP VIEW



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1D FILTERS

Pin Description

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
V_{CC}	B1, J1, A3, K4, L7, A10, F10, D11		+5 power supply input
V_{SS}	A1, F1, E2, K3, K6, L9, A11, E11, H11		Power supply ground input.
CLK	G3	I	The CLK input provides the DF system sample clock. The maximum clock frequency is 30MHz.
DIN0-8	A5-8, B5-7 C6, C7	I	These nine inputs are the data sample input bus. Nine-bit data samples are synchronously loaded through these pins to the X register of each filter cell of the DF simultaneously. The $\overline{\text{DIENB}}$ signal enables loading, which is synchronous on the rising edge of the clock signal. The data samples can be either 9-bit two's complement or 8-bit unsigned values. For 9-bit two's complement values, DIN8 is the sign bit. For 8-bit unsigned values, DIN8 must be held at logical zero.
$\overline{\text{DIENB}}$	C5	I	A low on this input enables the data sample input bus (DIN0-8) to all the filter cells. A rising edge of the CLK signal occurring while $\overline{\text{DIENB}}$ is low will load the X register of every filter cell with the 9-bit value present on DIN0-8. A high on this input forces all the bits of the data sample input bus to zero; a rising CLK edge when $\overline{\text{DIENB}}$ is high will load the X register of every filter cell with all zeros. This signal is latched inside the device, delaying its effect by one clock internal to the device. Therefore it must be low during the clock cycle immediately preceding presentation of the desired data on the DIN0-8 inputs. Detailed operation is shown in later timing diagrams.
CIN0-8	A9, B9-11, C10, C11, D10, E9, E10	I	These nine inputs are used to input the 9-bit coefficients. The coefficients are synchronously loaded into the C register of filter CELL0 if a rising edge of CLK occurs while $\overline{\text{CIENB}}$ is low. The $\overline{\text{CIENB}}$ signal is delayed by one clock as discussed below. The coefficients can be either 9-bit two's complement or 8-bit unsigned values. For 9-bit two's complement values, CIN8 is the sign bit. For 8-bit unsigned values, CIN8 must be held at logical zero.
ALIGN PIN	C3		Used for aligning chip on socket or printed circuit board. This pin must be left as a no connect in circuit.
$\overline{\text{CIENB}}$	B8	I	A low on this input enables the C register of every filter cell and the D (decimation) registers of every filter cell according to the state of the DCM0-1 inputs. A rising edge of the CLK signal occurring while $\overline{\text{CIENB}}$ is low will load the C register and appropriate D registers with the coefficient data present at their inputs. This provides the mechanism for shifting coefficients from cell to cell through the device. A high on this input freezes the contents of the C register and the D registers, ignoring the CLK signal. This signal is latched and delayed by one clock internal to the DF. Therefore it must be low during the clock cycle immediately preceding presentation of the desired coefficient on the CIN0-8 inputs. Detailed operation is shown in later timing diagrams.
COUT0-8	B2, B3, C1, D1, E1, C2, D2, F2, E3	O	These nine three-state outputs are used to output the 9-bit coefficients from filter CELL7. These outputs are enabled by the $\overline{\text{COENB}}$ signal low. These outputs may be tied to the CIN0-8 inputs of the same DF to recirculate to coefficients, or they may be tied to the CIN0-8 inputs of another DF to cascade DFs for longer filter lengths.
$\overline{\text{COENB}}$	A2	I	A low on the $\overline{\text{COENB}}$ input enables the COUT0-8 outputs. A high on this input places all these outputs in their high impedance state.
DCM0-1	L1, G2	I	These two inputs determine the use of the internal decimation registers as follows:

DCM1	DCM0	DECIMATION FUNCTION
0	0	Decimation registers not used
0	1	One decimation register is used
1	0	Two decimation registers are used
1	1	Three decimation registers are used

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
DCM0-1 (Cont.)	L1, G2	I	The coefficients pass from cell to cell at a rate determined by the number of decimation registers used. When no decimation registers are used, coefficients move from cell to cell on each clock. When one decimation register is used, coefficients move from cell to cell on every other clock, etc. These signals are latched and delayed by one clock internal to the device.
SUM0-25	J2, J5-8, J10, K2, K5-11 L2-6, L8, L10, L11	O	These 26 three-state outputs are used to output the results of the internal filter cell computations. Individual filter cell results or the result of the shift-and-add output stage can be output. If an individual filter cell result is to be output, the ADR0-2 signals select the filter cell result. The SHADD signal determines whether the selected filter cell result or the output stage adder result is output. The signals $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ enable the most significant and least significant bits of the SUM0-25 result respectively. Both $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ may be enabled simultaneously if the system has a 26-bit or larger bus. However individual enables are provided to facilitate use with a 16-bit bus.
$\overline{\text{SENBH}}$	K1	I	A low on this input enables result bits SUM16-25. A high on this input places these bits in their high impedance state.
$\overline{\text{SENBL}}$	E11	I	A low on this input enables result bits SUM0-15. A high on this input places these bits in their high impedance state.
ADR0-2	G1, H1, H2	I	These three inputs select the one cell whose accumulator will be read through the output bus (SUM0-25) or added to the output stage accumulator. They also determine which accumulator will be cleared when $\overline{\text{ERASE}}$ is low. These inputs are latched in the DF and delayed by one clock internal to the device. If ADR0-2 remains at the same address for more than one clock, the output at SUM0-25 will not change to reflect any subsequent accumulator updates in the addressed cell. Only the result available during the first clock, when ADR0-2 selects the cell, will be output. This does not hinder normal operation since the ADR0-2 lines are changed sequentially. This feature facilitates the interface with slow memories where the output is required to be fixed for more than one clock.
SHADD	F3	I	The SHADD input controls the activation of the shift and add operation in the output stage. This signal is latched on chip and delayed by one clock internal to the device. Detailed explanation is given in the DF Output Stage section.
$\overline{\text{RESET}}$	A4	I	A low on this input synchronously clears all the internal registers, except the cell accumulators It can be used with $\overline{\text{ERASE}}$ to also clear all the accumulators simultaneously. This signal is latched in the DF and delayed by one clock internal to the device.
$\overline{\text{ERASE}}$	B4	I	A low on this input synchronously clears the cell accumulator selected by the ADR0-2 signals. If $\overline{\text{RESET}}$ is also low simultaneously, all cell accumulators are cleared.

Functional Description

The Digital Filter Processor (DF) is composed of eight filter cells cascaded together and an output stage for combining or selecting filter cell outputs (See Block Diagram). Each filter cell contains a multiplier-accumulator and several registers (Figure 1). Each 9-bit coefficient is multiplied by a 9-bit data sample, with the result added to the 26-bit accumulator contents. The coefficient output of each cell is cascaded to the coefficient input of the next cell to its right.

DF Filter Cell

A 9-bit coefficient (CIN0-8) enters each cell through the C register on the left and exits the cell on the right as signals COUT0-8. With no decimation, the coefficient moves directly from the C register to the output, and is valid on the clock following its entrance. When decimation is selected the coefficient exit is delayed by 1, 2 or 3 clocks by passing through one or more decimation registers (D1, D2 or D3).

The combination of D registers through which the coefficient passes is determined by the state of DCM0 and DCM1. The output signals (COUT0-8) are connected to the CIN0-8 inputs of the next cell to its right. The $\overline{\text{COENB}}$ input signal enables the COUT0-8 outputs of the right most cell to the COUT0-8 pins of the device.

The C and D registers are enabled for loading by $\overline{\text{CIENB}}$. Loading is synchronous with CLK when $\overline{\text{CIENB}}$ is low. Note that $\overline{\text{CIENB}}$ is latched internally. It enables the register for loading after the next CLK following the onset of $\overline{\text{CIENB}}$ low. Actual loading occurs on the second CLK following the onset of $\overline{\text{CIENB}}$ low. Therefore $\overline{\text{CIENB}}$ must be low during the clock cycle immediately preceding presentation of the coefficient on the CIN0-8 inputs. In most basic FIR operations, $\overline{\text{CIENB}}$ will be low throughout the process, so this latching and delay sequence is only important during the initialization phase. When $\overline{\text{CIENB}}$ is high, the coefficients are frozen.

These registers are cleared synchronously under control of $\overline{\text{RESET}}$, which is latched and delayed exactly like $\overline{\text{CIENB}}$.

The output of the C register (C0-8) is one input to 9x9 multiplier.

The other input to the 9x9 multiplier comes from the output of the X register. This register is loaded with a data sample from the device input signals DIN0-8 discussed above. The X register is enabled for loading by $\overline{\text{DIENB}}$. Loading is synchronous with CLK when $\overline{\text{DIENB}}$ is low. Note that $\overline{\text{DIENB}}$ is latched internally. It enables the register for loading after the next CLK following the onset of $\overline{\text{DIENB}}$ low. Actual loading occurs on the second CLK following the onset of $\overline{\text{DIENB}}$ low; therefore, $\overline{\text{DIENB}}$ must be low during the clock cycle immediately preceding presentation of the data sample on the DIN0-8 inputs. In most basic FIR operations, $\overline{\text{DIENB}}$ will be low throughout the process, so this latching and delay sequence is only important during the initialization phase. When $\overline{\text{DIENB}}$ is high, the X register is loaded with all zeros.

The multiplier is pipelined and is modeled as a multiplier core followed by two pipeline registers, MREG0 and MREG1 (Figure 1). The multiplier output is sign extended and input as one operand of the 26-bit adder. The other adder operand is the output of the 26-bit accumulator. The adder output is loaded synchronously into both the accumulator and the TREG.

The TREG loading is disabled by the cell select signal, CELLn, where n is the cell number. The cell select is decoded from the ADR0-2 signals to generate the TREG load enable. The cell select is inverted and applied as the load enable to the TREG. Operation is such that the TREG is loaded whenever the cell is not selected. Therefore, TREG is loaded every clock except the clock following cell selection. The purpose of the TREG is to hold the result of a sum-of-products calculation during the clock when the accumulator is cleared to prepare for the next sum-of-products calculation. This allows continuous accumulation without wasting clocks.

The accumulator is loaded with the adder output every clock unless it is cleared. It is cleared synchronously in two ways. When $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ are both low, the accumulator is cleared along with all other registers on the device. Since $\overline{\text{ERASE}}$ and $\overline{\text{RESET}}$ are latched and delayed one clock internally, clearing occurs on the second CLK following the onset of both $\overline{\text{ERASE}}$ and $\overline{\text{RESET}}$ low.

The second accumulator clearing mechanism clears a single accumulator in a selected cell. The cell select signal, CELLn, decoded from ADR0-2 and the $\overline{\text{ERASE}}$ signal enable clearing of the accumulator on the next CLK.

The $\overline{\text{ERASE}}$ and $\overline{\text{RESET}}$ signals clear the DF internal registers and states as follows:

$\overline{\text{ERASE}}$	$\overline{\text{RESET}}$	CLEARING EFFECT
1	1	No clearing occurs, internal state remains same.
1	0	$\overline{\text{RESET}}$ only active, all registers except accumulators are cleared, including the internal pipeline registers.
0	1	$\overline{\text{ERASE}}$ only active, the accumulator whose address is given by the ADR0-2 inputs is cleared.
0	0	Both $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ active, all accumulators as well as all other registers are cleared.

The DF Output Stage

The output stage consists of a 26-bit adder, 26-bit register, feedback multiplexer from the register to the adder, an output multiplexer and a 26-bit three-state driver stage (Figure 2).

The 26-bit output adder can add any filter cell accumulator result to the 18 most significant bits of the output buffer. This result is stored back in the output buffer. This operation takes place in one clock period. The eight LSBs of the output buffer are lost. The filter cell accumulator is selected by the ADR0-2 inputs.

The 18 MSBs of the output buffer actually pass through the zero mux on their way to the output adder input. The zero mux is controlled by the SHADD input signal and selects either the output buffer 18 MSBs or all zeros for the adder input. A low on the SHADD input selects zero. A high on the SHADD input selects the output buffer MSBs, thus activating the shift-and-add operation. The SHADD signal is latched and delayed by one clock internally.

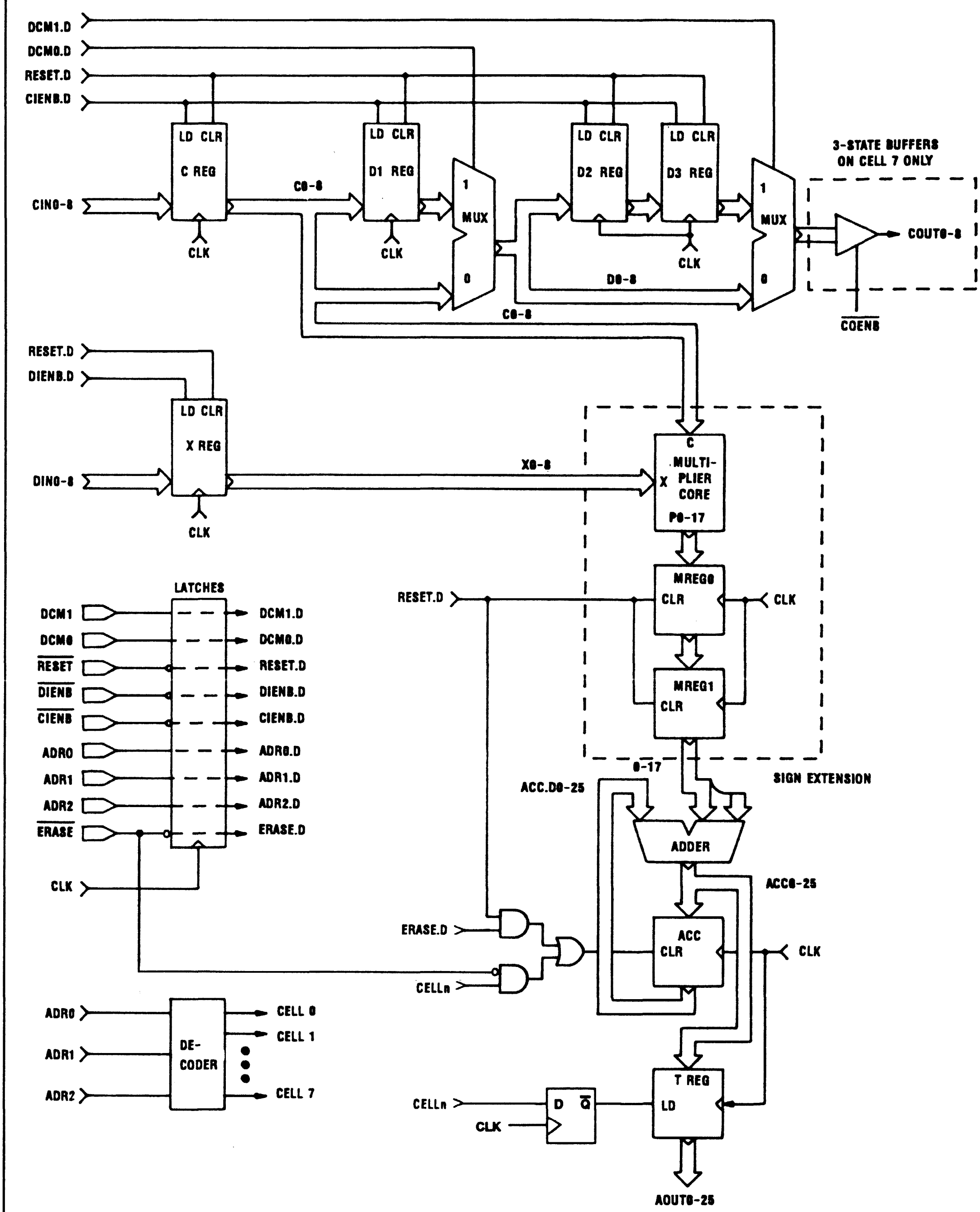


FIGURE 1. HSP43891 DF FILTER CELL

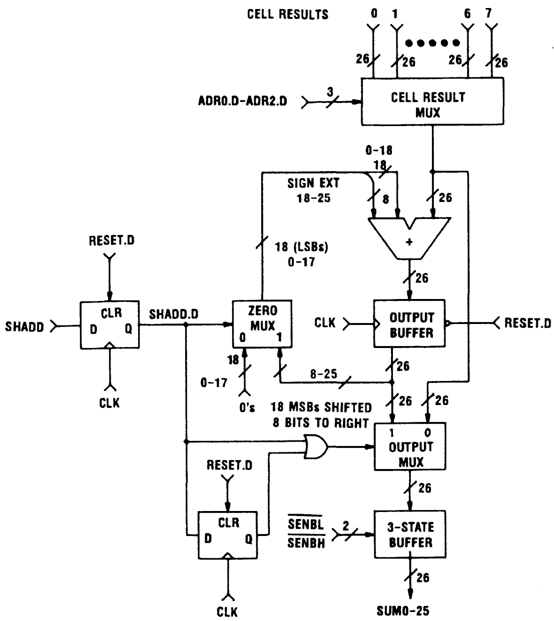


FIGURE 2. HSP43891 DFP OUTPUT STAGE

The 26 least significant bits (LSBs) from either a cell accumulator or the output buffer are output on the SUM0-25 bus. The output mux determines whether the cell accumulator selected by ADR0-2 or the output buffer is output to the bus. This mux is controlled by the SHADD input signal. Control is based on the state of the SHADD during two successive clocks; in other words, the output mux selection contains memory. If SHADD is low during a clock cycle and was low during the previous clock, the output mux selects the contents of the filter cell accumulator addressed by ADR0-2. Otherwise the output mux selects the contents of the output buffer.

If the ADR0-2 lines remain at the same address for more than one clock, the output at SUM0-25 will not change to reflect any subsequent accumulator updates in the addressed cell. Only the result available during the first clock when ADR0-2 selects the cell will be output. This does not hinder normal FIR operation since the ADR0-2 lines are changed sequentially. This feature facilitates the interface with slow memories where the output is required to be fixed for more than one clock.

The SUM0-25 output bus is controlled by the $\overline{SENBH}$ and $\overline{SENBL}$ signals. A low on $\overline{SENBL}$ enables bits SUM0-15. A low on $\overline{SENBH}$ enables bits SUM16-25. Thus all 26 bits can be output simultaneously if the external system has a 26-bit or larger bus. If the external system bus is only 16 bits, the bits can be enabled in two groups of 16 and 10 bits (sign extended).

DF Arithmetic

Both data samples and coefficients can be represented as either 8-bit unsigned or 9-bit two's complement numbers. The 9x9 bit multiplier in each cell expects 9-bit two's complement operands. The binary format of 8-bit two's complement is shown below. Note that if the most significant or sign bit is held at logical zero, the 9-bit two's complement multiplier can multiply 8-bit unsigned operands. Only the upper (positive) half of the two's complement binary range is used.

The multiplier output is 18 bits and the accumulator is 26 bits. The accumulator width determines the maximum possible number of terms in the sum of products without overflow. The maximum number of terms depends also on the number system and the distribution of the coefficient and data values. Then maximum numbers of terms in the sum products are:

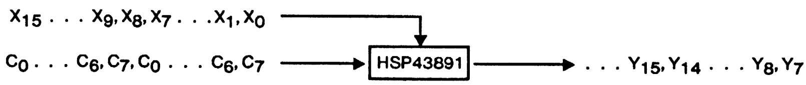
NUMBER SYSTEM	MAX # OF TERMS	
	8-BIT	9-BIT
Two unsigned vectors	1032	N/A
Two two's complement vectors:		
• Two positive vectors	2080	1032
• Negative vectors	2047	1024
• One positive and one negative vector	2064	1028
One unsigned 8 bit vector and one two's complement vector:		
• Postive two's complement vector	1036	1032
• Negative two's complement vector	1028	1028

For practical FIR filters, the coefficients are never all near maximum value, so even larger vectors are possible in practice.

Basic FIR Operation

A simple, 30MHz 8-tap filter example serves to illustrate more clearly the operation of the DF. The sequence table (Table 1) shows the results of the multiply accumulate in each cell after each clock. The coefficient sequence, Cn, enters the DF on the left and moves from left to right through the cells. The data sample sequence, Xn, enters the DF from the top, with each cell receiving the same sample simultaneously. Each cell accumulates the sum of products for one output point. Eight sums of products are calculated simultaneously, but staggered in time so that a new output is available every system clock.

TABLE 1. HSP43891 30MHz, 8-TAP FIR FILTER SEQUENCE



CLK	CELL 0	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7	SUM/CLR
0	$C_7 \times X_0$	0	0	0	-	-	-	-	-
1	$+C_6 \times X_1$	$C_7 \times X_1$	0	0	-	-	-	-	-
2	$+C_5 \times X_2$	$+C_6 \times X_2$	$C_7 \times X_2$	0	-	-	-	-	-
3	$+C_4 \times X_3$	$+C_5 \times X_3$	$+C_6 \times X_3$	$C_7 \times X_3$	-	-	-	-	-
4	$+C_3 \times X_4$	$+C_4 \times X_4$	$+C_5 \times X_4$	$+C_6 \times X_4$	$C_7 \times X_4$	-	-	-	-
5	$+C_2 \times X_5$	$+C_3 \times X_5$	$+C_4 \times X_5$	$+C_5 \times X_5$	$+C_6 \times X_5$	$C_7 \times X_5$	-	-	-
6	$+C_1 \times X_6$	$+C_2 \times X_6$	$+C_3 \times X_6$	$+C_4 \times X_6$	$+C_5 \times X_6$	$+C_6 \times X_6$	$C_7 \times X_6$	-	-
7	$+C_0 \times X_7$	$+C_1 \times X_7$	$+C_2 \times X_7$	$+C_3 \times X_7$	$+C_4 \times X_7$	$+C_5 \times X_7$	$+C_6 \times X_7$	$C_7 \times X_7$	Cell 0 (Y7)
8	$C_7 \times X_8$	$+C_0 \times X_8$	$+C_1 \times X_8$	$+C_2 \times X_8$	$+C_3 \times X_8$	$+C_4 \times X_8$	$+C_5 \times X_8$	$+C_6 \times X_8$	Cell 1 (Y8)
9	$+C_6 \times X_9$	$C_7 \times X_9$	$+C_0 \times X_9$	$+C_1 \times X_9$	$+C_2 \times X_9$	$+C_3 \times X_9$	$+C_4 \times X_9$	$+C_5 \times X_9$	Cell 2 (Y9)
10	$+C_5 \times X_{10}$	$+C_6 \times X_{10}$	$C_7 \times X_{10}$	$+C_0 \times X_{10}$	$+C_1 \times X_{10}$	$+C_2 \times X_{10}$	$+C_3 \times X_{10}$	$+C_4 \times X_{10}$	Cell 3 (Y10)
11	$+C_4 \times X_{11}$	$+C_5 \times X_{11}$	$+C_6 \times X_{11}$	$C_7 \times X_{11}$	$+C_0 \times X_{11}$	$+C_1 \times X_{11}$	$+C_2 \times X_{11}$	$+C_3 \times X_{11}$	Cell 4 (Y11)
12	$+C_3 \times X_{12}$	$+C_4 \times X_{12}$	$+C_5 \times X_{12}$	$+C_6 \times X_{12}$	$C_7 \times X_{12}$	$+C_0 \times X_{12}$	$+C_1 \times X_{12}$	$+C_2 \times X_{12}$	Cell 5 (Y12)
13	$+C_2 \times X_{13}$	$+C_3 \times X_{13}$	$+C_4 \times X_{13}$	$+C_5 \times X_{13}$	$+C_6 \times X_{13}$	$C_7 \times X_{13}$	$+C_0 \times X_{13}$	$+C_1 \times X_{13}$	Cell 6 (Y13)
14	$+C_1 \times X_{14}$	$+C_2 \times X_{14}$	$+C_3 \times X_{14}$	$+C_4 \times X_{14}$	$+C_5 \times X_{14}$	$+C_6 \times X_{14}$	$+C_7 \times X_{14}$	$+C_0 \times X_{14}$	Cell 7 (Y14)
15	$+C_0 \times X_{15}$	$+C_1 \times X_{15}$	$+C_2 \times X_{15}$	$+C_3 \times X_{15}$	$+C_4 \times X_{15}$	$+C_5 \times X_{15}$	$+C_6 \times X_{15}$	$C_7 \times X_{15}$	Cell 0 (Y15)

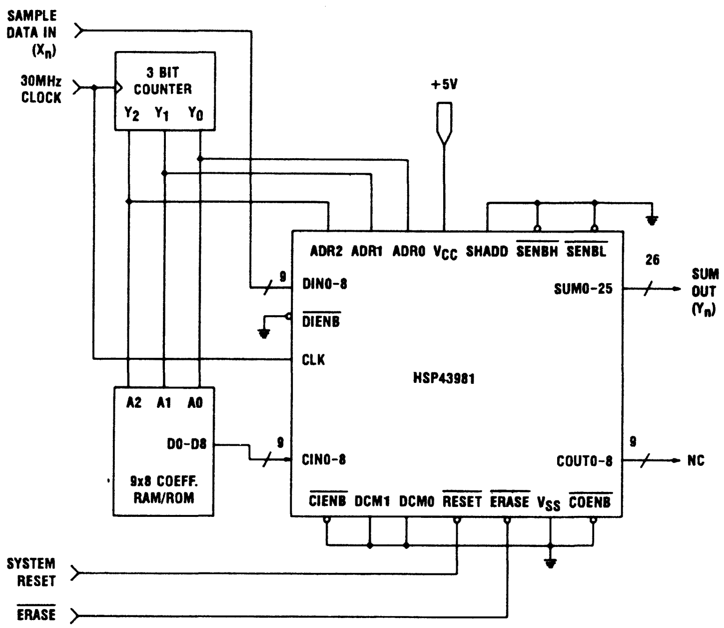


FIGURE 3. HSP43891 30MHz, 8-TAP FIR FILTER APPLICATION SCHEMATIC

3

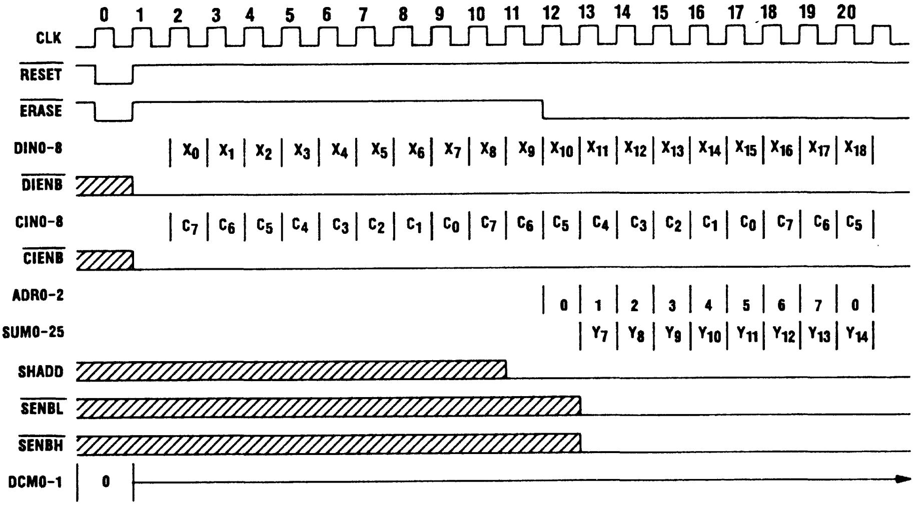
1D FILTERS

Detailed operation of the DF to perform a basic 8-tap, 9-bit coefficient, 9-bit data, 30MHz FIR filter is best understood by observing the schematic (Figure 3) and timing diagram (Figure 4). The internal pipeline length of the DF is four (4) clock cycles, corresponding to the register levels CREG (or XREG), MREG0, MREG1, and TREG (Figures 1 and 2). Therefore the delay from presentation of data and coefficients at the DIN0-8 and CIN0-8 inputs to a sum appearing at the SUM0-25 output is: k + Td, where k = filter length and Td = 4, the internal pipeline delay of the DF.

After the pipeline has filled, a new output sample is available every clock. The delay to last sample output from last sample input is Td.

The output sums, Yn, shown in the timing diagram are derived from the sum-of-products equation:

$Y(n) = C(0) \times X(n) + C(1) \times X(n-1) + C(2) \times X(n-2) + C(3) \times X(n-3) + C(4) \times X(n-4) + C(5) \times X(n-5) + C(6) \times X(n-6) + C(7) \times X(n-7)$



$$Y_N = \sum_{K=0}^{7} C_K \times X_{N-K}$$

FIGURE 4. HSP43891 30MHz, 8-TAP FIR FILTER TIMING

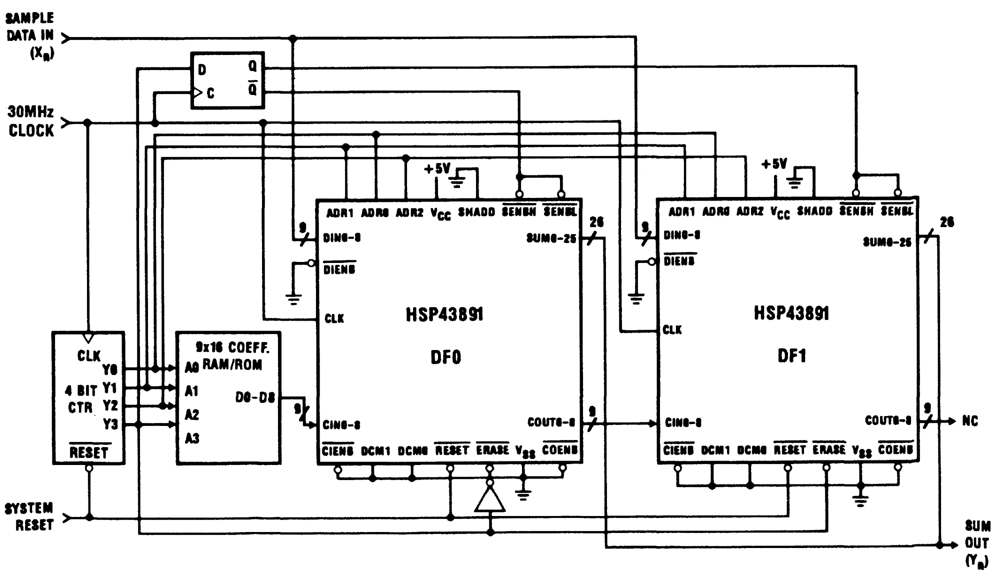


FIGURE 5. HSP43891 30MHz, 16-TAP FIR FILTER CASCADE APPLICATION SCHEMATIC

Extended FIR Filter Length

Filter lengths greater that eight taps can be created by either cascading together multiple DF devices or "reusing" a single device. Using multiple devices, an FIR filter of over 1000 taps can be constructed to operate at a 30MHz sample rate. Using a single device clocked at 30MHz, an FIR filter of over 500 taps can be constructed to operate at less than a 30MHz sample rate. Combinations of these two techniques are also possible.

Cascade Configuration

To design a filter length L>8, L/8 DFs are cascaded by connecting the COUT0-8 outputs of the (i)th DF to the CIN0-8 inputs of the (i+1)th DF. The DIN0-8 inputs and SUM0-25 outputs of all the DFs are also tied together. A specific example of two cascaded DFs illustrates the technique (Figure 5). Timing (Figure 6) is similar to the simple 8-tap FIR, except the $\overline{\text{ERASE}}$ and $\overline{\text{SENBL}}/\overline{\text{SENBH}}$ signals must be enabled independently for the two DFs in order to clear the correct accumulators and enable the SUM0-25 output signals at the proper times.

TABLE 2.

DATA SEQUENCE INPUT $X_{30} \ldots X_9, X_8, X_{22} \ldots X_1, X_0$ → HSP43891

COEFFICIENT SEQUENCE INPUT $C_0 \ldots C_{14}, C_{15}, 0 \ldots 0, C_0 \ldots C_{14}, C_{15}$ → HSP43891 → $\ldots 0, Y_{30} \ldots Y_{23}, 0 \ldots 0, Y_{22} \ldots Y_{15}, 0 \ldots 0$

CLK	CELL 0	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7	SUM/CLR
6	$C_{15} \times X_0$	0	0	0	-	-	-	-	-
7	$+C_{14} \times X_1$	$C_{15} \times X_1$	0	0	-	-	-	-	-
8	$+C_{13} \times X_2$		$C_{15} \times X_2$	0	-	-	-	-	-
9	$+C_{12} \times X_3$			$C_{15} \times X_3$	-	-	-	-	-
10	$+C_{11} \times X_4$			$+C_{14} \times X_4$	$C_{15} \times X_4$	-	-	-	-
11	$+C_{10} \times X_5$			$+C_{13} \times X_5$		$C_{15} \times X_5$	-	-	-
12	$+C_9 \times X_6$			$+C_{12} \times X_6$			$C_{15} \times X_6$	-	-
13	$+C_8 \times X_7$			$+C_{11} \times X_7$				$C_{15} \times X_7$	-
14	$+C_7 \times X_8$			$+C_{10} \times X_8$				$+C_{14} \times X_8$	-
15	$+C_6 \times X_9$			$+C_9 \times X_9$				$+C_{13} \times X_9$	-
16	$+C_5 \times X_{10}$			$+C_8 \times X_{10}$				$+C_{12} \times X_{10}$	-
17	$+C_4 \times X_{11}$			$+C_7 \times X_{11}$				$+C_{11} \times X_{11}$	-
18	$+C_3 \times X_{12}$			$+C_6 \times X_{12}$				$+C_{10} \times X_{12}$	-
19	$+C_2 \times X_{13}$			$+C_5 \times X_{13}$				$+C_9 \times X_{13}$	-
20	$+C_1 \times X_{14}$			$+C_4 \times X_{14}$				$+C_8 \times X_{14}$	-
21	$+C_0 \times X_{15}$			$+C_3 \times X_{15}$				$+C_7 \times X_{15}$	Cell 0(Y15)
22	0	$C_0 \times X_{16}$		$+C_2 \times X_{16}$				$+C_6 \times X_{16}$	Cell 1(Y16)
23	0	0	$C_0 \times X_{17}$	$+C_1 \times X_{17}$				$+C_5 \times X_{17}$	Cell 2(Y17)
24	0	0	0	$+C_0 \times X_{18}$				$+C_4 \times X_{18}$	Cell 3(Y18)
25	0	0	0	0	$C_0 \times X_{19}$			$+C_3 \times X_{19}$	Cell 4(Y19)
26	0	0	0	0	0	$C_0 \times X_{20}$		$+C_2 \times X_{20}$	Cell 5(Y20)
27	0	0	0	0	0	0	$C_0 \times X_{21}$	$+C_1 \times X_{21}$	Cell 6(Y21)
28	0	0	0	0	0	0	0	$+C_0 \times X_{22}$	Cell 7(Y22)
29	$C_{15} \times X_8$	0	0	0	0	0	0	0	-
30	$+C_{14} \times X_9$	$+C_{15} \times X_9$	0	0	0	0	0	0	-
31	$+C_{13} \times X_{10}$		$+C_{15} \times X_{10}$	0	0	0	0	0	-
32	$+C_{12} \times X_{11}$			$+C_{15} \times X_{11}$	0	0	0	0	-
33	$+C_{11} \times X_{12}$				$+C_{15} \times X_{12}$	0	0	0	-
34	$+C_{10} \times X_{13}$					$+C_{15} \times X_{12}$	0	0	-
35	$+C_9 \times X_{14}$						$+C_{15} \times X_{14}$	0	-
36	$+C_8 \times X_{15}$							$C_{15} \times X_{15}$	-
37	$+C_7 \times X_{16}$							$+C_{14} \times X_{16}$	-
38	$+C_6 \times X_{17}$							$+C_{13} \times X_{17}$	-
39	$+C_5 \times X_{18}$							$+C_{12} \times X_{18}$	-
40	$+C_4 \times X_{19}$							$+C_{11} \times X_{19}$	-
41	$+C_3 \times X_{20}$							$+C_{10} \times X_{20}$	-
42	$+C_2 \times X_{21}$							$+C_9 \times X_{21}$	-
43	$+C_1 \times X_{22}$							$+C_8 \times X_{22}$	-
44	$+C_0 \times X_{23}$							$+C_7 \times X_{23}$	Cell 0(Y23)
45	0	$C_0 \times X_{23}$						$+C_6 \times X_{24}$	Cell 1(Y24)
46	0	0	$C_0 \times X_{25}$					$+C_5 \times X_{25}$	Cell 2(Y25)
47	0	0	0	$C_0 \times X_{26}$				$+C_4 \times X_{26}$	Cell 3(Y26)
48	0	0	0	0	$C_0 \times X_{27}$			$+C_3 \times X_{27}$	Cell 4(Y27)

3

1D FILTERS

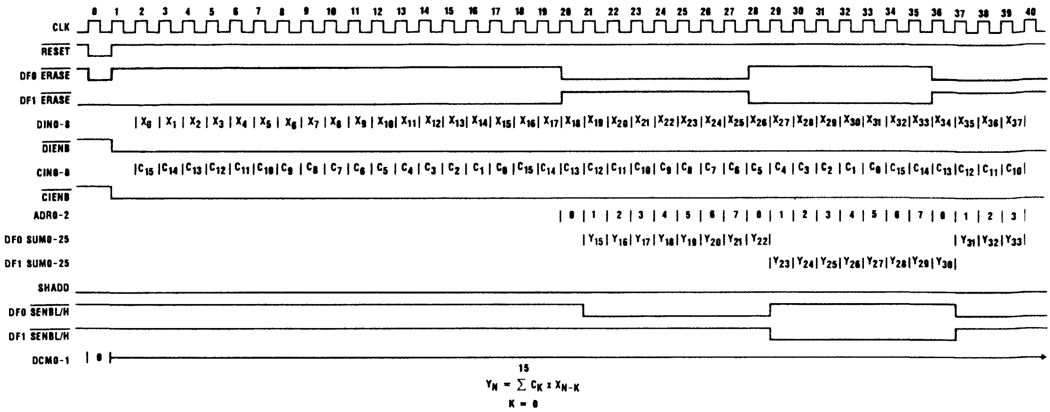


FIGURE 6. HSP43891 16-TAP 30MHz FILTER TIMING USING TWO CASCADED HSP43891s

Single DF Configuration

Using a single DF, a filter of length L>8 can be constructed by processing in L/8 passes, as illustrated in Table 2, for a 16-tap FIR. Each pass is composed of Tp = 7 + L cycles and computes eight output samples. In pass i, the sample with indices i*8 to i*8 +(L-1) enter the DIN0-8 inputs. The coefficients C_0 - C_{L-1} enter the CIN0-8 inputs, followed by seven zeros. As these zeros are entered, the result samples are output and the accumulators reset. Initial filing of the pipeline is not shown in this sequence table. Filter outputs can be put through a FIFO to even out the sample rate.

Extended Coefficient and Data Sample Word Size

The sample and coefficient word size can be extended by utilizing several DFs in parallel to get the maximum sample rate or a single DF with resulting lower sample rates. The technique is to compute partial products of 9x9 and combine these partial products by shifting and adding to obtain the final result. The shifting and adding can be accomplished with external adders (at full speed) or with the DF's shift-and-add mechanism contained in its output stage (at reduced speed).

Decimation/Resampling

The HSP43891 DF provides a mechanism for decimating by factors of 2, 3, or 4. From the DF filter cell block diagram (Figure 1), note the three D registers and two multiplexers in the coefficient path through the cell. These allow the coefficients to be delayed by 1, 2, or 3 clocks through the cell. The sequence table (Table 3) for a decimate-by-two-filter illustrates the technique (internal cell pipelining ignored for simplicity).

Detailed timing for a 30MHz input sample rate, 15MHz output sample rate (i.e., decimate-by-two), 16-tap FIR filter, including pipelining, is shown in Figure 7. This filter requires only a single HSP43891 DF.

TABLE 3. HSP43891 16-TAP DECIMATE-BY-TWO FIR FILTER SEQUENCE; 30MHz IN, 15MHz OUT

DATA SEQUENCE INPUT $\ldots X_2, X_1, X_0$

COEFFICIENT SEQUENCE INPUT $\ldots C_{15}, C_0, \ldots C_{13}, C_{14}, C_{15} \rightarrow$ HSP43891 $\rightarrow \ldots Y_{19}, -, Y_{17}, -, Y_{15}$

CLK	CELL 0	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7	SUM/CLR
6	$C_{15} \times X_0$	0	0	0	0	0	0	0	-
7	$+C_{14} \times X_1$	0	0	0	0	0	0	0	-
8	$+C_{13} \times X_2$	$C_{15} \times X_2$	0	0	0	0	0	0	-
9	$+C_{12} \times X_3$	$+C_{14} \times X_3$	0	0	0	0	0	0	-
10	$+C_{11} \times X_4$	$+C_{13} \times X_4$	$C_{15} \times X_4$	0	0	0	0	0	-
11	$+C_{10} \times X_5$	$+C_{12} \times X_5$	$+C_{14} \times X_5$	0	0	0	0	0	-
12	$+C_9 \times X_6$	$+C_{11} \times X_6$	$+C_{13} \times X_6$	$C_{15} \times X_6$	0	0	0	0	-
13	$+C_8 \times X_7$	$+C_{10} \times X_7$	$+C_{12} \times X_7$	$+C_{14} \times X_7$	0	0	0	0	-
14	$+C_7 \times X_8$	$+C_9 \times X_8$	$+C_{11} \times X_8$	$+C_{13} \times X_8$	$C_{15} \times X_8$	0	0	0	-
15	$+C_6 \times X_9$	$+C_8 \times X_9$	$+C_{10} \times X_9$	$+C_{12} \times X_9$	$+C_{14} \times X_9$	0	0	0	-
16	$+C_5 \times X_{10}$	$+C_7 \times X_{10}$	$+C_9 \times X_{10}$	$+C_{11} \times X_{10}$	$+C_{13} \times X_{10}$	$C_{15} \times X_{10}$	0	0	-
17	$+C_4 \times X_{11}$	$+C_6 \times X_{11}$	$+C_8 \times X_{11}$	$+C_{10} \times X_{11}$	$+C_{12} \times X_{11}$	$+C_{14} \times X_{11}$	0	0	-
18	$+C_3 \times X_{12}$	$+C_5 \times X_{12}$	$+C_7 \times X_{12}$	$+C_9 \times X_{12}$	$+C_{11} \times X_{12}$	$+C_{13} \times X_{12}$	$C_{15} \times X_{12}$	0	-
19	$+C_2 \times X_{13}$	$+C_4 \times X_{13}$	$+C_6 \times X_{13}$	$+C_8 \times X_{13}$	$+C_{10} \times X_{13}$	$+C_{12} \times X_{13}$	$+C_{14} \times X_{13}$	0	-
20	$+C_1 \times X_{14}$	$+C_3 \times X_{14}$	$+C_5 \times X_{14}$	$+C_7 \times X_{14}$	$+C_9 \times X_{14}$	$+C_{11} \times X_{14}$	$+C_{13} \times X_{14}$	$C_{15} \times X_{14}$	-
21	$+C_0 \times X_{15}$	$+C_2 \times X_{15}$	$+C_4 \times X_{15}$	$+C_6 \times X_{15}$	$+C_8 \times X_{15}$	$+C_{10} \times X_{15}$	$+C_{12} \times X_{15}$	$+C_{14} \times X_{15}$	Cell 0(Y15)
22	$C_{15} \times X_{16}$	$+C_1 \times X_{16}$	$+C_3 \times X_{16}$	$+C_5 \times X_{16}$	$+C_7 \times X_{16}$	$+C_9 \times X_{16}$	$+C_{11} \times X_{16}$	$+C_{13} \times X_{16}$	-
23	$+C_{14} \times X_{17}$	$+C_0 \times X_{17}$	$+C_2 \times X_{17}$	$+C_4 \times X_{17}$	$+C_6 \times X_{17}$	$+C_8 \times X_{17}$	$+C_{10} \times X_{17}$	$+C_{12} \times X_{17}$	Cell 1(Y17)
24	$+C_{13} \times X_{18}$	$C_{15} \times X_{18}$	$+C_1 \times X_{18}$	$+C_3 \times X_{18}$	$+C_5 \times X_{18}$	$+C_7 \times X_{18}$	$+C_9 \times X_{18}$	$+C_{11} \times X_{18}$	-
25	$+C_{12} \times X_{19}$	$+C_{14} \times X_{19}$	$+C_0 \times X_{19}$	$+C_2 \times X_{19}$	$+C_4 \times X_{19}$	$+C_6 \times X_{19}$	$+C_8 \times X_{19}$	$+C_{10} \times X_{19}$	Cell 2(Y19)
26	$+C_{11} \times X_{20}$	$+C_{13} \times X_{20}$	$C_{15} \times X_{20}$	$+C_1 \times X_{20}$	$+C_3 \times X_{20}$	$+C_5 \times X_{20}$	$+C_7 \times X_{20}$	$+C_9 \times X_{20}$	-
27	$+C_{10} \times X_{21}$	$+C_{12} \times X_{21}$	$+C_{14} \times X_{21}$	$+C_0 \times X_{21}$	$+C_2 \times X_{21}$	$+C_4 \times X_{21}$	$+C_6 \times X_{21}$	$+C_8 \times X_{21}$	Cell 3(Y21)
28	$+C_9 \times X_{22}$	$+C_{11} \times X_{22}$	$+C_{13} \times X_{22}$	$C_{15} \times X_{22}$	$+C_1 \times X_{22}$	$+C_3 \times X_{22}$	$+C_5 \times X_{22}$	$+C_7 \times X_{22}$	-
29	$+C_8 \times X_{23}$	$+C_{10} \times X_{23}$	$+C_{12} \times X_{23}$	$+C_{14} \times X_{23}$	$+C_0 \times X_{23}$	$+C_2 \times X_{23}$	$+C_4 \times X_{23}$	$+C_6 \times X_{23}$	Cell 4(Y23)
30	$+C_7 \times X_{24}$	$+C_9 \times X_{24}$	$+C_{11} \times X_{24}$	$+C_{13} \times X_{24}$	$+C_{15} \times X_{24}$	$+C_1 \times X_{24}$	$+C_3 \times X_{24}$	$+C_5 \times X_{24}$	-
31	$+C_6 \times X_{25}$	$+C_8 \times X_{25}$	$+C_{10} \times X_{25}$	$+C_{12} \times X_{25}$	$+C_{14} \times X_{25}$	$+C_0 \times X_{25}$	$+C_2 \times X_{25}$	$+C_4 \times X_{25}$	Cell 5(Y25)
32	$+C_5 \times X_{26}$	$+C_7 \times X_{26}$	$+C_9 \times X_{26}$	$+C_{11} \times X_{26}$	$+C_{13} \times X_{26}$	$+C_{15} \times X_{26}$	$+C_1 \times X_{26}$	$+C_3 \times X_{26}$	-
33	$+C_4 \times X_{27}$	$+C_6 \times X_{27}$	$+C_8 \times X_{27}$	$+C_{10} \times X_{27}$	$+C_{12} \times X_{27}$	$+C_{14} \times X_{27}$	$+C_0 \times X_{27}$	$+C_2 \times X_{27}$	Cell 6(Y27)
34	$+C_3 \times X_{28}$	$+C_5 \times X_{28}$	$+C_7 \times X_{28}$	$+C_9 \times X_{28}$	$+C_{11} \times X_{28}$	$+C_{13} \times X_{28}$	$+C_{15} \times X_{28}$	$+C_1 \times X_{28}$	-
35	$+C_2 \times X_{29}$	$+C_4 \times X_{29}$	$+C_6 \times X_{29}$	$+C_8 \times X_{29}$	$+C_{10} \times X_{29}$	$+C_{12} \times X_{29}$	$+C_{14} \times X_{29}$	$+C_0 \times X_{29}$	Cell 7(Y29)
36	$+C_1 \times X_{30}$	$+C_3 \times X_{30}$	$+C_5 \times X_{30}$	$+C_7 \times X_{30}$	$+C_9 \times X_{30}$	$+C_{11} \times X_{30}$	$+C_{13} \times X_{30}$	$C_{15} \times X_{30}$	-
37	$+C_0 \times X_{31}$	$+C_2 \times X_{31}$	$+C_4 \times X_{31}$	$+C_6 \times X_{31}$	$+C_8 \times X_{31}$	$+C_{10} \times X_{31}$	$+C_{12} \times X_{31}$	$+C_{14} \times X_{31}$	Cell 8(Y31)

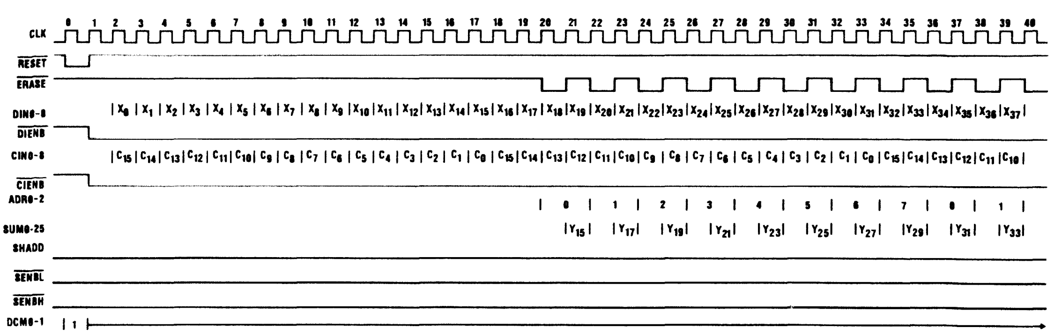


FIGURE 7. HSP43891 16-TAP DECIMATE-BY-TWO FIR FILTER TIMING; 30MHz IN, 15MHz OUT

3 1D FILTERS

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output Voltage .... GND -0.5V to V_{CC} +0.5V
Storage Temperature .... -65°C to +150°C
ESD .... Class 1
Maximum Package Power Dissipation at 70°C .... 1.7W (MQFP), 2.4W (PLCC), 2.88W (PGA)
θ_{jc} .... 11.1°C/W (PLCC), 7.78°C/W (PGA)
θ_{ja} .... 47°C/W (MQFP), 33.7°C/W (PLCC), 34.66°C/W (PGA)
Gate Count 17763
Junction Temperature .... 150°C (PLCC), 175°C (PGA)
Lead Temperature (Soldering 10s) .... 300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... 5V ±5%
Operating Temperature Range .... 0°C to +70°C

D.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
I_{CCOP}	Power Supply Current	-	140	mA	V_{CC} = Max CLK Frequency 20MHz Note 1, Note 3
I_{CCSB}	Standby Power Supply Current	-	500	µA	V_{CC} = Max, Note 3
I_I	Input Leakage Current	-10	10	µA	V_{CC} = Max, Input = 0V or V_{CC}
I_O	Output Leakage Current	-10	10	µA	V_{CC} = Max, Input = 0V or V_{CC}
V_{IH}	Logical One Input Voltage	2.0	-	V	V_{CC} = Max
V_{IL}	Logical Zero Input Voltage		0.8	V	V_{CC} = Min
V_{OH}	Logical One Output Voltage	2.6	-	V	I_{OH} = -400µA, V_{CC} = Min
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} = 2mA, V_{CC} = Min
V_{IHC}	Clock Input High	3.0	-	V	V_{CC} = Max
V_{ILC}	Clock Input Low	-	0.8	V	V_{CC} = Min
C_{IN}	Input Capacitance PLCC PGA	- -	10 15	pF pF	CLK Frequency 1MHz All measurements referenced to GND T_A = 25°C. Note 2
C_{OUT}	Output Capacitance PLCC PGA	- -	10 15	pF pF	

NOTES: 1. Operating supply current is proportional to frequency. Typical rating is 7mA/MHz.

2. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

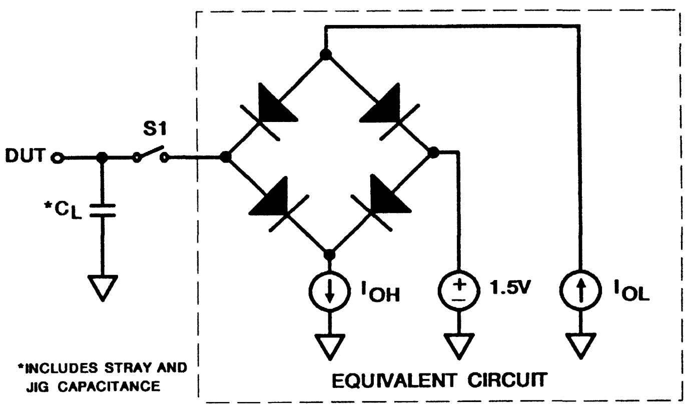
3. Output load per test load circuit and C_L = 40pF.

A.C. Electrical Specifications V_{CC} = 5V ± 5%, T_A = 0°C to +70°C

SYMBOL	PARAMETER	-20 (20MHz)		-25 (25.6MHz)		-30 (30MHz)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
T_{CP}	Clock Period	50	-	39	-	33	-	ns	
T_{CL}	Clock Low	20	-	16	-	13	-	ns	
T_{CH}	Clock High	20	-	16	-	13	-	ns	
T_{IS}	Input Setup	16	-	14	-	13	-	ns	
T_{IH}	Input Hold	0	-	0	-	0	-	ns	
T_{ODC}	CLK to Coefficient Output Delay	-	24	-	20	-	18	ns	
T_{OED}	Output Enable Delay	-	20	-	15	-	15	ns	
T_{ODD}	Output Disable Delay	-	20	-	15	-	15	ns	Note 1
T_{ODS}	CLK to SUM Output Delay	-	27	-	25	-	21	ns	
T_{OR}	Output Rise	-	6	-	6	-	6	ns	Note 1
T_{OF}	Output Fall	-	6	-	6	-	6	ns	Note 1

NOTE: 1. Controlled by design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

Test Load Circuit

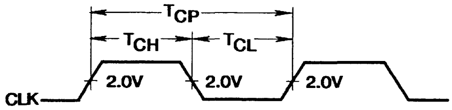


Switch S1 Open for I_{CCSB} and I_{CCOP} Tests

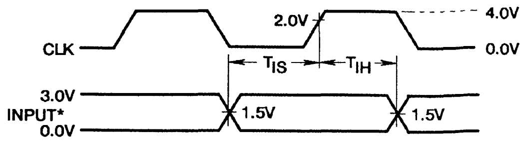
3

1D FILTERS

Waveforms

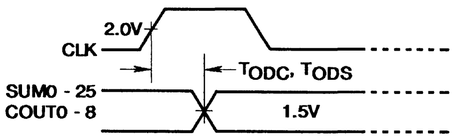


CLOCK AC PARAMETERS

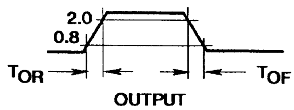


* Input includes: DIN0-7, CIN0-7, DIENB, CIENB, ERASE, RESET, DCM0-1, ADR0-1, TCS, TCCI, SHADD

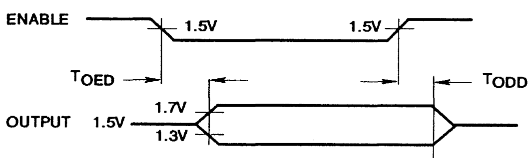
INPUT SETUP AND HOLD



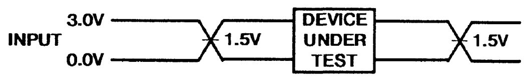
SUM0-25, COUT0-8, OUTPUT DELAYS



RISE AND FALL TIMES



OUTPUT ENABLE, DISABLE TIMING



A.C. Testing: Inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a Logic "1" and "0". CLK is driven at 4.0V and 0V and measured at 2.0V.

A.C. TESTING INPUT, OUTPUT WAVEFORM

HARRIS SEMICONDUCTOR

HSP43891/883

January 1994

Digital Filter

Features

- This Circuit Is Processed In Accordance to MIL-STD-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- 0MHz to 25.6MHz Sample Rate
- Eight Filter Cells
- 9-Bit Coefficients and Signal Data
- Low Power CMOS Operation
  - I_{CCSB} = 500μA Maximum
  - I_{CCOP} = 160μA Maximum at 20MHz
- 26-Bit Accumulator per Stage
- Filter Lengths Up to 1032 Taps
- Expandable Coefficient Size, Data Size and Filter Length
- Decimation by 2, 3 or 4

Applications

- 1-D and 2-D FIR Filters
- Radar/Sonar
- Digital Video
- Adaptive Filters
- Echo Cancellation
- Complex Multiply-Add
- Sample Rate Converters

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43891GM-20/883	-55°C to +125°C	85 Lead PGA
HSP43891GM-25/883	-55°C to +125°C	85 Lead PGA

Description

The HSP43891/883 is a video-speed Digital Filter (DF) designed to efficiently implement vector operations such as FIR digital filters. It is comprised of eight filter cells cascaded internally and a shift and add output stage, all in a single integrated circuit. Each filter cell contains a 9 x 9 two's complement multiplier, three decimation registers and a 26-bit accumulator. The output stage contains an additional 26-bit accumulator which can add the contents of any filter cell accumulator to the output stage accumulator shifted right by 8-bits. The HSP43891/883 has a maximum sample rate of 25.6MHz. The effective multiply-accumulate (mac) rate is 204MHz.

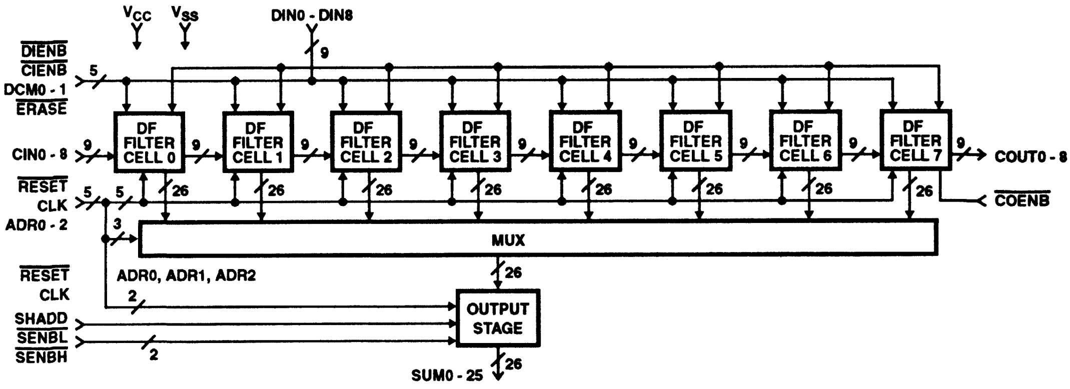
The HSP43891/883 DF can be configured to process expanded coefficient and word sizes. Multiple DFs can be cascaded for larger filter lengths without degrading the sample rate or a single DF can process larger filter lengths at less than 25.6MHz with multiple passes. The architecture permits processing filter lengths of over 1000 taps with the guarantee of no overflows. In practice, most filter coefficients are less than 1.0, making even larger filter lengths possible. The DF provides for 8-bit unsigned or 9-bit two's complement arithmetic, independently selectable for coefficients and signal data.

Each DF filter cell contains three re-sampling or decimation registers which permit output sample rate reduction at rates of 1/2, 1/3 or 1/4 the input sample rate. These registers also provide the capability to perform 2-D operations such as matrix multiplication and N x N spatial correlations/convolutions for image processing applications.

3

1D FILTERS

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

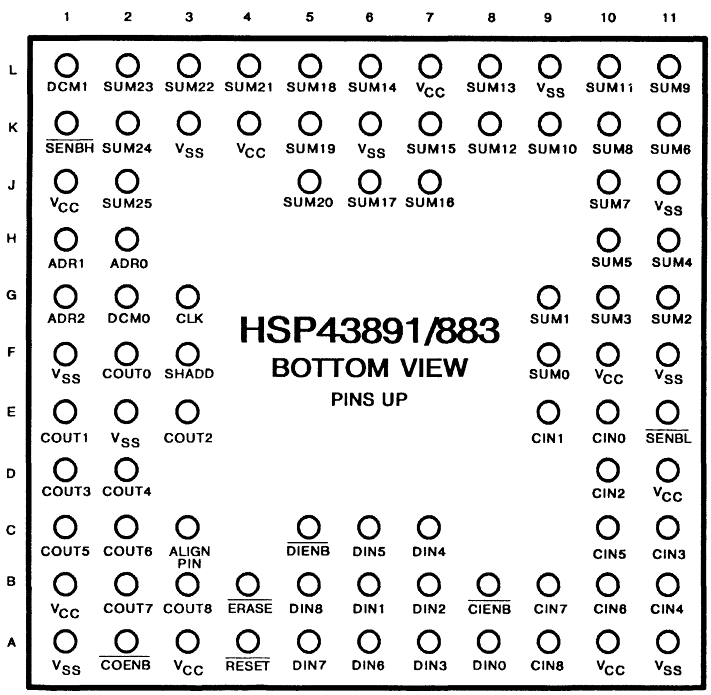
File Number 2451.3

Pinouts

85 PIN GRID ARRAY (PGA)

	1	2	3	4	5	6	7	8	9	10	11
A	V_{SS}	$\overline{\text{COENB}}$	V_{CC}	$\overline{\text{RESET}}$	DIN7	DIN6	DIN3	DIN0	CIN8	V_{CC}	V_{SS}
B	V_{CC}	COUT7	COUT8	$\overline{\text{ERASE}}$	DIN8	DIN1	DIN2	$\overline{\text{CIENB}}$	CIN7	CIN6	CIN4
C	COUT5	COUT6	ALIGN PIN		$\overline{\text{DIENB}}$	DIN5	DIN4			CIN5	CIN3
D	COUT3	COUT4								CIN2	V_{CC}
E	COUT1	V_{SS}	COUT2						CIN1	CIN0	$\overline{\text{SENBL}}$
F	V_{SS}	COUT0	SHADD						SUM0	V_{CC}	V_{SS}
G	ADR2	DCM0	CLK						SUM1	SUM3	SUM2
H	ADR1	ADR0								SUM5	SUM4
J	V_{CC}	SUM25			SUM20	SUM17	SUM16			SUM7	V_{SS}
K	$\overline{\text{SENBH}}$	SUM24	V_{SS}	V_{CC}	SUM19	V_{SS}	SUM15	SUM12	SUM10	SUM8	SUM6
L	DCM1	SUM23	SUM22	SUM21	SUM18	SUM14	V_{CC}	SUM13	V_{SS}	SUM11	SUM9

HSP43891/883
TOP VIEW
PINS DOWN



Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output Voltage Applied .... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering, Ten Seconds) .... +300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic PGA Package	34.66°C/W	7.78°C/W

Maximum Package Power Dissipation at +125°C
Ceramic PGA Package .... 1.44 Watt
Gate Count .... 17762 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range .... -55°C to +125°C

TABLE 1. HSP43891/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA V_{CC} = 4.5V (Note 1)	1, 2, 3	$-55°C \le T_A \le +125°C$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC} = 4.5V (Note 1)	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-10	+10	µA
Output Leakage Current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-10	+10	µA
Clock Input High	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.8	V
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V, Outputs Open	1, 2, 3	$-55°C \le T_A \le +125°C$	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 20.0MHz V_{CC} = 5.5V (Note 2)	1, 2, 3	$-55°C \le T_A \le +125°C$	-	160.0	mA
Functional Test	FT	(Note 3)	7, 8	$-55°C \le T_A \le +125°C$	-	-	

NOTES: 1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 8mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, $V_{OH} \ge$ 1.5V, $V_{OL} \le$ 1.5V, V_{IHC} = 3.4V, and V_{ILC} = 0.4V.

TABLE 2. HSP43891/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	-20 (20MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
Clock Period	T_{CP}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	39	-	ns
Clock Low	T_{CL}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	16	-	ns
Clock High	T_{CH}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	16	-	ns
Input Setup	T_{IS}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	17	-	ns
Input Hold	T_{IH}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
CLK to Coefficient Output Delay	T_{ODC}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	24	-	20	ns
Output Enable Delay	T_{OED}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	20	-	15	ns
CLK to SUM Output Delay	T_{ODS}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	31	-	25	ns

NOTE: 1. A.C. Testing: VCC = 4.5V and 5.5V. Inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a Logic "1" and "0". CLK is driven at 4.0V and 0V and measured at 2.0V.

TABLE 3. HSP43891/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	-20 (20MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	V_{CC}=Open, f=1MHz All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	15	-	15	pF
Output Capacitance	C_{OUT}		1	$T_A = +25^oC$	-	15	-	15	pF
Output Disable Delay	T_{ODD}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	20	-	15	ns
Output Rise Time	T_{OR}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	7	-	6	ns
Output Fall Time	T_{OF}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	7	-	6	ns

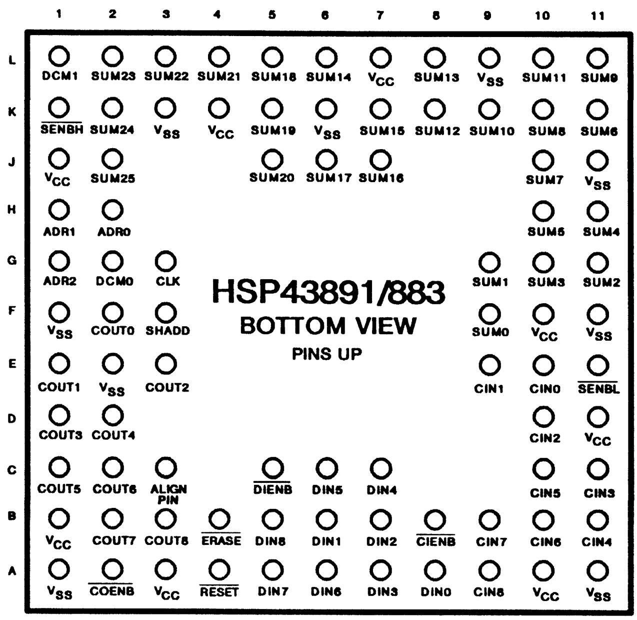
NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. Loading is as specified in the test load circuit, C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Burn-In Circuit



PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	V_{SS}	GND	C1	COUT5	$V_{CC}/2$	F10	V_{CC}	V_{CC}	K4	V_{CC}	V_{CC}
A2	$\overline{\text{COENB}}$	F10	C2	COUT6	$V_{CC}/2$	F11	V_{SS}	GND	K5	SUM19	$V_{CC}/2$
A3	V_{CC}	V_{CC}	C3	ALIGN	NC	G1	ADR2	F2	K6	V_{SS}	GND
A4	$\overline{\text{RESET}}$	F11	C5	$\overline{\text{DIENB}}$	F10	G2	DCM0	F5	K7	SUM15	$V_{CC}/2$
A5	DIN7	F8	C6	DIN5	F5	G3	CLK	F0	K8	SUM12	$V_{CC}/2$
A6	DIN6	F6	C7	DIN4	F4	G9	SUM1	$V_{CC}/2$	K9	SUM10	$V_{CC}/2$
A7	DIN3	F3	C10	CIN5	F5	G10	SUM3	$V_{CC}/2$	K10	SUM8	$V_{CC}/2$
A8	DIN0	F0	C11	CIN3	F3	G11	SUM2	$V_{CC}/2$	K11	SUM6	$V_{CC}/2$
A9	CIN8/TCCI	F8	D1	COUT3	$V_{CC}/2$	H1	ADR1	F1	L1	DCM1	F6
A10	V_{CC}	V_{CC}	D2	COUT4	$V_{CC}/2$	H2	ADR0	F0	L2	SUM23	$V_{CC}/2$
A11	V_{SS}	GND	D10	CIN2	F2	H10	SUM5	$V_{CC}/2$	L3	SUM22	$V_{CC}/2$
B1	V_{CC}	V_{CC}	D11	V_{CC}	V_{CC}	H11	SUM4	$V_{CC}/2$	L4	SUM21	$V_{CC}/2$
B2	COUT7	$V_{CC}/2$	E1	COUT1	$V_{CC}/2$	J1	V_{CC}	V_{CC}	L5	SUM18	$V_{CC}/2$
B3	COUT8/ TCCO	$V_{CC}/2$	E2	V_{SS}	GND	J2	SUM25	$V_{CC}/2$	L6	SUM14	$V_{CC}/2$
B4	$\overline{\text{ERASE}}$	F10	E3	COUT2	$V_{CC}/2$	J5	SUM20	$V_{CC}/2$	L7	V_{CC}	V_{CC}
B5	DIN8/TCS	F7	E9	CIN1	F1	J6	SUM17	$V_{CC}/2$	L8	SUM13	$V_{CC}/2$
B6	DIN1	F1	E10	CIN0	F0	J7	SUM16	$V_{CC}/2$	L9	V_{SS}	GND
B7	DIN2	F2	E11	$\overline{\text{SENBL}}$	F10	J10	SUM7	$V_{CC}/2$	L10	SUM11	$V_{CC}/2$
B8	$\overline{\text{CIENB}}$	F10	F1	V_{SS}	GND	J11	V_{SS}	GND	L11	SUM9	$V_{CC}/2$
B9	CIN7	F7	F2	CUT0	$V_{CC}/2$	K1	$\overline{\text{SENBH}}$	F10			
B10	CIN6	F6	F3	SHADD	F9	K2	SUM24	$V_{CC}/2$			
B11	CIN4	F4	F9	SUM0	$V_{CC}/2$	K3	V_{SS}	GND			

NOTES:
1. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5 ±0.5V.
4. 0.1µF (min) capacitor between V_{CC} and GND per position.
5. F0 = 100KHz ±10%, F1 = F0/2, F2 = F1/2 . . . . ., F11 = F10/2, 40% - 60% Duty Cycle.
6. Input voltage limits: V_{IL} = 0.8V max., V_{IH} = 4.5V ±10%

Metallization Topology

DIE DIMENSIONS:
328 x 283 x 19 ±1 mils

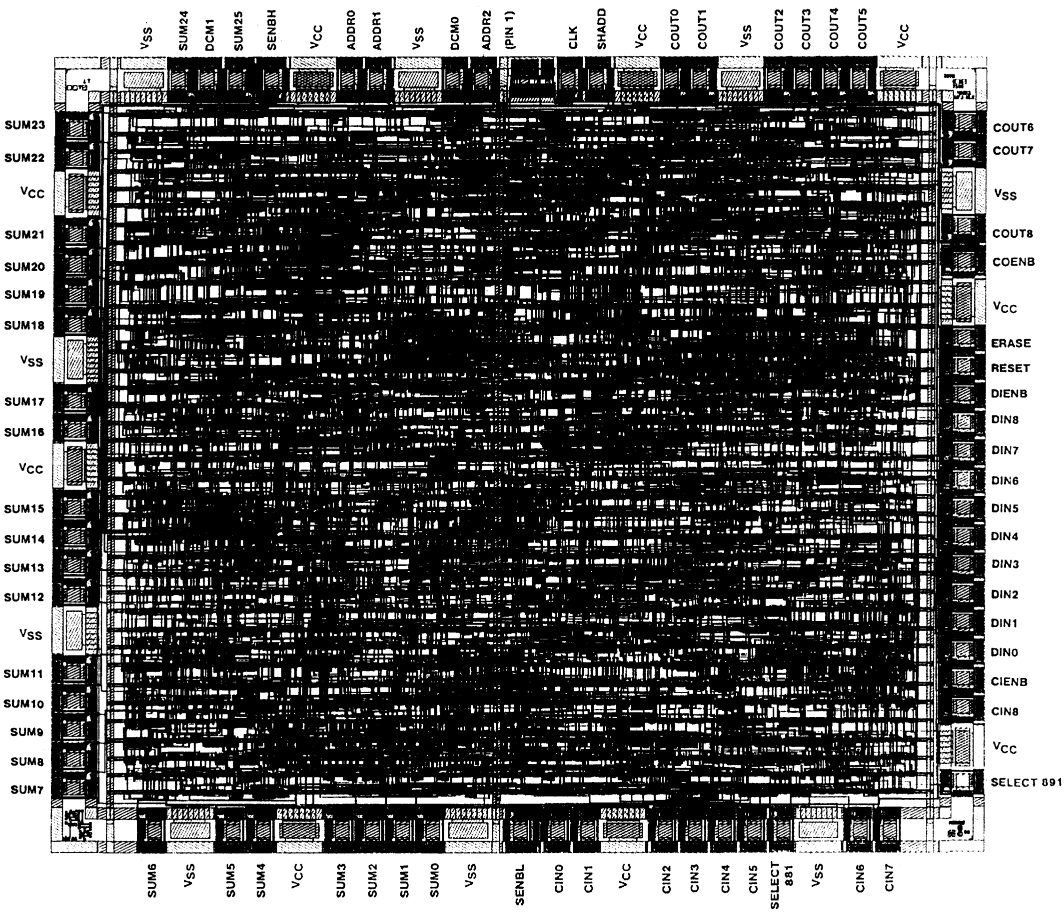
METALLIZATION:
Type: Si - Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:
$1.2 \times 10^5 A/cm^2$

Metallization Mask Layout

HSP43891/883



DSP 4

VIDEO PROCESSING

NOTE: Bold Type Designates a New Product from Harris.

HARRIS SEMICONDUCTOR

HSP48212

January 1994

Digital Video Mixer

Features

- 12-Bit Pixel Data
- Two's Complement or Unsigned Data
- 12-Bit Mix Factor
- 13-Bit Signed or Unsigned Three State Output
- Overflow Detection and Output Saturation
- Rounding to 8, 10, 12, or 13-Bits
- Input and Output Pixel Data Synchronous to Clock
- Programmable Pipeline Delay of up to 7 Clock Cycles for Control of Misaligned Input Data
- TTL Compatible Inputs/Outputs
- DC to 40MHz Clock Rate

Applications

- Video Summing (Frame Addition)
- Video Mixing
- Fade In/Out
- Video Switching
- High Speed Multiplying

Description

The Harris HSP48212 is a 68 pin Digital Video Mixer IC intended for use in multimedia and medical imaging applications.

The HSP48212 allows the user to mix two video sources based on a programmable weighting factor. After weighting the input data signals, the Video Mixer simply adds the two weighted signals mathematically. This results in the mixed output, which is a weighted sum of the two sources.

The input and output interfaces are synchronous with respect to the input clock, simplifying the user interface requirements.

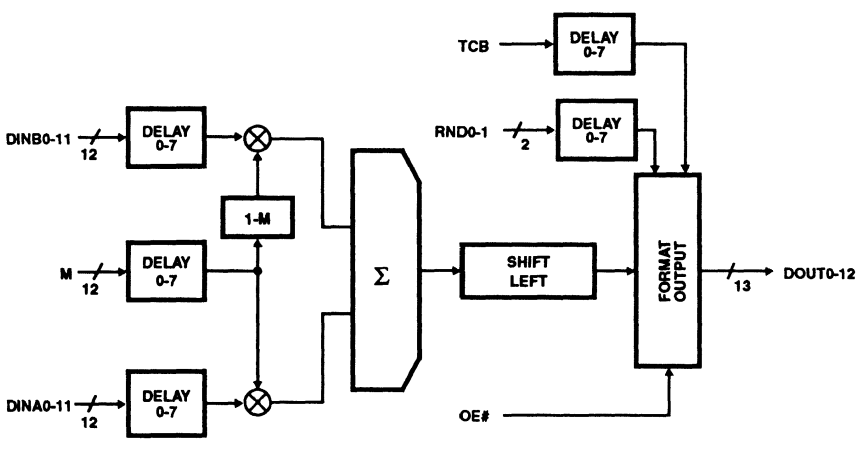
Input Data (DINA, DINB), Mix Factor (M) and control signals (RND, TCB) may be delayed relative to each other in order to compensate for any misalignment that may have occurred prior to entering the HSP48212. Each input's delay may be independently programmed up to seven clock cycles.

The output data may be rounded to 8, 10, 12, or 13-bits. The enabling of data onto the output data bus is under the user's control via an output enable signal (OE#).

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
HSP48212VC-40	0°C to +70°C	64 Lead MQFP
HSP48212JC-40	0°C to +70°C	68 Lead PLCC

Block Diagram



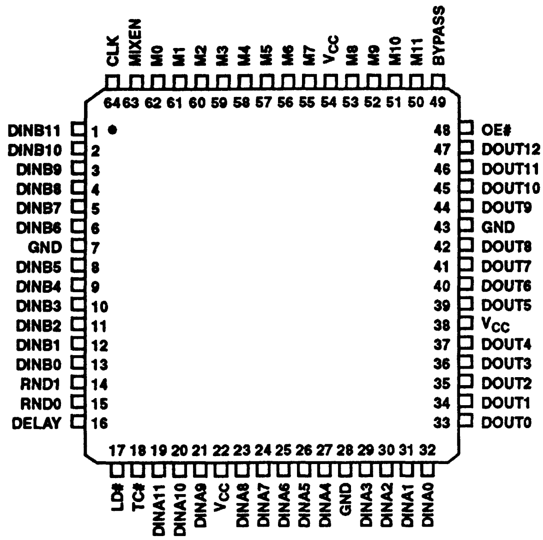
DOUT = 2 x [DINA x M + DINB x (1-M)]

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

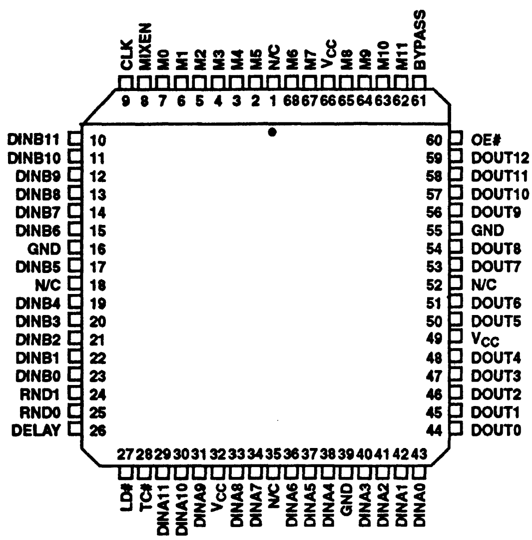
File Number 3627

Pinouts

64 LEAD MQFP
TOP VIEW



68 PIN PLCC
TOP VIEW



Pin Description

NAME	PLCC PIN	TYPE	DESCRIPTION
CLK	9	I	Clock input. All signal pins are synchronous with respect to this clock except LD#, DEL, OE#, and BYPASS.
DINA0-11	29-31 33-34 36-38 40-43	I	Input data bus. Provides data to the Mixer from one video source. Synchronous to the rising edge of CLK.
DINB0-11	10-15, 17 19-23	I	Input data bus. Provides data to the Mixer from one video source. Synchronous to the rising edge of CLK.
M0-11	62-65 67-68 2-7	I	Mix input bus. The range of M is from 0 to 1. The number format is unsigned, with one bit position to the left of the binary point. If a value greater than 1 is placed on this bus, the internal circuitry will saturate M to 1, i.e anytime the MSB is 1, the internal value defaults to 1.00000000000. Synchronous to the rising edge of CLK.
TC#	28	I	Specifies the number format of the input data busses DINA and DINB. 1 = unsigned, 0 = 2's complement. The signal has the same number of latency stages as the incoming data. Therefore, the number format affects the incoming data but not the data in the internal pipeline stages. Synchronous to the rising edge of CLK.
RND0-1	24-25	I	Specifies the number of significant bits on the output bus. 00 = 8-bit, 01 = 10-bit, 10 = 12-bit, 11 = 13-bit. Rounding is performed by adding a binary 1 to the bit position to the right of the desired LSB. The remaining bits are forced to zero. These control signals have the same number of latency stages as the incoming data. Therefore, the output round format does not take effect until the current data has propagated to the output. Synchronous to the rising edge of CLK.
MIXEN	8	I	Mix enable. This pin is used to disable the clock signal which samples the Mix input. When MIXEN = 1, the M0-11 bus is sampled by the rising edge of CLK. When MIXEN = 0, the M0-11 bus is ignored and the previously stored value of M0-11 is used. Synchronous to the rising edge of CLK.
LD#	27	I	Asynchronous load pin. LD# is used to load the delay control registers. The delay control word is loaded serially from LSB to MSB. This signal drives the clock input to a 15-bit serial shift register. Each LD# cycle, the data is transferred through the register bank on the rising edge of LD# In order to load the delay control word, the user must supply exactly 15 LD# pulses.
DEL	26	I	Delay input. This is the serial input data that is sampled by the rising edge of LD#. It is the input to the first stage of the 15-bit serial shift register which contains the delay control word. Synchronous to the rising edge of LD#.
BYPASS	61	I	Allows user to disable (bypass) the LD# interface and use the default delay paths. When BYPASS = 1, the delay control word is forced to all 0's and no extra delays are included in the paths. When BYPASS = 0, the delay control word must be initialized using the LD#/DEL interface in order for the chip to give predictable results. This pin is asynchronous and is not intended to change states during operation.
DOUT0-12	59-56 54-53 51-50 48-44	O	Output data bus. The data on this bus reflects the results of the equation: 2x[AxM + Bx(1-M)]. The number format of the output is either 2's complement or unsigned depending on the value of the TC# signal during data input. The representation of DOUT is also dependent on the value sampled on RND0-1 during data input. (See RND0-1 & TC# pin description)
OE#	60	I	Output enable. Asynchronous input which takes effect immediately following a transition. When OE# = 0 the DOUT bus is driving, when OE# = 1 the DOUT bus is not driven (floating).
V_{CC}	32,49,66	I	5V power supply. There are 3 V_{CC} pads.
GND	16,39,55	I	0V power supply. There are 3 GND pads.

Functional Block Diagram

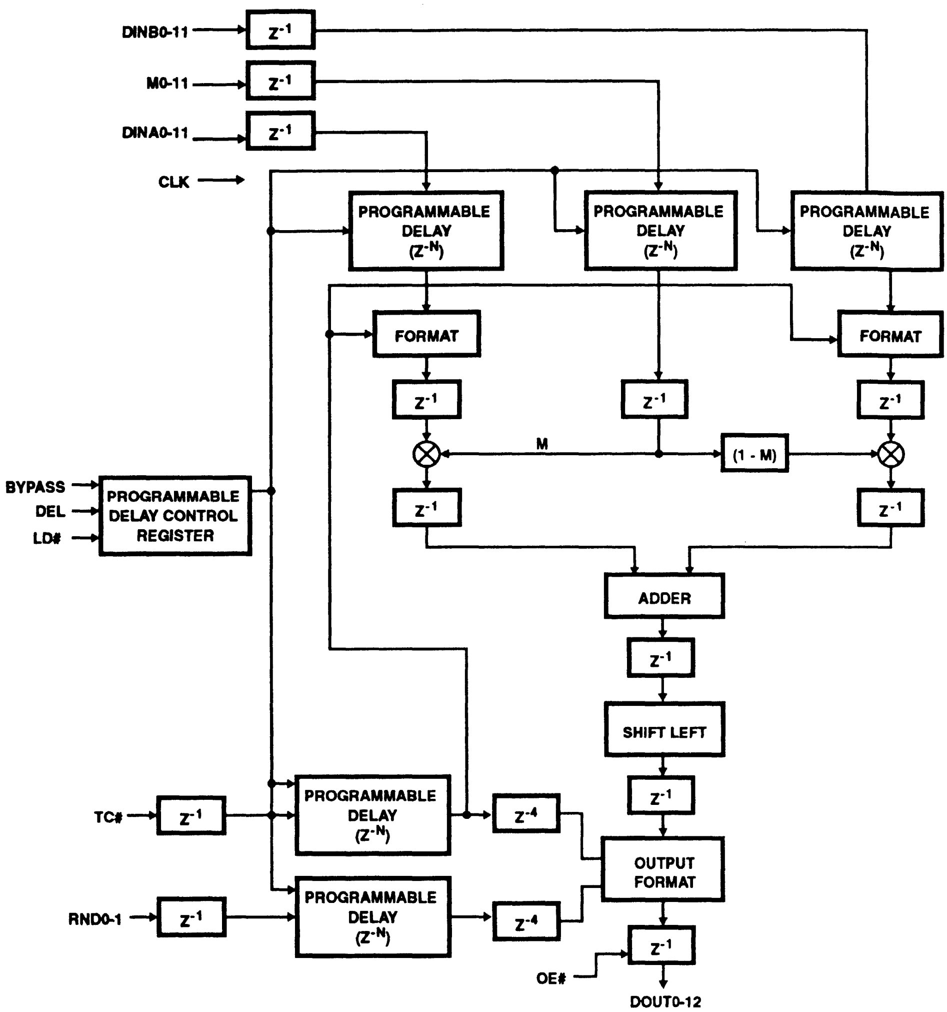


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

Functional Description

The Digital Video Mixer is intended for use in professional video, multimedia and medical imaging applications. The HSP48212 allows the user to mix two video sources based on a programmable weighting factor. After weighting the input data signals, the Video Mixer simply adds the two weighted signals mathematically. This results in the mixed output, which is a weighted sum of the two sources. The fundamental equation implemented by this architecture is:

Eq. (1) $DOUT = 2 \times [DINA \times M + DINB \times (1\text{-}M)]$

where DINA and DINB are the two video sources (pixels) and M is the weighting (Mix) factor. As expressed by this equation, the output DOUT is a weighted average of the incoming pixels. For instance, when M is set to 0 the DINB input source is passed to the output, and when M is set to 1 the DINA input is passed to the output, and when M is set to 0.5 the output is the sum of the two sources DINA and DINB. The user can therefore vary the mix factor to apply different weights to each of the inputs DINA, DINB. This allows functions such as fading in, fading out, fading between images, graphics overlays, and keying. The multiplication factor of 2 as seen in Eq. (1) is accomplished through a 1-bit shift left (See Figure 1). This shifter is not programmable and cannot be accessed by the user.

The functional block diagram is shown in Figure 1. It can be seen that Eq. (1) is directly implemented by this architecture. The architecture has a 6 stage inherent latency. This architecture is extremely flexible in that it allows the user to account for misaligned input data by independently programming up to seven additional delay stages for DINA0-11, DINB0-11, and M0-11, as well as for the format control signals TC# and RND0-1. The programmable delay registers are controlled by the signals DEL, LD#, and BYPASS.

The HSP48212 input interface is primarily synchronous to the rising edge of CLK with the exception of the programmable delay control signals DEL, LD#, and BYPASS. The output data bus DOUT0-12 is registered synchronous to the rising edge of CLK and may also be controlled via the asynchronous output enable signal OE#. The input data, DINA0-11 and DINB0-11, as well as the mix factor M0-11 have 12-bit precision. The output data DOUT0-12 has 13-bit precision to allow for 1-bit of growth.

The signals TC# and RND0-1 control the format of the input and output data. TC# allows DINA0-11 and DINB 0-11 to be either two's complement or unsigned (Note: DINA0-11 and DINB0-11 must have the same format, i.e. no mixed mode). The output data DOUT0-12 can be rounded to 8, 10, 12, or 13-bits as determined by the control signals RND0-1.

Input Data Format

DINA0-11 and DINB0-11 represent two digital video sources (pixels). Each input bus has 12-bits of precision. They may be represented in two's complement form (TC# = 0) or in unsigned form (TC# = 1). It is important to note that DINA0-11 and DINB0-11 must be represented in the same format (i.e. No mixed mode operation is allowed).

M0-11 supplies the weighting (Mix) factor and has 12-bits of precision. M0-11 must be represented in unsigned format and may range from 0 to 1. If a value greater than 1 is placed on the bus, the internal circuitry will saturate M0-11 to 1.00000000000.

DINA0-11, DINB0-11, and M0-11 are synchronously registered on the rising edge of CLK.

The signal MIXEN allows the user to disable the internal clock signal which samples the M0-11 input bus. When MIXEN = 0, the M0-11 bus is ignored and the previously sampled M0-11 value is used. When MIXEN = 1, the M0-11 bus is sampled on the rising edge of CLK.

Programmable Delay

The input data (DINA0-11, DINB0-11), mix factor (M0-11), and control signals (RND0-1, TC#), may be delayed relative to each other in order to compensate for any misalignment that may have occurred prior to entering the HSP48212. Each input's delay may be independently programmed for up to seven delays. In other words, the user can program a different number of pipeline delays for each input. This programmed delay is in addition to the inherent 6 stage delay required by the architecture.

As shown in Figures 2 and 3, the programmable delay information is loaded using the signals LD# and DEL. LD# is the asynchronous load pin used to clock in the delay control word. The delay control word is clocked into a 15-bit serial shift register on the rising edge of LD# (i.e. DEL is synchronous to LD#). The delay control word data is supplied by the DEL signal beginning with the least significant bit and continuing until the most significant bit has been clocked in. On each LD# cycle the DEL data input is transferred through the register bank. The user must supply exactly 15 LD# pulses; if the shift register is clocked more than 15 times, only the most recent 15 data inputs will be stored.

As previously stated, the length of the control word is 15-bits: 3-bits are allocated for each of the 5 inputs, DINA0-11, DINB0-11, M0-11, RND0-1, and TC#. Each 3-bits of the control word allow the user to specify from 0 to 7 additional delay stages by programming the binary equivalent of the desired delay into the appropriate bit position of the delay control word register (e.g. 000 for 0 delays, 001 for 1 delay, ..., 111 for 7 delays).

TABLE 1. DELAY CONTROL WORD

INPUT SIGNAL	CONTROL WORD BIT POSITION
RND0-1	12-14
TC#	9-11
M0-11	6-8y
DINB0-11	3-5
DINA0-11	0-2

The BYPASS control signal enables the programmable delay registers to be bypassed. When BYPASS is high, the delay control word is forced to all 0's and no additional delays are included in any of the input paths. However, when BYPASS is low, the LD#/DEL serial delay control word interface is active and the delay control word must be initialized in order to achieve any meaningful results.

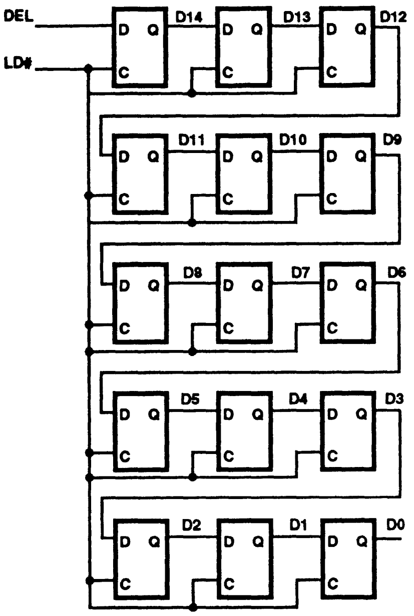


FIGURE 2. DELAY CONTROL WORD SHIFT REGISTER

Format Control Signals

The control signals TC# and RND0-1 are used to specify the input data representation and the output data representation respectively. TC# and RND0-1 are synchronous to CLK, which allows them to be changed on a cycle by cycle basis if needed. The control signals are designed to match the latency of the data paths. When the control inputs change, the new configuration will effect the current input data and will not effect the data in the pipeline stages. For example, if the rounding selection is changed from 8-bit rounding to 10-bit rounding on a given cycle, the output will remain in an 8-bit representation while the new data is propagating through the circuit. When the results of the new data are available at the output, the number format will change to 10-bits.

The RND0-1 control signals determine the number of significant bits on the output bus DOUT0-12. The output data may be rounded to 8, 10, 12, or 13-bits.The rounding operation is performed by adding a binary 1 to the bit position right of the desired LSB and forcing the undesired bits to 0. For example, in 8-bit rounding, a 1 is added to the 9th bit to the right of the MSB (DOUT4), and DOUT0-4 are forced to 0 (i.e. DOUT0-12 = XXXXXXXX00000).

Output Control

DOUT0-12 is the output data bus which represents the weighted average of the incoming pixel data as indicated by Eq. (2):

Eq. (2) DOUT = 2 x [(DINA x M) +(DINB x (1-M))]

The output data will be represented in either two's complement format or in unsigned format depending on the value of the TC# signal when the input data (DINA0-11 and DINB0-11) is sampled by CLK. Similarly, the output representation of DOUT0-12 is also dependent on the value of RND0-1 during sampling of the input data.

The output data DOUT0-12 is registered at the output of the HSP48212 on the rising edge of CLK. The output data may be accessed through the activation of the signal OE#. OE# is an asynchronous input which, when low, causes the DOUT0-12 bus to drive; when OE# is high, the DOUT0-12 bus is not driven (floating).

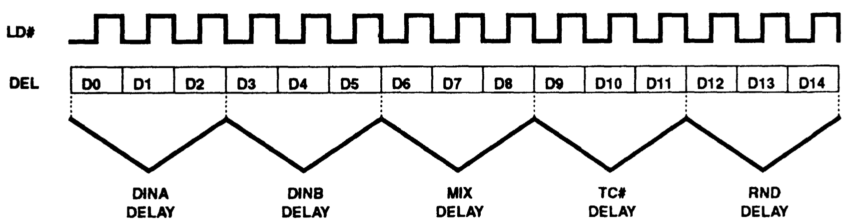


FIGURE 3. DELAY CONTROL WORD TIMING DIAGRAM

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output or I/O Voltage .... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +150°C
Lead Temperature (Soldering 10s) .... +300°C
ESD Classification .... Class 1

Thermal Resistance	θ_{JA}	θ_{JC}
PLCC Package	43°C/W	15°C/W
MQFP Package	51°C/W	30°C/W

Maximum Package Power Dissipation at +70°C
PLCC Package 1.86W
MQFP Package 1.57W
Gate Count .... 6,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range, Commercial .... +5V ± 5%
Operating Temperature Range, Commercial .... 0°C to +70°C

DC Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
I_{CCOP}	Power Supply Current	-	170	mA	V_{CC} = Max, CLK Frequency 40Mhz, Note 2, Note 3
I_{CCSB}	Standby Power Supply Current	-	500	μA	V_{CC} = Max, Outputs Not Loaded
I_I	Input Leakage Current	-10	10	μA	V_{CC} = Max, Input = 0V or V_{CC}
I_O	Output Leakage Current	-10	10	μA	V_{CC} = Max, Input = 0V or V_{CC}
V_{IH}	Logical One Input Voltage	2.0	-	V	V_{CC} = Max
V_{IL}	Logical Zero Input Voltage	-	0.8	V	V_{CC} = Min
V_{OH}	Logical One Output Voltage	2.6	-	V	I_{OH} = -400μA, V_{CC} = Min
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} = 2mA, V_{CC} = Min
V_{IHC}	Clock Input High	3.0	-	V	V_{CC} = Max
V_{ILC}	Clock input Low	-	0.8	V	V_{CC} = Min
C_{IN}	Input Capacitance	-	10	pF	CLK Frequency 1MHz, All Measurements Referenced to GND. T_A = +25°C, Note 1
C_{OUT}	Output Capacitance	-	10	pF	

NOTES:

1. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.
2. Power Supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 4.25mA/MHz.
3. Output load per test load circuit and C_L = 40pF.

AC Electrical Specifications

SYMBOL	PARAMETER	40MHz		UNITS
		MIN	MAX	
T_{CP}	CLK Period	25	-	ns
T_{CH}	CLK High	10	-	ns
T_{CL}	CLK Low	10	-	ns
T_{LP}	LD# Period	25	-	ns

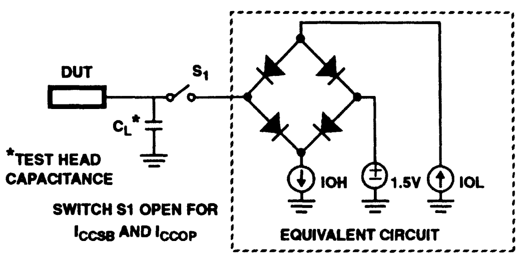
AC Electrical Specifications

SYMBOL	PARAMETER	40MHz		UNITS
		MIN	MAX	
T_{LH}	LD# High	10	-	ns
T_{LL}	LD# Low	10	-	ns
T_{DS}	Data Setup Time to CLK High	10		ns
T_{DH}	Data Hold Time from CLK High	0	-	ns
T_{MS}	MIX Data Setup Time to CLK High	10	-	ns
T_{MH}	MIX Data Hold Time From CLK High	0	-	ns
T_{CS}	Control Data Setup Time to CLK High	10	-	ns
T_{CH}	Control Data Hold Time From CLK High	0	-	ns
T_{DLS}	DEL Setup to LD# High	12	-	ns
T_{DLH}	DEL Hold from LD# High	0	-	ns
T_{OUT}	CLK to Output Data Delay	-	13	ns
T_{OE}	Output Enable Time	-	13	ns
T_{OD}	Output Disable Time	-	13	ns, Note 2
T_{RF}	Output Rise/Fall Time	-	5	ns. Note 2

NOTES:

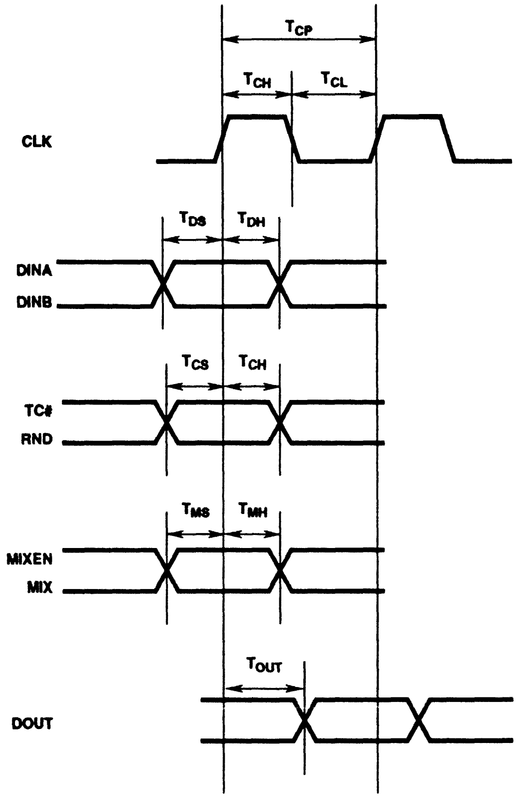
1. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -400μA. Input reference level CLK = 2.0V. Input reference level for all other inputs is 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V, V_{ILC} = 0V.
2. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or Design changes.

AC Test Load Circuit

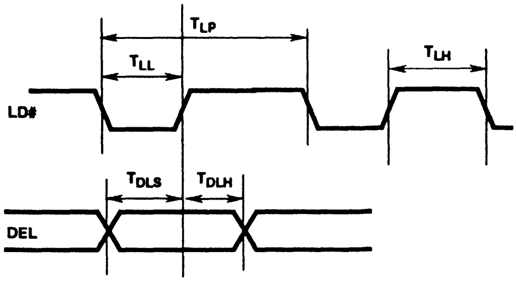


Waveforms

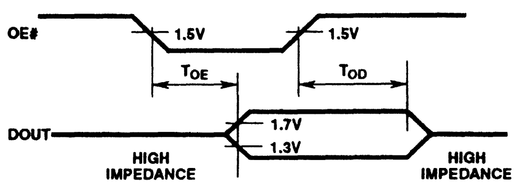
SYNCHRONOUS TIMING



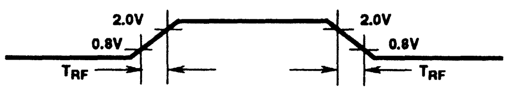
ASYNCHRONOUS TIMING



OUTPUT ENABLE, DISABLE TIMING



OUTPUT RISE AND FALL TIMES



HARRIS SEMICONDUCTOR

HSP48410

January 1994

Histogrammer/Accumulating Buffer

Features

- **10-Bit Pixel Data**
- **4k x 4k Frame Sizes**
- **Asynchronous Flash Clear Pin**
- **Single Cycle Memory Clear**
- **Fully Asynchronous 16 or 24-Bit Host Interface**
- **Generates and Stores Cumulative Distribution Function**
- **Look Up Table Mode**
- **1024 x 24-Bit Delay Memory**
- **24-Bit Three State I/O Bus**
- **DC to 40MHz Clock Rate**

Applications

- **Histogramming**
- **Histogram Equalization**
- **Image and Signal Analysis**
- **Image Enhancement**
- **RGB Video Delay Line**

Description

The Harris HSP48410 is an 84 lead Histogrammer IC intended for use in image and signal analysis. The on-board memory is configured as 1024 x 24 array. This translates to a pixel resolution of 10-bits and an image size of 4k x 4k with no possibility of overflow.

In addition to Histogramming, the HSP48410 can generate and store the Cumulative Distribution Function for use in Histogram Equalization applications. Other capabilities of the HSP48410 include: Bin Accumulation, Look Up Table, 24-bit Delay memory, and Delay and Subtract mode.

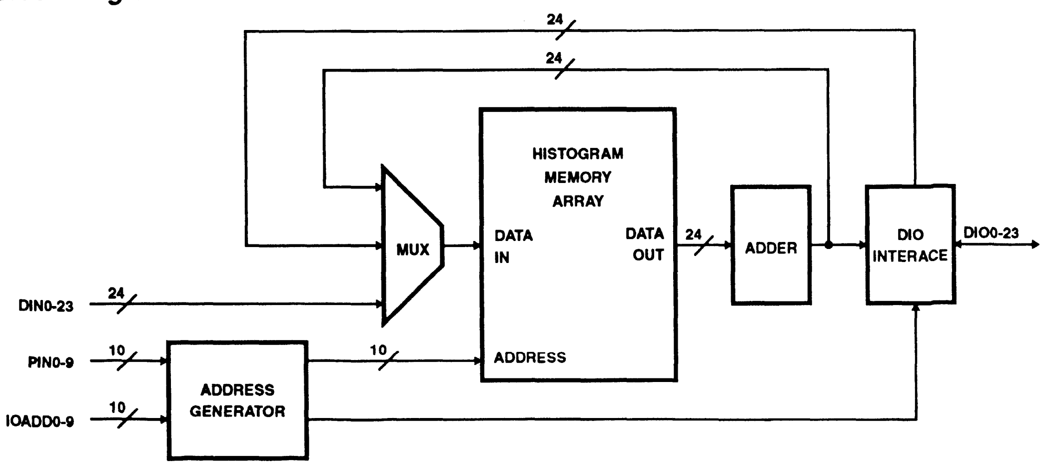
A Flash Clear pin is available in all modes of operation and performs a single cycle reset on all locations of the internal memory array and all internal data paths.

The HSP48410 includes a fully asynchronous interface which provides a means for communications with a host, such as a microprocessor. The interface includes dedicated Read/Write pins and an address port which are asynchronous to the system clock. This allows random access of the Histogram Memory Array for analysis or conditioning of the stored data.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP48410JC-33	0°C to +70°C	84 Lead PLCC
HSP48410JC-40	0°C to +70°C	84 Lead PLCC
HSP48410GC-33	0°C to +70°C	84 Lead PGA
HSP48410GC-40	0°C to +70°C	84 Lead PGA

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3185.1**

Pinouts

84 PIN GRID ARRAY
TOP VIEW

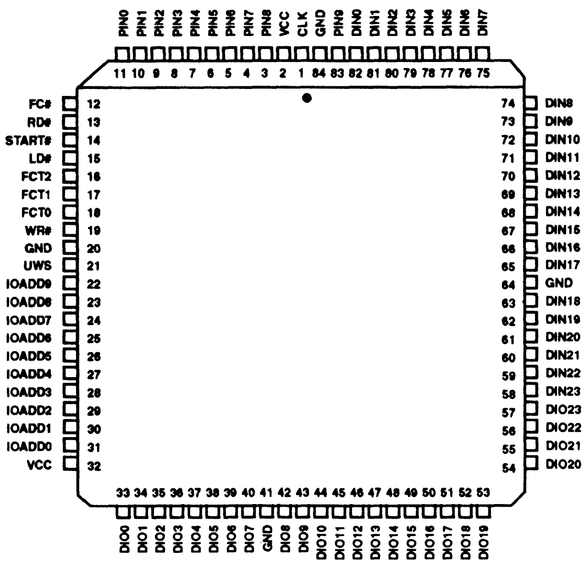
	A	B	C	D	E	F	G	H	J	K	L
11	DIN8	DIN10	DIN11	DIN13	DIN16	DIN17	DIN19	DIN22	DIO23	DIO22	DIO19
10	DIN5	DIN7	DIN9	DIN12	DIN15	DIN21	DIN20	DIN23	DIO21	DIO20	DIO17
9	DIN4	DIN6			DIN14	GND	DIN18			DIO18	DIO16
8	DIN2	DIN3								DIO15	DIO14
7	PIN9	DIN0	GND						DIO10	DIO12	DIO11
6	VCC	DIN1	CLK						DIO9	DIO8	DIO13
5	PIN8	PIN7	PIN6						DIO6	DIO7	GND
4	PIN5	PIN4								DIO4	DIO5
3	PIN3	PIN1			FCT0	IOADD 9	IOADD 8			DIO1	DIO3
2	PIN2	FC#	RD#	FCT2	WR#	UWS	IOADD 6	IOADD 3	IOADD 0	DIO0	DIO2
1	PIN0	START#	LD#	FCT1	GND	IOADD 5	IOADD 7	IOADD 4	IOADD 2	IOADD 1	VCC

PIN 'A1' ID

84 PIN GRID ARRAY
BOTTOM VIEW

	L	K	J	H	G	F	E	D	C	B	A
11	DIO19	DIO22	DIO23	DIN22	DIN19	DIN17	DIN16	DIN13	DIN11	DIN10	DIN8
10	DIO17	DIO20	DIO21	DIN23	DIN20	DIN21	DIN15	DIN12	DIN9	DIN7	DIN5
9	DIO16	DIO18			DIN18	GND	DIN14			DIN6	DIN4
8	DIO14	DIO15								DIN3	DIN2
7	DIO11	DIO12	DIO10						GND	DIN0	PIN9
6	DIO13	DIO8	DIO9						CLK	DIN1	VCC
5	GND	DIO7	DIO6						PIN6	PIN7	PIN8
4	DIO5	DIO4								PIN4	PIN5
3	DIO3	DIO1			IOADD 8	IOADD 9	FCT0			PIN1	PIN3
2	DIO2	DIO0	IOADD 0	IOADD 3	IOADD 6	UWS	WR#	FCT2	RD#	FC#	PIN2
1	VCC	IOADD 1	IOADD 2	IOADD 4	IOADD 7	IOADD 5	GND	FCT1	LD#	START #	PIN0

84 LEAD PLCC
TOP VIEW



4

VIDEO PROCESSING

Pin Description

NAME	PLCC PIN	TYPE	DESCRIPTION
CLK	1	I	Clock input. This input has no effect on the chips functionality when the chip is programmed to an asynchronous mode. All signals denoted as synchronous have their timing specified with reference to this signal.
PIN0-9	3-11, 83	I	Pixel Input. This input bus is sampled by the rising edge of clock. It provides the on-chip RAM with address values in Histogram, Bin Accumulate and LUT(write) mode. During Asynchronous modes it is unused.
LD#	15	I	The Load pin is used to load the FCT0-2-bits into the FCT registers. (See below).
FCT0-2	16-18	I	These three pins are decoded to determine the mode of operation for the chip. The signals are sampled by the rising edge of LD# and take effect after the rising edge of LD#. Since the loading of this function is asynchronous to CLK, it is necessary to disable the START# pin during loading and enable START# at least 1 CLK cycle following the LD# pulse.
START#	14	I	This pin informs the on-chip circuitry which clock cycle will start and/or stop the current mode of operation. Thus, the modes are asynchronously selected (via LD#) but are synchronously started and stopped. This input is sampled by the rising edge of CLK. The actual function of this input depends on the mode that is selected. START# must always be held high (disabled) when changing modes. This will provide a smooth transition from one mode to the next by allowing the part to reconfigure itself before a new mode begins. When START# is high, LUT(read) mode is enabled except for Delay and Delay and Subtract modes.
FC#	12	I	Flash Clear. This input provides a fully asynchronous signal which effectively resets all bits in the RAM Array and the input and output data paths to zero.
DIN0-23	58-63, 65-82	I	Data input bus. Provides data to the Histogrammer during Bin Accumulate, LUT, Delay and Delay and Subtract modes. Synchronous to CLK.
DIO0-23	33-40, 42-57	I/O	Asynchronous data bus. Provides RAM access for a microprocessor in preconditioning the memory array and reading the results of the previous operation. Configuarable as either a 24 or 16-bit bus.
IOADD0-9	22-31	I	RAM address in asynchronous modes. Sampled on the falling edge of WR# or RD#.
UWS	21	I	Upper Word Select. In 16-bit Asynchronous mode, a one on this pin denotes the contents of DIO0-7 as being the upper eight-bits of the data in or out of the Histogrammer. A zero means that DIO0-15 are the lower 16-bits. In all other modes, this pin has no effect.
WR#	19	I	Write enable to the RAM for the data on DIO0-23 when the HSP48410 is configured in one of the asynchronous modes. Asynchronous to CLK.
RD#	13	I	Read control for the data on DIO0-23 in asynchronous modes. Output enable for DIO0-23 in other modes. Asynchronous to CLK.
V_{CC}	2,32		+5V. 0.1μF capacitors between the V_{CC} and GND pins are recommended.
GND	20, 41, 64, 84		Ground

NOTES:

1. A # after a pin name denotes an active low signal.
2. Bit 0 is the LSB on all busses.

Functional Description

The Histogrammer is intended for use in signal and image processing applications. The on-board RAM is 24-bits by 1024 locations. For histogramming, this translates to an image size of 4k x 4k with 10-bit data. A functional block diagram of the part is shown in Figure 1.

In addition to histogramming, the HSP48410 will also perform Histogram Accumulation while feeding the results back into the memory array. The on-board RAM will then contain the Cumulative Distribution Function and can be used for further operation such as histogram equalization.

Other modes are: Bin Accumulate, Look Up Table (LUT), Delay Memory, and Delay and Subtract. The part can also be accessed as a 24-bit by 1024 word asynchronous RAM for preconditioning or reading the results of the histogram.

The Histogrammer can be accessed both synchronously and asynchronously to the system clock (CLK). It was designed to be configured asynchronously by a microprocessor, then switched to a synchronous mode to process data. The result of the processing can then be read out synchronously, or the part can be switched to one of the asynchronous modes so the data may be read out by a microprocessor. All modes are synchronous except for the Asynchronous 16 and 24 modes.

A Flash Clear operation allows the user to reset the entire RAM array and all input and output data paths in a single cycle.

Histogram Memory Array

The Histogram Memory Array is a 24-bit by 1024 deep RAM. Depending on the current mode, its input data comes from either the synchronous input DIN0-23, from the asynchronous data bus DIO0-23, or from the output of the adder. The output data goes to the DIO bus in both synchronous and asynchronous modes.

Address Generator

This section of the circuit determines the source of the RAM address. In the synchronous modes, the address is taken from either the output of the counter or PIN0-9. The pixel input bus is used for Histogram, Bin Accumulate, and LUT(read) modes. All other synchronous modes, i.e. Histogram Accumulate, LUT(write), Delay, and Delay and Subtract use the counter output. The counter is reset on the first rising edge of CLK after a falling edge on START#.

During asynchronous modes, the read and write addresses to the RAM are taken from the IOADD bus on the falling edge of the RD# and WR# signals, respectively.

Adder Input

The Adder Input Control section contains muxes, registers and other logic that provide the proper data to the adder. The configuration of this section is controlled by the output of the Function Decode section.

DIO Interface

The DIO Interface Section transfers data between the Histogrammer and the outside world. In the synchronous modes, DIO acts as a synchronous output for the data currently being processed by the chip; RD# acts as the output enable for the DIO bus; WR# and IOADD0-9 have no effect. When either of the Asynchronous modes are selected (16 or 24- bit), the RAM output is passed directly to the DIO bus on read cycles, and on write cycles, data input on DIO goes to the RAM input port. In this case, data reads and writes are controlled by RD#, WR# and IOADD0-9.

Function Decode

This section provides the signals needed to configure the part for the different modes. The eight modes are decoded from FCT0-2 on the rising edge of LD# (see Table 1). The output of this section is a set of signals which control the path of data through the part.

The mode should only be changed while START# is high. After changing from one mode to another, START# must be clocked high by the rising edge of CLK at least once.

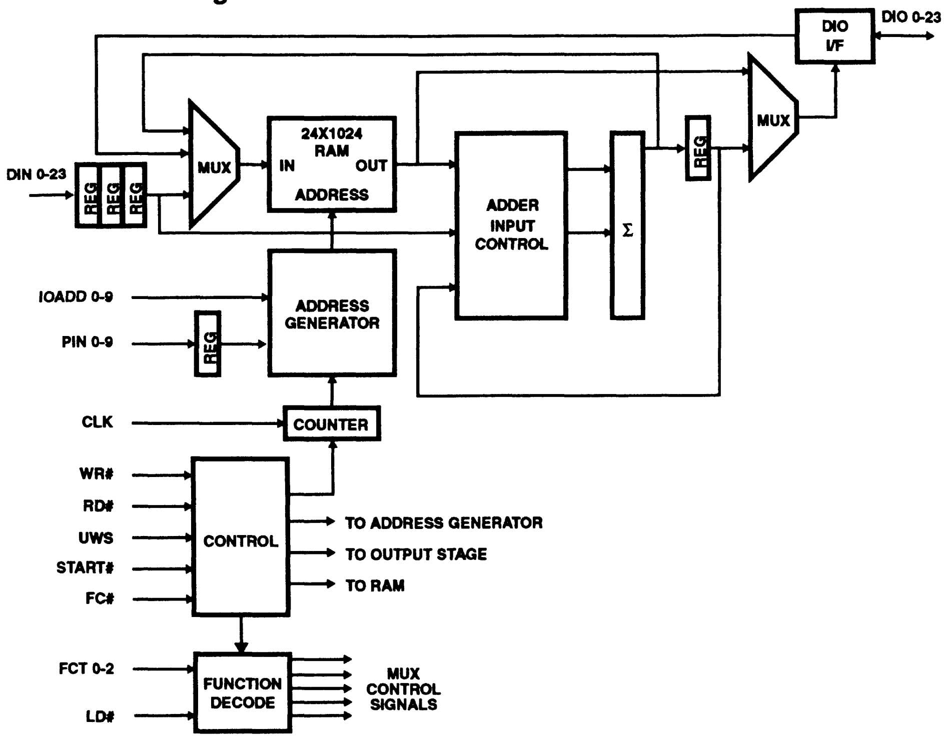
TABLE 1. FUNCTION DECODE

FCT			
2	1	0	MODE
0	0	0	Histogram
0	0	1	Histogram Accumulate
0	1	0	Delay and Subtract
0	1	1	Look Up Table
1	0	0	Bin Accumulate
1	0	1	Delay Memory
1	1	0	Asynchronous 24
1	1	1	Asynchronous 16

Flash Clear

Flash Clear allows the user to clear the entire RAM with a single pin. When the FC# pin is low, all bits of the RAM and the data path from the RAM to DIO0-23 are set to zero. The FC# pin is asynchronous with respect to CLK: the reset begins immediately following a low on this signal. For synchronous modes, in order to ensure consistent results, FC# should only be active while START# is high. For asynchronous modes, WR# must remain inactive while FC# is low.

Functional Block Diagram



ALL REGISTERS ARE CLOCKED BY CLK

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

Histogram Mode

This is the fundamental operation for which this chip was intended. When this mode is selected, the chip configures itself as shown in the block diagram of Figure 2. The pixel data is sampled on the rising edge of clock and used as the read address to the RAM array. The data contained in that address (or bin) is then incremented by 1 and written back into the RAM at the same address.

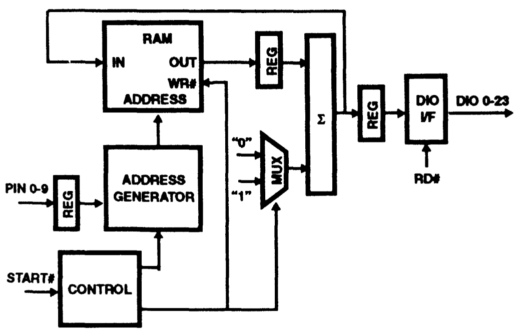


FIGURE 2. HISTOGRAM MODE BLOCK DIAGRAM

At the same time, the new value is also displayed on the DIO bus. This procedure continues until the circuit is interrupted by START# returning high. When START# is high, the RAM write is disabled, the read address is taken from the Pixel Input bus, and the chip acts as if it is in LUT(read) mode. Figure 3 shows histogram mode timing. START# is used to disregard the data on PIN0-9 at DATA2. START# is sampled on the rising edge of clock, but is delayed internally by 3 cycles to match the latency of the Address Generator. Data is clocked onto the DIO bus on the rising edge of CLK. RD# acts as output enable.

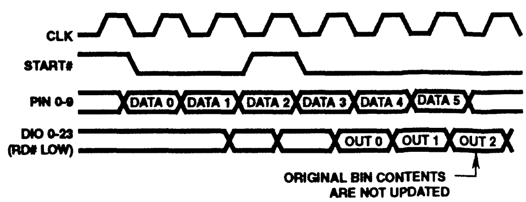


FIGURE 3. HISTOGRAM MODE TIMING

Histogram Accumulate Mode

This function is very similar to the Histogram function. In this case, a counter is used to provide the address data to the RAM. The RAM is sequentially accessed, and the data from each bin is added to the data from the previous bins. This accumulation of data continues until the function is halted. The results of the accumulation are displayed on the DIO bus while simultaneously being written back to the RAM. When the operation is complete, the RAM will contain the Cumulative Distribution Function (CDF) of the image.

Figure 4 shows the configuration for this mode. Once this function is selected, the START# pin is used to reset the counter and enable writing to the RAM. Write enable is delayed 3 cycles to match the delay in the Address Generator. The START# pin determines when the accumulation will begin. Before this pin is activated, the counter will be in an unknown state and the DIO bus will contain unpredictable data. Once the START# pin is sampled low, the data registers are reset in order to clear the accumulation. The output (DIO bus) will then be zero until a non-zero data value is read from the RAM. Timing for this operation is shown in Figure 5.

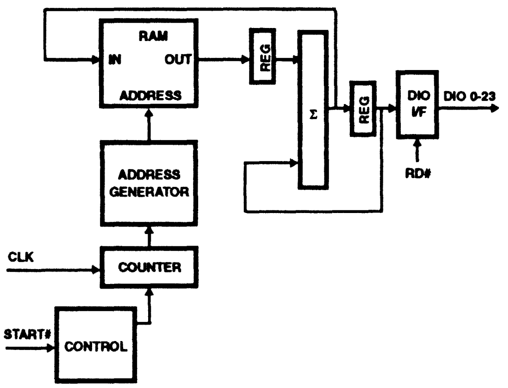


FIGURE 4. HISTOGRAM ACCUMULATE MODE BLOCK DIAGRAM

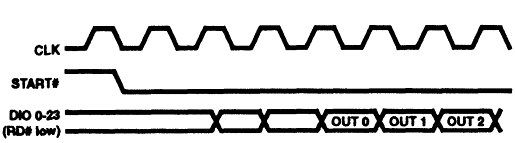


FIGURE 5. HISTOGRAM ACCUMULATE MODE TIMING

The START# pin must remain low in order to allow the accumulated data to overwrite the original histogram data contained in the RAM. When the START# pin returns to a high state, the configuration remains intact, but writing to the RAM is disabled and the part is in LUT(read) mode. Note that the counter is not reset at this point. The counter will be reset on the first cycle of CLK that START# is detected low. To prevent invalid data from being written to the RAM, when the counter reaches its maximum value (1023), further writing to the RAM is disabled and the counter remains at this value until the mode is changed.

At the end of the histogram accumulation, the DIO output bus will contain the last accumulated value. The chip will remain in this state until START# becomes inactive. The results of the accumulation can then be read out synchronously by keeping START# high, or asynchronously in either of the asynchronous modes.

Bin Accumulate Mode

The functionality of this mode is also similar to the Histogram function. The only difference is that instead of incrementing the bin data by 1, the bin data is added to the incoming DIN bus data. The DIN bus is delayed internally by 3 cycles to match the latency in the address generator. Figure 6 shows the block diagram of the internal configuration for this mode, while the timing is given in Figure 7. Note that in this figure, START# is used to disregard the data on DIN0-23 during DATA2.

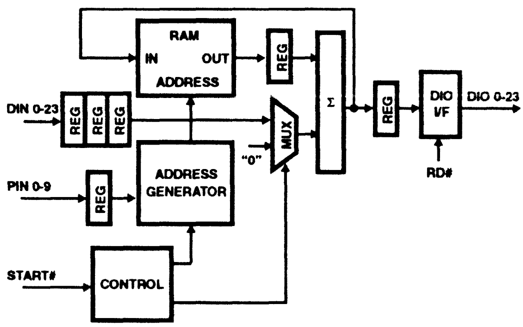


FIGURE 6. BIN ACCUMULATE BLOCK DIAGRAM

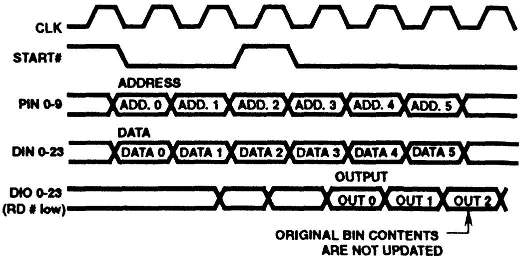


FIGURE 7. BIN ACCUMULATE TIMING

Look Up Table Mode

A Look Up Table (LUT) is used to perform a fixed transformation function on pixel values. This is particularly useful when the transformation is non-linear and cannot be realized directly with hardware. An example is the remapping of the original pixel values to a new set of values based on the CDF obtained through Histogram Accumulation.

The transformation function can be loaded into the LUT in one of three ways: in LUT mode, through DIN0-23; in either asynchronous mode, over the DIO bus as described below under Asynchronous 16/24 Modes; in the Histogram Accumulate mode the transformation function is calculated internally (see description above). The transformation function can then be utilized by deactivating START#, putting the part in LUT mode and clocking the data to be transformed onto the PIN bus. Note that it is necessary to wait one clock cycle after changing the mode before clocking data into the part.

The block diagram and timing for this mode are shown in Figures 8 and 9. The left half of the timing diagram shows LUT(write) mode. On the first CLK that detects START# low, the counter is reset and the write enable is activated for the RAM. As long as START# remains low, the counter provides the write address to the RAM and data is sequentially loaded through the DIN bus. The DIN bus is delayed internally by 3 cycles to match the latency in the Address Generator. The DIO bus will contain the previous contents of the memory location being updated. When 1024 words have been written to the RAM, the counter stops and further writes to the RAM are disabled. The part stays in this state while START# remains low.

When START# returns high, the RAM write is disabled, the read address is taken from the PIN bus, and the chip acts as a synchronous LUT. (This is known as LUT(read) mode.) In order to ensure that the internal pipelines are clear, data should not be input to PIN0-9 until the third clock after START# goes high.

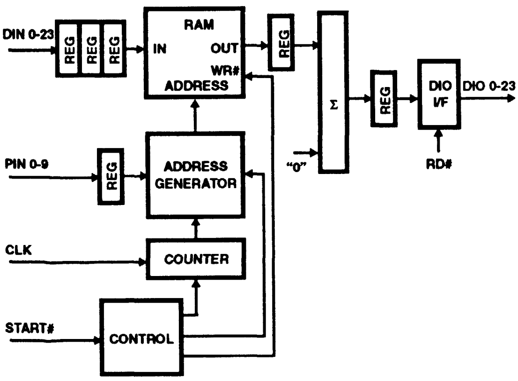
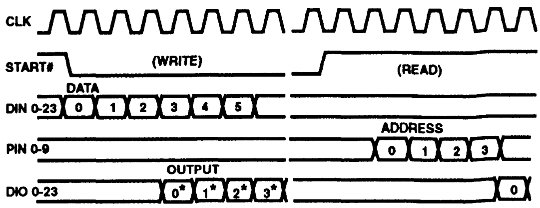


FIGURE 8. LOOK UP TABLE BLOCK DIAGRAM



* PREVIOUS CONTENTS OF BIN LOCATION.

FIGURE 9. LOOK UP TABLE MODE TIMING

Delay Memory (Row Buffer) Mode

As seen by comparing Figures 8 and 10, the configuration for this mode is nearly identical to the LUT mode. In this mode, however, the counter is always providing the address and the write function is always enabled.

In order to force this configuration to act as a row delay register, the START# signal must be used to reset the internal counter each time a new row of pixels is being sampled. Because of the inherent latency in the address and data paths, the counter must be reset every N-4 cycles, where N is the desired delay length. For example, if a delay from DIN to DIO of ten cycles is desired, the START# signal must be set low every six cycles (see Figure 11). If the internal address counter reaches its maximum count (1023), it holds that value and further writes to the RAM are disabled.

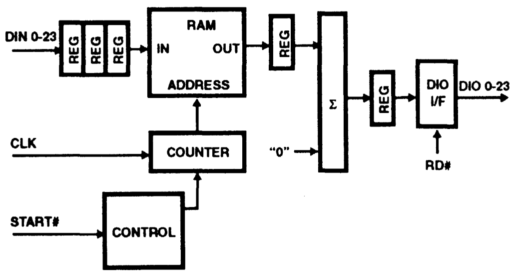


FIGURE 10. DELAY MEMORY BLOCK DIAGRAM

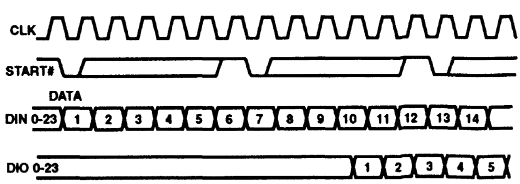


FIGURE 11. DELAY MEMORY MODE TIMING FOR ROW LENGTH OF TEN

Delay and Subtract Mode

This mode is similar to the Delay Memory mode, except the input data is subtracted from the corresponding data stored in RAM (See Figures 12 and 13).

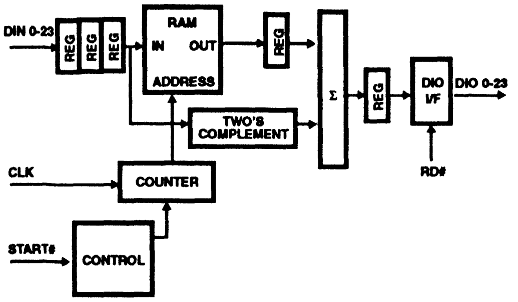


FIGURE 12. DELAY AND SUBTRACT BLOCK DIAGRAM

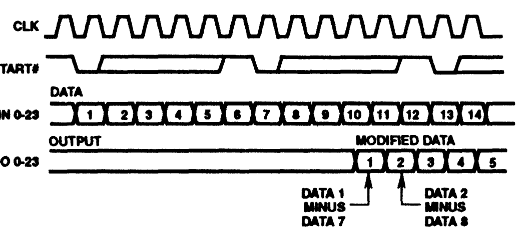


FIGURE 13. DELAY AND SUBTRACT MODE TIMING FOR ROW LENGTH OF TEN

Asynchronous 16/24 Modes

In the Asynchronous modes, the chip acts like a single port RAM. In this mode, the user can read (access) any bin location on the fly by simply setting the 10-bit IO address to the desired bin location. The RAM is then read or written on the following RD# or WR# pulse. A block diagram for this mode is shown in Figure 14. Note that all registers and pipeline stages are bypassed; START# and CLK have no effect in this mode.

Timing waveforms for this mode are also shown in Figure 15. During reading, the read address is latched (internally) on the falling edge of RD#. During write operations, the address is latched on the falling edge of WR# and data is latched on the rising edge of WR#. Note that reading and writing occur on different ports, so that, in this mode, the write port always latches its address and data values from the WR# signal, while the read port always uses RD# for latching.

The difference between the Async 16 mode and the Async 24 mode is the number of data bits available to the user. In 16-bit mode, the user can connect the system data bus to the lower 16-bits of the Histogrammer's DIO bus. The UWS pin becomes the LSB of the IO address, which determines if the lower 16-bits or upper 8-bits of the 24-bit Histogrammer data is being used. When UWS is low, the data present at DIO0-15 is the lower 16-bits of the data in the IOADD0-9 location. When UWS is high, the upper 8-bits of the IOADD09 location are present on DIO0-7. (This is true for both reading and writing.) Thus it takes 2 cycles for an asynchronous 24-bit operation when in Async 16 mode. Unused outputs are zeros.

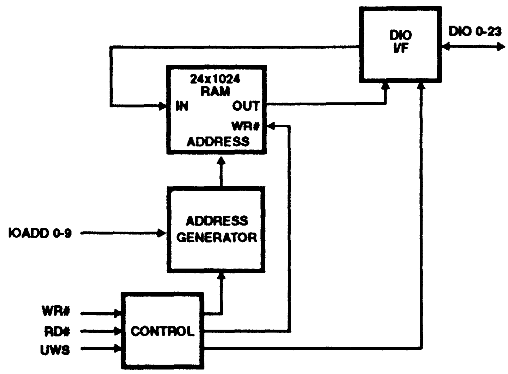


FIGURE 14. ASYNCHRONOUS 16/24 BLOCK DIAGRAM

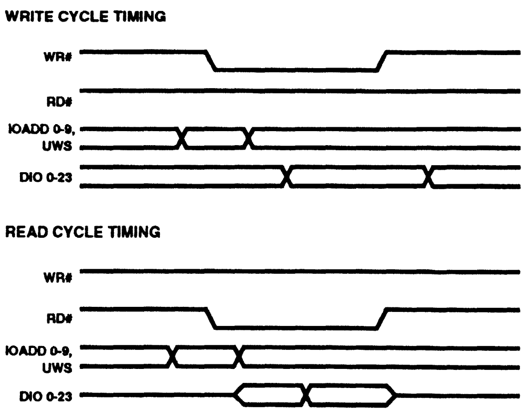


FIGURE 15. ASYNCHRONOUS 16/24 MODE TIMING

4 VIDEO PROCESSING

Absolute Maximum Ratings

Supply Voltage . . . . +8.0V
Input, Output Voltage . . . . GND-0.5V to V_{CC}+0.5V
Storage Temperature Range . . . . -65°C to +150°C
Junction Temperature. . . . . +175°C (PGA), +150°C (PLCC)
Lead Temperature (Soldering 10s). . . . . +300°C
ESD Classification . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
PGA Package	34.3°C/W	8.0°C/W
PLCC Package	23.0°C/W	7.4°C/W

Maximum Package Power Dissipation at +70°C
PGA Package 3.1W
PLCC Package 3.5W
Gate Count . . . . 3500 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . +5V ±5%
Operating Temperature Range . . . . 0°C to +70°C

DC Electrical Specifications

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.0	-	V	V_{CC} = 5.25V
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = 4.75V
High Level Clock Input	V_{IHC}	3.0	-	V	V_{CC} = 5.25V
Low Level Clock Input	V_{ILC}	-	0.8	V	V_{CC} = 4.75V
Output High Voltage	V_{OH}	2.6	-	V	I_{OH} = -400µA, V_{CC} = 4.75V
Output Low Voltage	V_{OL}	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.75V
Input Leakage Current	I_L	-10	10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V
I/O Leakage Current	I_O	-10	10	µA	V_{OUT} = V_{CC} or GND, V_{CC} = 5.25V
Standby Supply Current	I_{CCSB}	-	500	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Outputs Open
Operating Power Supply Current	I_{CCOP}	-	396	mA	f = 33 MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.25V (Note 1, 2)

NOTES:

1. Power supply current is proportional to operating frequency. typical rating for I_{CCOP} is 12mA/MHz.
2. Maximum junction temperature must be considered when operating part at high clock frequencies.

Capacitance T_A = +25°C, Not tested, but characterized at initial design and at major process or design changes.

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_{IN}	-	12	pF	FREQ = 1 MHz, V_{CC} = Open, all measurements are referenced to device ground.
Output Capacitance	C_{OUT}	-	12	pF	

AC Electrical Specifications V_{CC} = 5V ± 5%, T_A = 0°C to +70°C (Note 1)

PARAMETER	SYMBOL	-40 (40 MHz)		-33 (33 MHz)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Clock Period	T_{CP}	25	-	30	-	ns	
Clock Low	T_{CH}	10	-	12	-	ns	
Clock High	T_{CL}	10	-	12	-	ns	
DIN Setup	T_{DS}	12	-	13	-	ns	

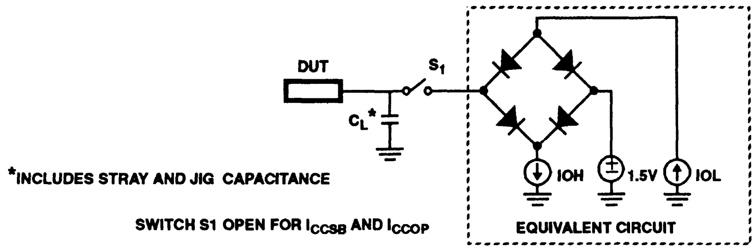
AC Electrical Specifications V_{CC} = 5V ± 5%, T_A = 0°C to +70°C (Note 1) **(Continued)**

PARAMETER	SYMBOL	-40 (40 MHz) MIN	-40 (40 MHz) MAX	-33 (33 MHz) MIN	-33 (33 MHz) MAX	UNITS	TEST CONDITIONS
DIN0-23 Hold	T_{DH}	0	-	0	-	ns	
Clock to DIO0-23 Valid	T_{DO}	-	15	-	19	ns	
FC# Pulse Width	T_{FL}	35	-	35	-	ns	
FCT0-2 Setup to LD#	T_{FS}	10	-	10	-	ns	
FCT0-2 Hold from LD#	T_{FH}	0	-	0	-	ns	
START# Setup to CLK	T_{SS}	12	-	13	-	ns	
START# Hold from CLK	T_{SH}	0	-	0	-	ns	
PIN0-9 Setup Time	T_{PS}	12	-	13	-	ns	
PIN0-9 Hold Time	T_{PH}	0	-	0	-	ns	
LD# Pulse Width	T_{LL}	10	-	12	-	ns	
LD# Setup to START#	T_{LS}	T_{CP}		T_{CP}	-	ns	Note 2
WR# Low	T_{WL}	12	-	15	-	ns	
WR# High	T_{WH}	12	-	15	-	ns	
Address Setup	T_{AS}	13	-	15	-	ns	
Address Hold	T_{AH}	1	-	1	-	ns	
DIO Setup to WR#	T_{WS}	12	-	15	-	ns	
DIO Hold from WR#	T_{WH}	1	-	1	-	ns	
RD# Low	T_{RL}	35	-	43	-	ns	
RD# High	T_{RH}	15	-	17	-	ns	
RD# Low to DIO Valid	T_{RD}	-	35	-	43	ns	
Read/Write Cycle Time	T_{CY}	55	-	65	-	ns	
DIO Valid after RD# High	T_{OH}	-	0	-	0	ns	Note 3
Output Enable Time	T_{OE}	-	18	-	19	ns	Note 4
Output Disable Time	T_{OD}	-	18	-	19	ns	Note 3
Output Rise Time	T_R	-	6	-	6	ns	From 0.8V to 2.0V, Note 3
Output Fall Time	T_F	-	6	-	6	ns	From 2.0V to 0.8V, Note 3

NOTES:

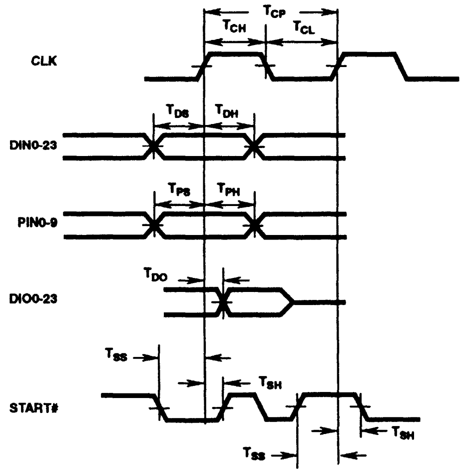
1. AC Testing is performed as follows: Input levels (CLK) 0.0V and 4.0V; Input levels (All other inputs) 0V and 3.0V. Timing reference levels (CLK) = 2.0V, (All others) = 1.5V. Output load circuit with C_L = 40pF. Output transition measured at $V_{OH} \geq$ 1.5V and $V_{OL} \leq$ 1.5V.
2. There must be at least one rising edge of CLK between the rising edge of LD# and the falling edge of START#.
3. Characterized upon initial design and after major changes to design and/or process.
4. Transition is measured at ±200mV from steady state voltage with loading as specified in test load circuit with C_L = 40pF.

Test Load Circuit

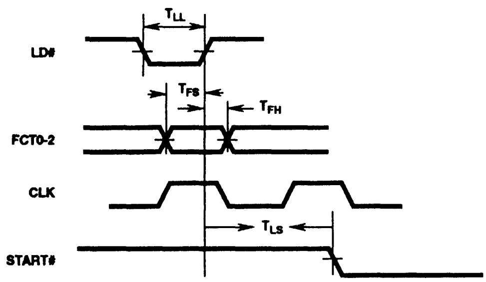


Waveforms

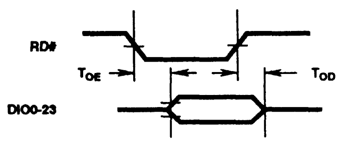
SYNCHRONOUS DATA AND CONTROL TIMING



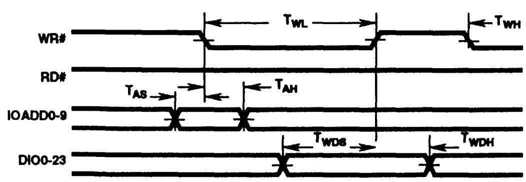
FUNCTION LOAD TIMING



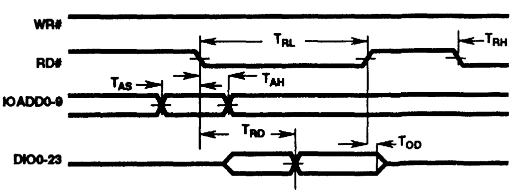
SYNCHRONOUS OUTPUT TIMING



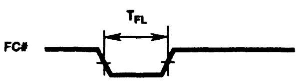
WRITE CYCLE TIMING



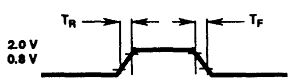
READ CYCLE TIMING



FLASH CLEAR TIMING



OUTPUT RISE AND FALL TIMES



HARRIS SEMICONDUCTOR

HSP48410/883

January 1994

Histogrammer/Accumulating Buffer

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **10-Bit Pixel Data**
- **4k x 4k Frame Sizes**
- **Asynchronous Flash Clear Pin**
- **Fully Asynchronous 16-Bit or 24-Bit Host Interface**
- **DC to 33MHz Clock Rate**

Applications

- **Histogramming**
- **Histogram Equalization**
- **Image and Signal Analysis**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP48410GM-33/883	-55°C to +125°C	84 Lead PGA
HSP48410GM-25/883	-55°C to +125°C	84 Lead PGA

Description

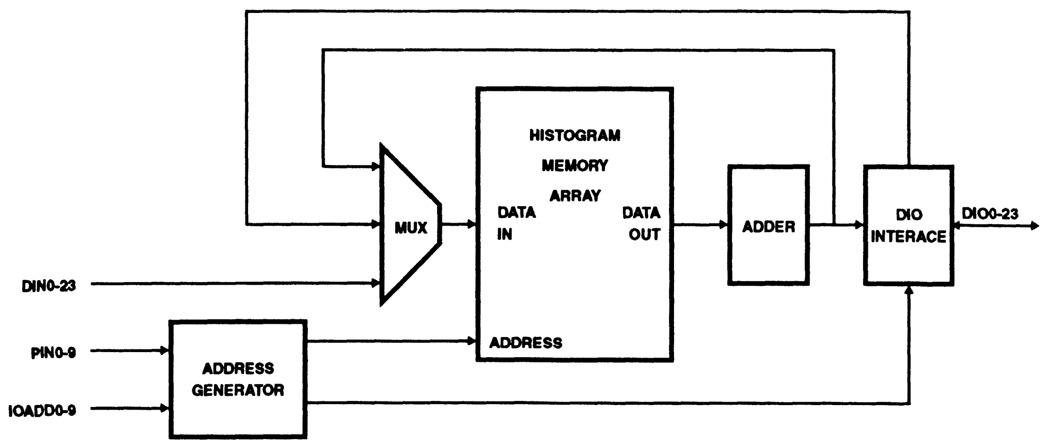
The Harris HSP48410 is an 84 lead Histogrammer IC intended for use in image and signal analysis. The on board memory is configured as 1024 x 24 array. This translates to a pixel resolution of 10-bits and an image size of 4k x 4k with no possibility of overflow.

In addition to Histogramming, the HSP48410 can generate and store the Cumulative Distribution Function for use in Histogram Equalization applications. Other capabilities of the HSP48410 include: Bin Accumulation, Look Up Table, 24-bit Delay memory, and Delay and Subtract mode.

A Flash Clear pin is available in all modes of operation and performs a single cycle reset on all locations of the internal memory array and all internal data paths.

The HSP48410 includes a fully asynchronous interface which provides a means for communications with a host, such as a microprocessor. The interface includes dedicated Read/Write pins and an address port which are asynchronous to the system clock. This allows random access of the Histogram Memory Array for analysis or conditioning of the stored data.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3542.1**

Pinouts

84 LEAD PIN GRID ARRAY
TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L
11	DIN8	DIN10	DIN11	DIN13	DIN16	DIN17	DIN19	DIN22	DIO23	DIO22	DIO19
10	DIN5	DIN7	DIN9	DIN12	DIN15	DIN21	DIN20	DIN23	DIO21	DIO20	DIO17
9	DIN4	DIN6			DIN14	GND	DIN18			DIO18	DIO16
8	DIN2	DIN3								DIO15	DIO14
7	PIN9	DIN0	GND						DIO10	DIO12	DIO11
6	VCC	DIN1	CLK						DIO9	DIO8	DIO13
5	PIN8	PIN7	PIN6						DIO6	DIO7	GND
4	PIN5	PIN4								DIO4	DIO5
3	PIN3	PIN1			FCT0	IOADD 9	IOADD 8			DIO1	DIO3
2	PIN2	FC#	RD#	FCT2	WR#	UWS	IOADD 6	IOADD 3	IOADD 0	DIO0	DIO2
1	PIN0	START #	LD#	FCT1	GND	IOADD 5	IOADD 7	IOADD 4	IOADD 2	IOADD 1	VCC

PIN 'A1' ID

84 LEAD PIN GRID ARRAY
BOTTOM VIEW

L	K	J	H	G	F	E	D	C	B	A	
DIO19	DIO22	DIO23	DIN22	DIN19	DIN17	DIN16	DIN13	DIN11	DIN10	DIN8	11
DIO17	DIO20	DIO21	DIN23	DIN20	DIN21	DIN15	DIN12	DIN9	DIN7	DIN5	10
DIO16	DIO18			DIN18	GND	DIN14			DIN6	DIN4	9
DIO14	DIO15								DIN3	DIN2	8
DIO11	DIO12	DIO10						GND	DIN0	PIN9	7
DIO13	DIO8	DIO9						CLK	DIN1	VCC	6
GND	DIO7	DIO6						PIN6	PIN7	PIN8	5
DIO5	DIO4								PIN4	PIN5	4
DIO3	DIO1			IOADD 8	IOADD 9	FCT0			PIN1	PIN3	3
DIO2	DIO0	IOADD 0	IOADD 3	IOADD 6	UWS	WR#	FCT2	RD#	FC#	PIN2	2
VCC	IOADD 1	IOADD 2	IOADD 4	IOADD 7	IOADD 5	GND	FCT1	LD#	START #	PIN0	1

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
CLK	C6	I	Clock input. This input has no effect on the chips functionality when the chip is programmed to an asynchronous mode. All signals denoted as synchronous have their timing specified with reference to this signal.
PIN0-9	A1-5, A7, B3-5, C5	I	Pixel Input. This input bus is sampled by the rising edge of clock. It provides the on chip RAM with address values in Histogram, Bin Accumulate and LUT(write) mode. During Asynchronous modes it is unused.
LD#	C1	I	The Load pin is used to load the FCT0-2 bits into the FCT registers. (See below).
FCT0-2	D1-2, E3	I	These three pins are decoded to determine the mode of operation for the chip. The signals are sampled by the rising edge of LD# and take effect after the rising edge of LD#. Since the loading of this function is asynchronous to CLK, it is necessary to disable the START# pin during loading and enable START# at least 1 CLK cycle following the LD# pulse.
START#	B1	I	This pin informs the on chip circuitry which clock cycle will start and/or stop the current mode of operation. Thus, the modes are asynchronously selected (via LD#) but are synchronously started and stopped. This input is sampled by the rising edge of CLK. The actual function of this input depends on the mode that is selected. START# must always be held high (disabled) when changing modes. This will provide a smooth transition from one mode to the next by allowing the part to reconfigure itself before new mode begins. When START# is high, LUT(read) mode is enabled except for Delay and Delay and Subtract modes.
FC#	B2	I	Flash Clear. This input provides a fully asynchronous signal which effectively resets all bits in the RAM Array and the input and output data paths to zero.
DIN0-23	A8-11, B6-11, C10-11, D10-11, E9-11, F10-11, G9-11, H10-11	I	Data input bus. Provides data to the Histogrammer during Bin Accumulate, LUT, Delay and Delay and Subtract modes. Synchronous to CLK.
DIO0-23	J5-7, J10-11, K2-11, L2-4, L6-11	I/O	Asynchronous data bus. Provides RAM access for a microprocessor in preconditioning the memory array and reading the results of the previous operation. Configuarable as either a 24-bit or 16-bit bus
IOADD0-9	F1,F3,G1-3, H1-2, J1-2,K1	I	RAM address in asynchronous modes. Sampled on the falling edge of WR# or RD#.
UWS	F2	I	Upper Word Select. In 16-bit Asynchronous mode, a one on this pin denotes the contents of DIO0-7 as being the upper eight-bits of the data in or out of the Histogrammer. A zero means that DIO0-15 are the lower 16-bits. In all other modes, this pin has no effect.
WR#	E2	I	Write enable to the RAM for the data on DIO0-23 when the HSP48410 is configured in one of the asynchronous modes. Asynchronous to CLK.
RD#	C2	I	Read control for the data on DIO0-23 in asynchronous modes. Output enable for DIO0-23 in other modes. Asynchronous to CLK.
VCC	A6, L1		+5V
GND	C7, E1, F9, L5		Ground

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output Voltage .... GND -0.5V to V_{CC} +0.5V
Storage Temperature .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering 10s) .... +300°C
ESD .... Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic PGA Package	34.3°C/W	8.0°C/W

Maximum Package Power Dissipation at +125°C
Ceramic PGA Package .... 1.46 Watt
Gate Count .... 3500 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range .... -55°C to +125°C

TABLE 1. DC ELECTRICAL SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
High Level Clock Input	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	3.0	-	V
Low Level Clock Input	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
Output High Voltage	V_{OH}	I_{OH} = -400μA, V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.6	-	V
Output Low Voltage	V_{OL}	I_{OL} = +2.0mA, V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
Input Leakage Current	I_L	V_{IN} = VCC or GND, V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	10	μA
I/O Leakage Current	I_O	V_{OUT} = V_{CC} or GND, V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	10	μA
Standby Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	500	μA
Operating Power Supply Current	I_{CCOP}	f = 25.6MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.5V (Note 2)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	308	mA
Functional Test	FT	(Notes 3,4)	7, 8	-55°C ≤ T_A ≤ +125°C	-	-	-

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Power Supply current is proportional to operating frequency. Typical rating for I_{CCOP} is12mA/MHz. Maximum junction temperature must be considered when operating part at high clock frequencies.
3. Tested as follows: f = 1MHz, V_{IH} = 2.6V, V_{IL} = 0.4V, V_{OH} ≥ 1.5V, V_{OL} ≤ 1.5V, V_{IHC} = 3.4V and V_{ILC} = 0.4V.
4. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C (Note 1)

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	-33 (33MHz) MIN	-33 (33MHz) MAX	-25 (25.6MHz) MIN	-25 (25.6MHz) MAX	UNITS
Clock Period	T_{CP}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	30	-	39	-	ns
Clock Low	T_{CH}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	12	-	15	-	ns
Clock High	T_{CL}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	12	-	15	-	ns
DIN Setup	T_{DS}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	15	-	16	-	ns
DIN 0-23 Hold	T_{DH}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	1	-	1	-	ns
Clock to DIO 0-23 Valid	T_{DO}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	19	-	24	ns
FC# Pulse Width	T_{FL}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	35	-	35	-	ns
FCT 0-2 Setup to LD#	T_{FS}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	12	-	15	-	ns
FCT 0-2 Hold from LD#	T_{FH}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	1	-	1	-	ns
START# Setup to CLK	T_{SS}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	15	-	16	-	ns
START# Hold from CLK	T_{SH}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	0	-	0	-	ns
PIN 0-9 Setup Time	T_{PS}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	15	-	16	-	ns
PIN 0-9 Hold Time	T_{PH}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	1	-	1	-	ns
LD# Pulse Width	T_{LL}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	12	-	15	-	ns
LD# Setup to START#	T_{LS}	Note 2	9, 10, 11	-55°C ≤ T_A ≤ +125°C	T_{CP}		T_{CP}	-	ns
WR# Low	T_{WL}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	15	-	20	-	ns
WR# High	T_{WH}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	15	-	20	-	ns
Address Setup	T_{AS}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	16	-	20	-	ns
Address Hold	T_{AH}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	2	-	2	-	ns
DIO Setup to WR#	T_{WS}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	16	-	20	-	ns
DIO Hold from WR#	T_{WH}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	2	-	2	-	ns
RD# Low	T_{RL}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	43	-	55	-	ns
RD# High	T_{RH}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	17	-	20	-	ns
RD# Low to DIO Valid	T_{RD}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	43	-	55	ns
Output Enable Time	T_{OE}	Note 3	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	19	-	24	ns
Read/Write Cycle Time	T_{CY}		9, 10, 11	-55°C ≤ T_A ≤ +125°C	65		80	-	ns

NOTES:

1. A.C. Testing is performed as follows: Input levels (CLK) 0.0V and 4.0V; Input levels (All other inputs) 0V and 3.0V. Timing reference levels (CLK) = 2.0V, (All others) = 1.5V. Output load circuit with C_L = 40pF. Output transition measured at V_{OH} ≥ 1.5V and V_{OL} ≥ 1.5V.
2. There must be at least one rising edge of CLK between the rising edge of LD# and the falling edge of START#.
3. Transition is measured at ±200 mV from steady state voltage with loading as specified in test load circuit with C_L = 40pF.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	-33 (33MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	12	-	12	pF
Output Capacitance	C_O	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	12	-	12	pF
DIO Valid After RD# High	T_{OH}		1, 2	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
Output Disable Time	T_{OD}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	27	-	27	ns
Output Rise Time	T_R	From 0.8V to 2.0V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	9	-	9	ns
Output Fall Time	T_F	From 2.0V to 0.8V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	9	-	9	ns

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2,3,8A,8B,10,11
Group A	-	1,2,3,7,8A,8B,9,10,11
Groups C and D	Samples/5005	1,7,9

Burn-In Circuits

84 LEAD GRID ARRAY
TOP VIEW

11	DIN8	DIN10	DIN11	DIN13	DIN16	DIN17	DIN19	DIN22	DIO23	DIO22	DIO19
10	DIN5	DIN7	DIN9	DIN12	DIN15	DIN21	DIN20	DIN23	DIO21	DIO20	DIO17
9	DIN4	DIN6			DIN14	GND	DIN18			DIO18	DIO16
8	DIN2	DIN3								DIO15	DIO14
7	PIN9	DIN0	GND						DIO10	DIO12	DIO11
6	VCC	DIN1	CLK						DIO9	DIO8	DIO13
5	PIN8	PIN7	PIN6						DIO6	DIO7	GND
4	PIN5	PIN4								DIO4	DIO5
3	PIN3	PIN1			FCT0	IOADD 9	IOADD 8			DIO1	DIO3
2	PIN2	FC#	RD#	FCT2	WR#	UWS	IOADD 6	IOADD 3	IOADD 0	DIO0	DIO2
1	PIN0	START #	LD#	FCT1	GND	IOADD 5	IOADD 7	IOADD 4	IOADD 2	IOADD 1	VCC

PIN 'A1'

A

PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	PIN0	F1
A2	PIN2	F3
A3	PIN3	F4
A4	PIN5	F6
A5	PIN8	F9
A6	VCC	VCC
A7	PIN9	F10
A8	DIN2	F3
A9	DIN4	F5
A10	DIN5	F6
A11	DIN8	F9
B1	START#	F10
B2	FC#	F16
B3	PIN1	F2
B4	PIN4	F5
B5	PIN7	F8
B6	DIN1	F2
B7	DIN0	F1
B8	DIN3	F4

PGA PIN	PIN NAME	BURN-IN SIGNAL
B9	DIN6	F7
B10	DIN7	F8
B11	DIN10	F11
C1	LD#	F11
C2	RD#	F1
C5	PIN6	F7
C6	CLK	F0
C7	GND	GND
C10	DIN9	F10
C11	DIN11	F12
D1	FCT1	F13
D2	FCT2	F14
D10	DIN12	F13
D11	DIN13	F14
E1	GND	GND
E2	WR#	F2
E3	FCT0	F12
E9	DIN14	F15
E10	DIN15	F1

PGA PIN	PIN NAME	BURN-IN SIGNAL
E11	DIN16	F2
F1	IOADD5	F6
F2	UWS	F11
F3	IOADD9	F10
F9	GND	GND
F10	DIN21	F7
F11	DIN17	F3
G1	IOADD7	F8
G2	IOADD6	F7
G3	IOADD8	F9
G9	DIN18	F4
G10	DIN20	F6
G11	DIN19	F5
H1	IOADD4	F5
H2	IOADD3	F4
H10	DIN23	F9
H11	DIN22	F8
J1	IOADD2	F3
J2	IOADD0	F1

PGA PIN	PIN NAME	BURN-IN SIGNAL
J5	DIO6	F7
J6	DIO9	F10
J7	DIO10	F11
J10	DIO21	F7
J11	DIO23	F9
K1	IOADD1	F2
K2	DIO0	F1
K3	DIO1	F2
K4	DIO4	F5
K5	DIO7	F8
K6	DIO8	F9
K7	DIO12	F13
K8	DIO15	F1
K9	DIO18	F4
K10	DIO20	F6
K11	DIO22	F8
L1	VCC	VCC
L2	DIO2	F3
L3	DIO3	F4
L4	DIO5	F6

NOTES:

1. $V_{CC}/2$ (2.7V ± 10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5 ± 0.5V.
4. 0.1µf (min) capacitor between V_{CC} and GND per position.
5. F_O = 100KHz ± 10%, F1 = F0/2, F2 = F1/2 . . . F16 = F15/2, 40% - 60% Duty Cycle.
6. Input Voltage Limits: V_{IL} = 0.8V max. V_{IH} = 4.5V ± 10%.

Metallization Topology

DIE DIMENSIONS:
330 x 281 x 19 ± 1mils

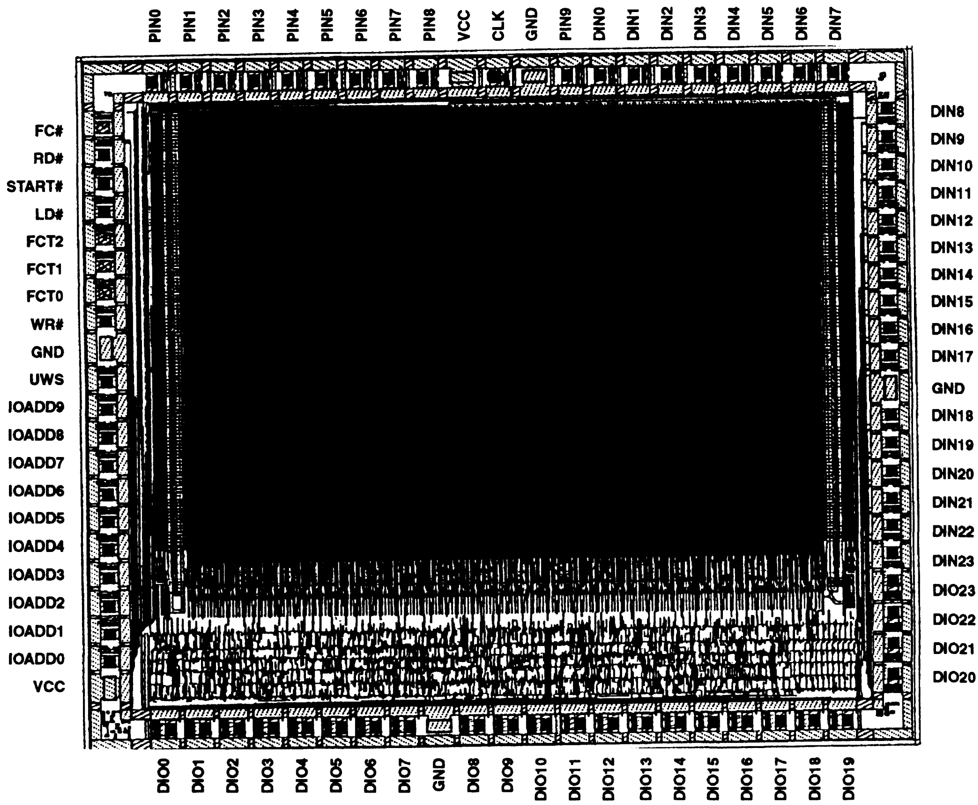
METALLIZATION:
Type: Si - Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:
0.47×10^5 A/cm^2

Metallization Mask Layout

HSP48410/883



HARRIS SEMICONDUCTOR

HSP48901

January 1994

3 x 3 Image Filter

Features

- DC to 30MHz Clock Rate
- Configurable for 1-D and 2-D Correlation/ Convolution
- Dual Coefficient Mask Registers, Switchable in a Single Clock Cycle
- Two's Complement or Unsigned 8-Bit Input Data and Coefficients
- 20-Bit Extended Precision Output
- Standard µP Interface

Applications

- Image Filtering
- Edge Detection/Enhancement
- Pattern Matching
- Real Time Video Filters

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP48901JC-20	0°C to +70°C	68 Lead PLCC
HSP48901JC-30	0°C to +70°C	68 Lead PLCC
HSP48901GC-20	0°C to +70°C	68 Lead PGA
HSP48901GC-30	0°C to +70°C	68 Lead PGA

Description

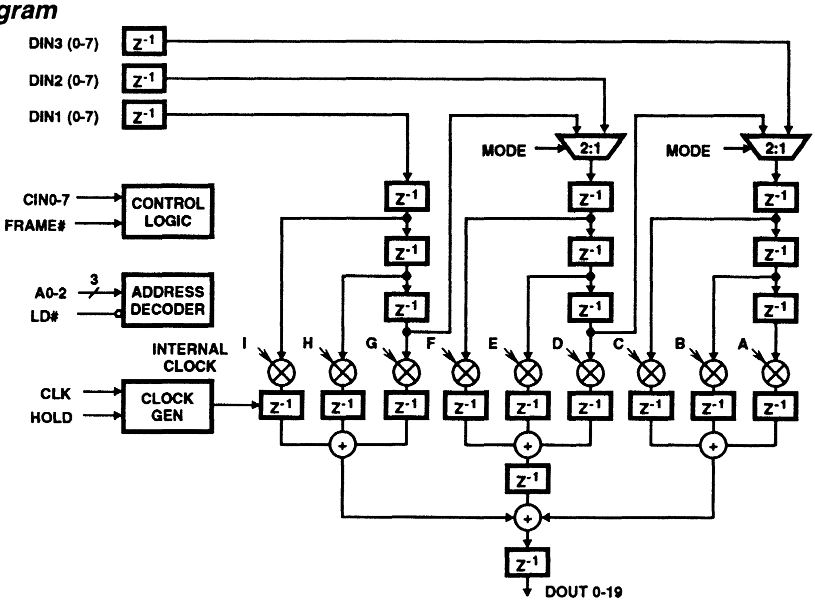
The Harris HSP48901 is a high speed 9-Tap FIR Filter which utilizes 8-bit wide data and coefficients. It can be configured as a one dimensional (1-D) 9-Tap filter for a variety of signal processing applications, or as a two dimensional (2-D) filter for image processing. In the 2-D configuration, the device is ideally suited for implementing 3 x 3 kernel convolution. The 30MHz clock rate allows a large number of image sizes to be processed within the required frame time for real-time video.

Data is provided to the HSP48901 through the use of programmable data buffers such as the HSP9500 or any other programmable shift register. Coefficient and pixel input data are 8-bit signed or unsigned integers, and the 20-bit extended output guarantees no overflow will occur during the filtering operation.

There are two internal register banks for storing independent 3 x 3 filter kernels, thus facilitating the implementation of adaptive filters and multiple filter operations on the same data.

The configuration of the HSP48901 Image Filter is controlled through a standard microprocessor interface and all inputs and outputs are TTL compatible.

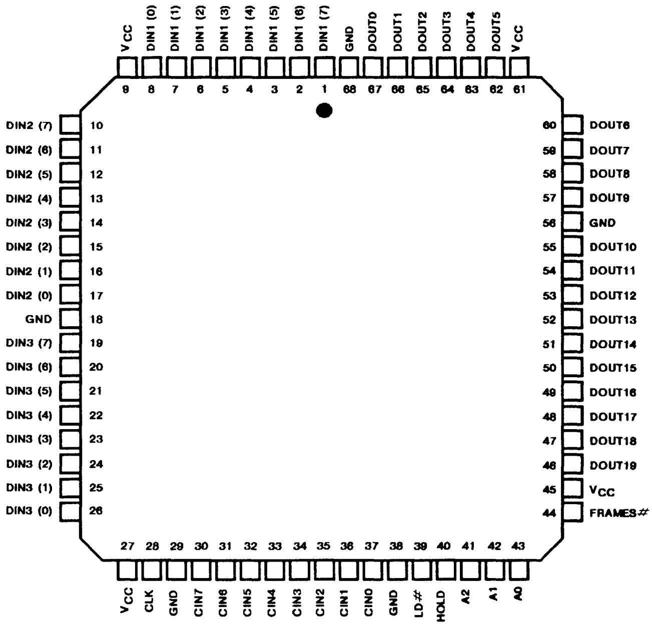
Block Diagram



File Number **2459.4**

Package Pinouts

68 LEAD PLCC
TOP VIEW



68 PIN GRID ARRAY
TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L
11		DOUT6	DOUT7	DOUT9	DOUT10	DOUT12	DOUT14	DOUT16	DOUT18	V_{CC}	
10	DOUT5	V_{CC}	DOUT8	GND	DOUT11	DOUT13	DOUT15	DOUT17	DOUT19	FRAME #	A0
9	DOUT3	DOUT4								A2	A1
8	DOUT1	DOUT2								LD#	HOLD
7	GND	DOUT0								CIN0	GND
6	DIN1 (6)	DIN1 (7)								CIN2	CIN1
5	DIN1 (4)	DIN1 (5)								CIN4	CIN3
4	DIN1 (2)	DIN1 (3)								CIN6	CIN5
3	DIN1 (0)	DIN1 (1)								GND	CIN7
2	V_{CC}	DIN2 (7)	DIN2 (5)	DIN2 (3)	DIN2 (1)	GND	DIN3 (6)	DIN3 (4)	DIN3 (2)	V_{CC}	CLK
1		DIN2 (6)	DIN2 (4)	DIN2 (2)	DIN2 (0)	DIN3 (7)	DIN3 (5)	DIN3 (3)	DIN3 (1)	DIN3 (0)	

Pin Descriptions

NAME	PLCC PIN	TYPE	DESCRIPTION
VCC	9, 27, 45, 61		The +5V power supply pins. 0.1µF capacitors between the VCC and GND pins are recommended.
GND	18, 29, 38, 56		The device ground.
CLK	28	I	Input and System clock. Operations are synchronous with the rising edge of this clock signal.
DIN1(7-0)	1-8	I	Pixel Data Input bus #1. These inputs are used to provide 8-bit pixel data to the HSP48901. The data must be provided in a synchronous fashion, and is latched on the rising edge of the CLK signal. The DIN1(0-7) inputs are also used to input data when operating in the 9 Tap FIR mode.
DIN2(7-0)	10-17	I	Pixel Data Input bus #2. Same as above. These inputs should be grounded when operating in the 1D mode.
DIN3(7-0)	19-26	I	Pixel Data Input bus #3. Same as above. These inputs should be grounded when operating in the 1D mode.
CIN7-0	30-37	I	Coefficient Data Input bus. This input bus is used to load the Coefficient Mask register(s) and the Initialization register. The register to be loaded is defined by the register address bits A0-2. The CIN0-7 data is loaded to the addressed register through the use of the LD# input.
DOUT19-0	46-55, 57-60, 62-67	O	Output Data bus. This 20-Bit output port is used to provide the convolution result. The result is the sum of products of the input data samples and their corresponding coefficients.
FRAME#	44	I	Frame# is an asynchronous new frame or vertical sync input. A low on this input resets all internal circuitry except for the Coefficient and INT registers. Thus, after a Frame# reset has occurred, a new frame of pixels may be convolved without reloading these registers.
HOLD	40	I	The Hold Input is used to gate the clock from all of the internal circuitry of the HSP48901. This signal is synchronous, is sampled on the rising edge of CLK and takes effect on the following cycle. While this signal is active (high), the clock will have no effect on the HSP48901 and internal data will remain undisturbed.
A2-0	41-43	I	Control Register Address. These lines are decoded to determine which register in the control logic is the destination for the data on the CIN0-7 inputs. Register loading is controlled by the A0-2 and LD# inputs.
LD#	39	I	Load Strobe. LD# is used for loading the internal registers of the HSP48901. The rising edge of LD# will latch the CIN0-7 data into the register specified by A0-2. The Address on A0-2 must be set up with respect to the falling edge of LD# and must be held with respect to the rising edge of LD#.

Functional Description

The HSP48901 can perform convolution of a 3 x 3 filter kernel with 8-bit image data. It accepts the image data in a raster scan, non-interlaced format, convolves it with the filter kernel and outputs the filtered image. The input and filter kernel data are both 8-bits, while the output data is 20-bits to prevent overflow during the convolution operation. Image data is input via the DIN1, DIN2, and DIN3 busses. This data would normally be provided by programmable data buffer such as the HSP9501 as illustrated in the operations section of this specification. The data is then convolved with the 3 x 3 array of filter coefficients. The resultant output data is then stored in the output register. The HSP48901 may also be used in a one-dimensional mode. In this configuration, it functions as a 1-D 9-tap FIR filter. Data would be input via the DIN1(0-7) bus for operation in this mode.

Initialization of the convolver is done using the CIN0-7 bus to load configuration data and the filter kernel(s). The address lines A0-2 are used to address the internal registers for initialization. The configuration data is loaded using the A0-2, CIN0-7 and LD# controls as address, data and write enable, respectively. This interface is compatible with standard microprocessors without the use of any additional glue logic.

Filtered image data is output from the convolver over the DOUT0-19 bus. This output bus is 20-bits wide to provide room for growth during the convolution operation.

8-Bit Multiplier Array

The multiplier array consists of nine 8 x 8 multipliers. Each multiplier forms the product of a filter coefficient with a corresponding pixel in the input image. Input and coefficient data may be in either two's complement or unsigned integer format. The nine coefficients form a 3 x 3 filter kernel which is multiplied by the input pixel data and summed to form a sum of products for implementation of the convolution operation as shown below:

FILTER KERNEL			INPUT DATA		
A	B	C	P1	P2	P3
D	E	F	P4	P5	P6
G	H	I	P7	P8	P9

OUTPUT = (A x P1) + (B x P2) + (C x P3)
+ (D x P4) + (E x P5) + (F x P6)
+ (G x P7) + (H x P8) + (I x P9)

Control Logic

The control logic (Figure 1) contains the Initialization Register and the Coefficient Registers. The control logic is updated by placing data on the CIN0-7 bus and using the A0-2 and LD# control lines to write to the addressed register (see Address Decoder). All of the control logic registers are unaffected by FRAME#.

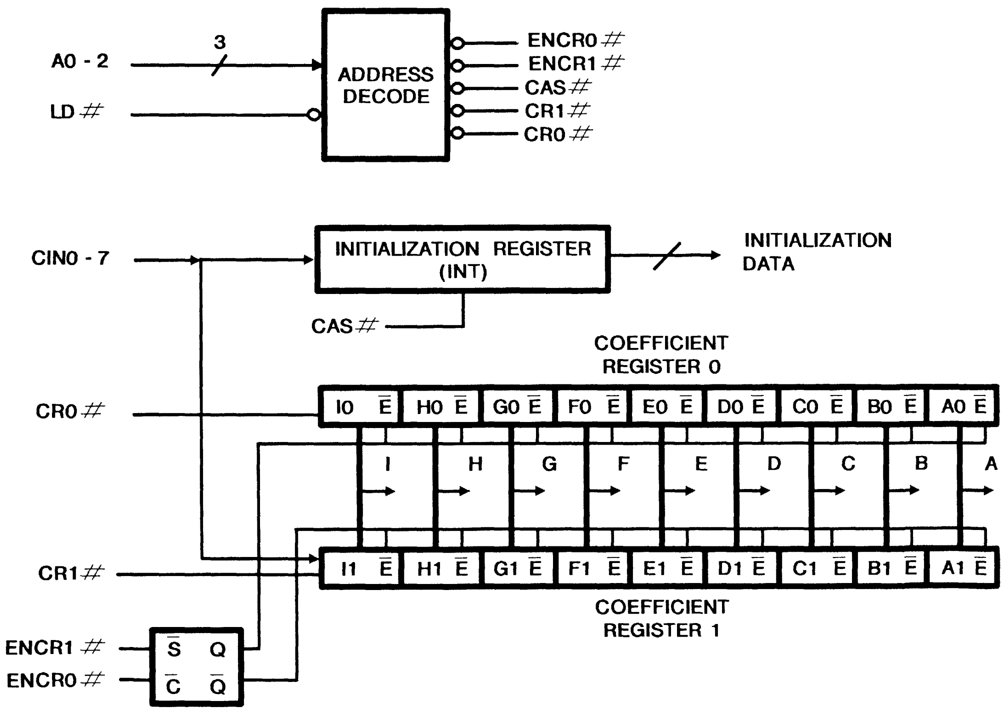


FIGURE 1. CONTROL LOGIC BLOCK DIAGRAM

Initialization Register

The initialization register is used to appropriately configure the convolver for a particular application. It is loaded through the use of the CIN0-7 bus along with the LD# input. Bit 0 defines the input data and coefficients format (unsigned or two's complement); Bit 1 defines the mode of operation (1-D or 2- D); and Bits 2 and 3 determine the type of rounding to occur on the DOUT0-19 bus; The complete definition of the initialization register bits is given in Table 1.

TABLE 1. INITIALIZATION REGISTER DEFINITION

INITIALIZATION REGISTER		
BIT 0		FUNCTION = Input & Coefficient Data Format
0		Unsigned Integer format
1		Two's complement format
BIT 1		FUNCTION = Operating Mode
0		1-D 9-tap filter
1		2-D 3 x 3 filter
3 BIT	2	FUNCTION = Output Rounding
0	0	No Rounding
0	1	Round to 16 bits (i.e. DOUT19-4)
1	0	Round to 8 bits (i.e. DOUT19-12)
1	1	Not Valid

Coefficient Registers (CREG0, CREG1)

The control logic contains two coefficient register banks, CREG0 and CREG1. Each of these register banks is capable of storing nine 8-bit filter coefficient values (3 x 3 Kernel). The output of the registers are connected to the coefficient input of the corresponding multiplier in the 3 x 3 multiplier array (designated A through I). The register bank to be used for the convolution is selectable by writing to the approprite address (See address decoder). All registers in a given bank are enabled simultaneously, and one of the banks is always active.

For most applications, only one of the register banks is necessary. The user can simply load CREG0 after power up, and use it for the entire convolution operation. (CREG0 is the default register). The alternate register bank allows the user to maintain two sets of filter coefficients and switch between them in real time. The coefficient masks are loaded via the CIN0-7 bus by using A0-2 and LD#. The selection of the particular register bank to be used in processing is also done by writing to the appropriate address (See address decoder). For example, if CREG0 is being used to provide coefficients to the multipliers, CREG1 can be updated at a low rate by an external processor; then, at the proper time, CREG1 can be selected, so that the new coefficient mask is used to process the data. Thus, no clock cycles have been lost when changing between alternate 3 x 3 filter kernels.

The nine coefficients must be loaded sequentially over the CIN0-7 bus from A to I. The address of CREG0 or CREG1 is placed on A0-2, and then the coefficients are written to the corresponding coefficient register one at a time by using the LD# input.

Address Decoder

The address decoder (See Figure 1) is used for writing to the control logic of the HSP48901. Loading an internal register is done by selecting the destination register with the A0-2 address lines, placing the data on CIN0-7, and asserting LD# control line. When LD# goes high, the data on CIN0-7 is latched into the addressed register. The address map for the A0-2 bus is shown in Table 2.

While loading of the control logic registers is asynchronous to CLK, the target register in the control logic is being read synchronous to the internal clock. Therefore, care must be taken when modifying the convolver setup parameters during processing to avoid changing the contents of the registers near a rising edge of CLK. The required setup time relative to CLK is given by the specification TLCS. For example, in order to change the active coefficient register from CREG0 to CREG1 during an active convolution operation, a write will be performed to the address for selecting CREG1 for internal processing (A0-2 = 110). In order to provide proper uninterrupted operation, LD# should be deasserted at least TLCS prior to the next rising edge of CLK. Failure to meet this setup time may result in unpredictable results on the output of the convolver. Keep in mind that this requirement applies only to the case where changes are being made in the control logic during an active convolution operation. In a typical convolver configuration routine, where the configuration data is loaded prior to the actual convolution operation, this specification would not apply.

TABLE 2. ADDRESS MAP

CONTROL LOGIC ADDRESS MAP			
A2-0			FUNCTION
0	0	0	Reserved for future use
0	0	1	Reserved for future use
0	1	0	Load Coefficient Register 0 (CREG0)
0	1	1	Load Coefficient Register 1 (CREG1)
1	0	0	Load Initialization Register (INT)
1	0	1	Select CREG0 for Internal Processing
1	1	0	Select CREG1 for Internal Processing
1	1	1	No Operation

Control Signals

Hold

The HOLD control input provides the ability to disable internal clock and stop all operations temporarily. HOLD is sampled on the rising edge of CLK and takes effect during the following clock cycle (Refer to Figure 2). This signal can be used to momentarily ignore data at the input of the convolver while maintaining its current output data and operational state.

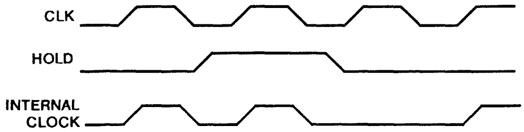


FIGURE 2. HOLD OPERATION

FRAME#

The FRAME# input initializes all internal flip flops and registers except for the coefficient and initialization registers. It is used as a reset between video frames and eliminates the need to re-initialize the entire HSP48901 or reload the coefficients. The registers and flip flops will remain in a reset state as long as FRAME# is active. FRAME# is an asynchronous input and may occur at any time. However, it must be deasserted at least tFS ns prior to the rising clock edge that is to begin operation for the next frame in order to ensure the new pixel data is properly loaded.

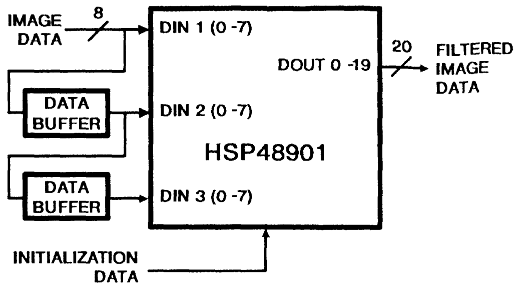
Operation

A single HSP48901 can be used to perform 3 x 3 convolution on 8-bit image data. A block diagram of this configuration is shown in Figure 3. The inputs of an external data buffer (such as the HSP9501) are connected to the input data in parallel with the DIN1(0-7) lines; the outputs of the data buffer are connected to the DIN2(0-7) bus. A second external data buffer is connected between the outputs of the first buffer and the DIN3(0-7) inputs. To perform the convolution operation, a group of nine image pixels is multiplied by the 3 x 3 array of filter coefficients and their products are summed and sent to the output. For the example in figure 3, the pixel value in the output image at location m,n is given by:

$$\begin{aligned}DOUT(m,n) = \; & A \times P_{m-1,n-1} + B \times P_{m-1,n} + C \times P_{m-1,n+1} \\ & + D \times P_{m,n-1} + E \times P_{m,n} + F \times P_{m,n+1} \\ & + G \times P_{m+1,n-1} + H \times P_{m+1,n} + I \times P_{m+1,n+1}\end{aligned}$$

This process is continually repeated until the last pixel of the last row of the image has been input. It can then start again with the first row of the next frame. The FRAME# pin is used to clear the internal multiplier registers and DOUT0-19 registers between frames. The row length of the image to be convolved is limited only by the maximum length of the external data buffers.

The setup is straightforward. The user must first setup the HSP48901 by loading a new value into the initialization register. The coefficients can now be loaded one at a time from A to I via the CIN0-7 coefficient bus, and the A0-2 and LD# control lines.



A	B	C	$P_{M-1,N-1}$	$P_{M-1,N}$	$P_{M-1,N+1}$
D	E	F	$P_{M,N-1}$	$P_{M,N}$	$P_{M,N+1}$
F	H	I	$P_{M+1,N-1}$	$P_{M+1,N}$	$P_{M+1,N+1}$

FILTER KERNEL — IMAGE DATA

FIGURE 3. 3 x 3 KERNEL ON AN 8-BIT IMAGE

Multiple filter kernels can also be used on the same image data using the dual coefficient registers CREG0 and CREG1. This type of filtering is used when the characteristics of the input pixel data change over the image in such a way that no one filter produces satisfactory results for the entire image. In order to filter such an image, the characteristics of the filter itself must change while the image is being processed. The HSP48901 can perform this function with the use of an external processor. The processor is used to calculate the required new filter coefficients, loads them into the coefficient register not in use, and selects the newly loaded coefficient register at the proper time. The first coefficient register can then be loaded with new coefficients in preparation for the next change. This can be carried out with no interruption in processing, provided that the new register is selected synchronous to the convolver CLK signal.

The HSP48901 can also operate as a one dimensional 9 tap FIR filter by programming the initialization register to 1-D mode (i.e. INT bit 1 = '0'). This configuration will provide for nine sequential input values to be multiplied by the coefficient values in the selected coefficient register and provide the proper filtered output. The input bus to be used when operating in this mode is the DIN1(0-7) inputs.

The equation for the output in the 1-D 9-tap FIR case becomes:

$$\begin{aligned}DOUT_n = \; & A \times D_{n-8} + B \times D_{n-7} + C \times D_{n-6} + D \times D_{n-5} \\ & + E \times D_{n-4} + F \times D_{n-3} + G \times D_{n-2} + H \times D_{n-1} \\ & + I \times D_n\end{aligned}$$

Frame Rate

The total time to process an image is given by the formula:

$$T = R \times C / F$$

where:
- T = Time to process a frame
- R = number of rows in the image
- C = number of pixels in a row
- F = clock rate of the HSP48901

Absolute Maximum Ratings

Supply Voltage	+8.0V
Input, Output or I/O Voltage Applied	GND -0.5V to V_{CC} +0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation at +70°C	PGA Package = 2.56W, PLCC Package = 1.9W
Thermal Impedance Junction To Ambient (θ_{ja})	PGA Package = 41°C/W, PLCC Package = 42.8°C/W
Thermal Impedance Junction To Case (θ_{jc})	PGA Package = 16°C/W, PLCC Package = 14.9°C/W
Gate Count	13,594 Gates
Junction Temperature (T_J)	PGA Package = +175°C, PLCC Package = +150°C
Lead Temperature (Soldering, Ten Seconds)	+300°C
ESD Classification	Class 1

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range	+4.75V to +5.25V
Operating Temperature Range	0°C to +70°C

D.C. Electrical Specifications (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	VIH	2.0	-	V	V_{CC} = 5.25V
Logical Zero Input Voltage	VIL	-	0.8	V	V_{CC} = 4.75V
High Level Clock Input	VIHC	3.0	-	V	V_{CC} = 5.25V
Low Level Clock Input	VILC	-	0.8	V	V_{CC} = 4.75V
Output HIGH Voltage	VOH	2.6	-	V	I_{OH} = -400μA, V_{CC} = 4.75V
Output LOW Voltage	VOL	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.75V
Input Leakage Current	II	-10	10	μA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V
Standby Power Supply Current	ICCSB	-	500	μA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Outputs Open
Operating Power Supply Current	ICCOP	-	120	mA	f = 20MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.25V (Note 1)

Capacitance (T_A = +25°C, Note 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Capacitance	CIN	-	10	pF	FREQ = 1 MHz, V_{CC} = Open, all measurements are referenced to device ground.
Output Capacitance	CO	-	15	pF	

NOTES: 1. Power supply current is proportional to operating frequency. Typical rating for ICCOP is 6mA/MHz.

2. Not tested, but characterized at initial design and at major process/design changes.

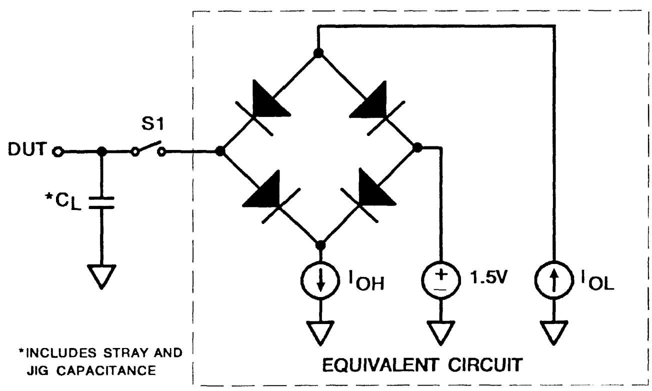
CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

A.C. Electrical Specifications (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C)

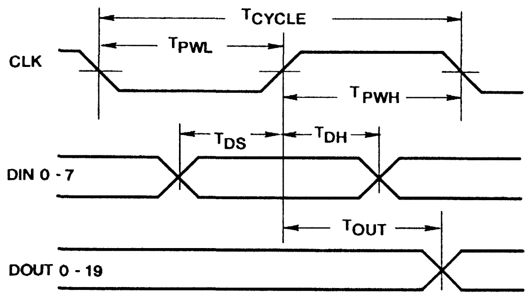
PARAMETER	SYMBOL	-30		-20		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Clock Period	T_{CYCLE}	33	-	50	-	ns	
Clock Pulse Width High	T_{PWH}	13	-	20	-	ns	
Clock Pulse Width Low	T_{PWL}	13	-	20	-	ns	
Data Input Setup Time	T_{DS}	14	-	16	-	ns	
Data Input Hold Time	T_{DH}	0	-	0	-	ns	
Clock to Data Out	T_{OUT}	-	21	-	30	ns	
Address Setup Time	T_{AS}	5	-	5	-	ns	
Address Hold Time	T_{AH}	2	-	2	-	ns	
Configuration Data Setup Time	T_{CS}	10	-	12	-	ns	
Configuration Data Hold Time	T_{CH}	0	-	0	-	ns	
LD# Pulse Width	T_{LPW}	13	-	20	-	ns	
LD# Setup Time	T_{LCS}	31	T_{CYCLE}+2	40	T_{CYCLE}+2	ns	Note 1
HOLD Setup Time	T_{HS}	10	-	12	-	ns	
HOLD Hold Time	T_{HH}	0	-	0	-	ns	
FRAME# Pulse Width	T_{FPW}	T_{CYCLE}	-	T_{CYCLE}	-	ns	
FRAME# Setup Time	T_{FS}	28	-	40	-	ns	Note 2
Output Rise Time	T_R	-	8	-	8	ns	From 0.8V to 2.0V
Output Fall Time	T_F	-	8	-	8	ns	From 2.0V to 0.8V

NOTES:
1. This specification applies only to the case where a change in the active coefficient register is being selected during a convolution operation. It must be met in order to achieve predictable results at the next rising clock edge. In most applications, this selection will be made asynchronously, and the T_{LCS} specification may be disregarded.
2. While FRAME# is asynchronous with respect to CLK, it must be deasserted a minimum of T_{FS} ns prior to the rising clock edge which is to begin loading new pixel data for the next frame.
3. A.C. Testing is performed as follows: Input levels (CLK Input) = 4.0V and 0V; Input levels (All other Inputs) = 0V to 3.0V; Input timing reference levels: (CLK) = 2.0V, (Others) = 1.5V; Other timing references: $V_{OH} \geq 1.5V$, $V_{OL} \leq 1.5V$; Output load per test load circuit with C_L = 40pF.

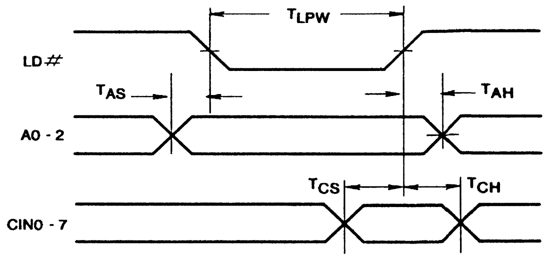
Test Load Circuit



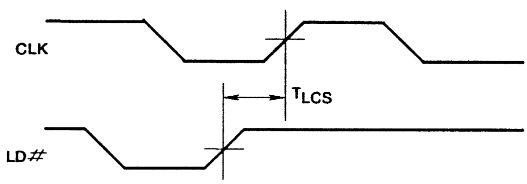
Timing Waveforms



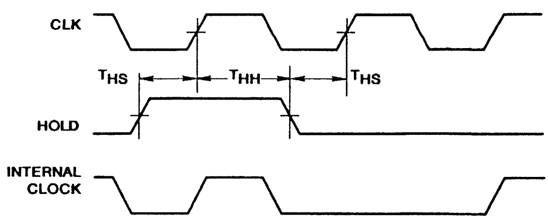
FUNCTIONAL TIMING



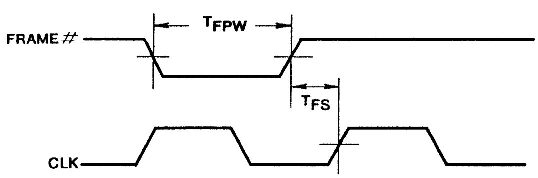
CONFIGURATION TIMING



SYNCHRONOUS LOAD TIMING



HOLD TIMING



FRAME# TIMING

HARRIS SEMICONDUCTOR

HSP48908

January 1994

Two Dimensional Convolver

Features

- Single Chip 3 x 3 Kernel Convolution
- Programmable On-Chip Row Buffers
- DC to 32MHz Clock Rate
- Cascadable for Larger Kernels and Images
- On-Chip 8-Bit ALU
- Dual Coefficient Mask Registers, Switchable in a Single Clock Cycle
- 8-Bit Signed or Unsigned Input and Coefficient Data
- 20-Bit Extended Precision Output
- Standard μP Interface
- Low Power CMOS

Applications

- Image Filtering
- Edge Detection
- Adaptive Filtering
- Real Time Video Filters

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP48908VC-20	0°C to +70°C	100 Lead MQFP
HSP48908VC-32	0°C to +70°C	100 Lead MQFP
HSP48908JC-20	0°C to +70°C	84 Lead PLCC
HSP48908JC-32	0°C to +70°C	84 Lead PLCC
HSP48908GC-20	0°C to +70°C	84 Lead PGA
HSP48908GC-32	0°C to +70°C	84 Lead PGA

Description

The Harris HSP48908 is a high speed Two Dimensional Convolver which provides a single chip implementation of a video data rate 3 x 3 kernel convolution on two dimensional data. It eliminates the need for external data storage through the use of the on-chip row buffers which are programmable for row lengths up to 1024 pixels.

There are internal register banks for storing two independent 3 x 3 filter kernels, thus facilitating the implementation of adaptive filters and multiple filter operations on the same data. The pixel data path also includes an on-chip ALU for performing real-time arithmetic and logical pixel point operations.

Data is provided to the HSP48908 in a raster scan noninterlaced fashion, and is internally buffered on images up to 1024 pixels wide for the 3 x 3 convolution operation. Images with larger rows and convolution with larger kernel sizes can be accommodated by using external row buffers and/or multiple HSP48908s. Coefficient and pixel input data are 8-bit signed or unsigned integers, and the 20-bit convolver output guarantees no overflow for kernel sizes up to 4 x 4. Larger kernel sizes can be implemented however, since the filter coefficients will normally be less than their maximum 8-bit values.

The HSP48908 is manufactured using an advanced CMOS process, and is a low power fully static design. The configuration of the device is controlled through a standard microprocessor interface and all inputs/outputs are TTL compatible.

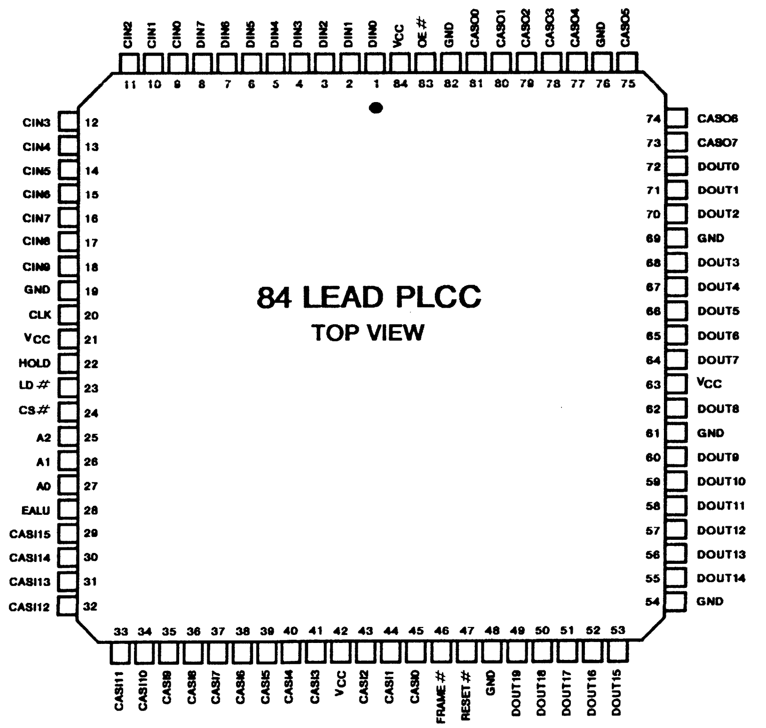
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2456.

Package Pinouts

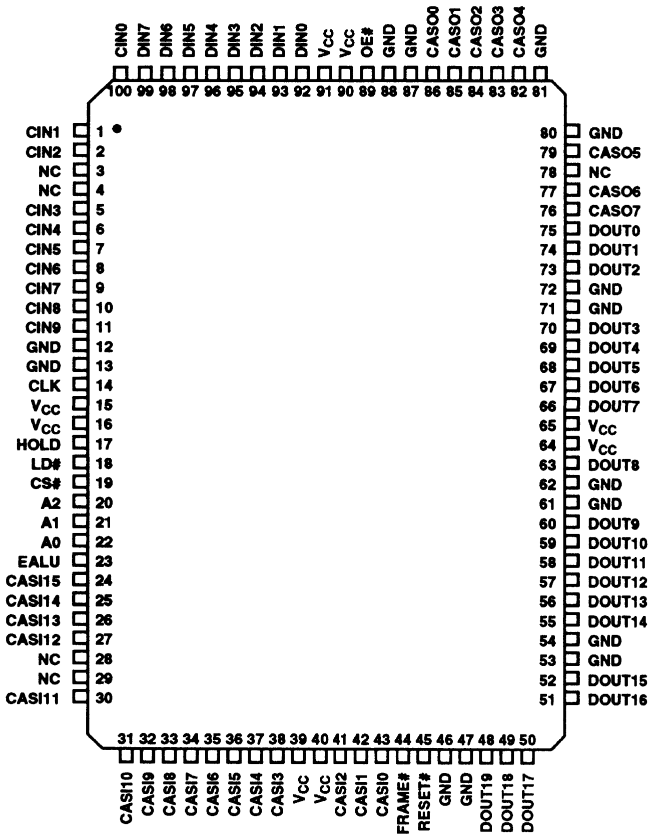
84 PIN PGA
TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L
11	CASO6	DOUT0	DOUT1	GND	DOUT5	DOUT6	DOUT8	DOUT10	DOUT12	DOUT13	DOUT15
10	CASO4	CASO5	CASO7	DOUT2	DOUT4	DOUT9	GND	DOUT11	DOUT14	GND	DOUT17
9	CASO3	GND			DOUT3	DOUT7	V_{CC}			DOUT16	DOUT18
8	CASO1	CASO2								DOUT19	GND
7	OE#	GND	V_{CC}						CASI1	FRAME #	CASI0
6	DIN1	CASO0	DIN0						CASI2	V_{CC}	RESET #
5	DIN2	DIN3	DIN4						CASI5	CASI4	CASI3
4	DIN5	DIN6								CASI7	CASI6
3	DIN7	CIN1			CIN9	HOLD	LD#			CASI10	CASI8
2	CIN0	CIN3	CIN4	CIN7	GND	V_{CC}	A2	EALU	CASI13	CASI11	CASI9
1	CIN2	CIN5	CIN6	CIN8	CLK	A1	CS#	A0	CASI15	CASI14	CASI12

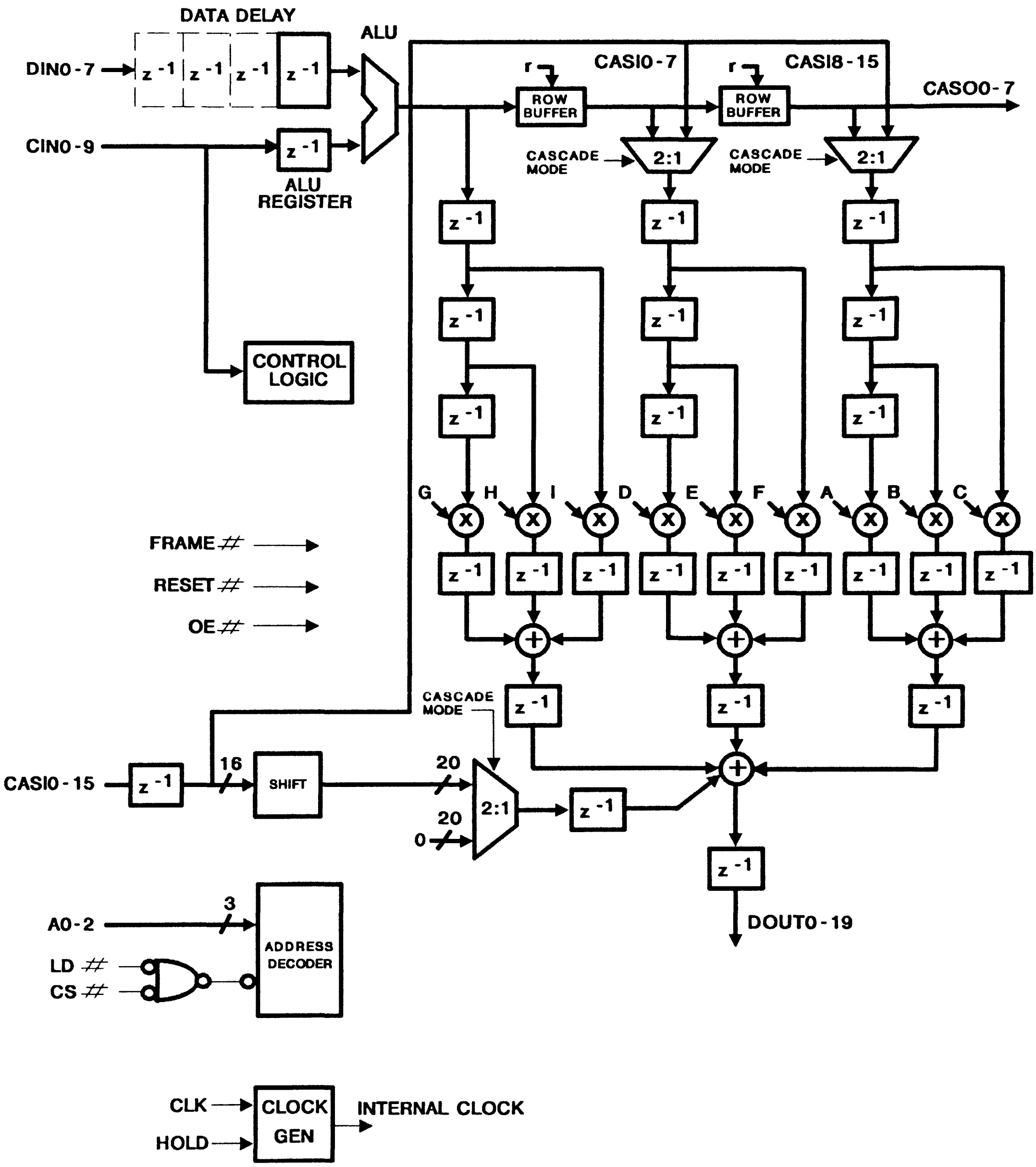


Pinouts (Continued)

100 LEAD MQFP
TOP VIEW



Block Diagram



Pin Descriptions

NAME	PLCC PIN	TYPE	DESCRIPTION
V_{CC}	21, 42, 63, 84		The +5V power supply pins. 0.1μF capacitors between the V_{CC} and GND pins are recommended.
GND	19, 48, 54, 61 69, 76, 82		The device ground.
CLK	20	I	Input and System clock. Operations are synchronous with the rising edge of this clock signal.
DIN0-7	1-8	I	Pixel Data input bus. This bus is used to provide the 8-bit pixel input data to the HSP48908. The data must be provided in a synchronous fashion, and is latched on the rising edge of the CLK signal.
CIN0-9	9-18	I	Coefficient Input bus. This input bus is used to load the Coefficient Mask register(s), the Initialization register, the Row Buffer length register and the ALU microcode. It may also be used to provide a second operand input to the ALU. The definition of the CIN0-9 bits is defined by the register address bits A0-2. The CIN0-9 data is loaded to the addressed register through the use of the CS# and LD# inputs.
DOUT0-19	49-53, 55-60, 62, 64-68, 70-72	O	Output Data bus. This 20-Bit output port is used to provide the convolution result. The result is the sum of products of the input data samples and their corresponding coefficients. The Cascade inputs CASI0-15 may also be added to the result by selecting the appropriate cascade mode in the Initialization register.
CASI0-15	29-41, 43-45	I	Cascade Input bus. This bus is used for cascading multiple HSP48908s to allow convolution with larger kernels or row sizes. It may also be used to interface to external row buffers. The function of this bus is determined by the Cascade Mode bit (Bit 0) of the Initialization register. When this bit is set to a '0', the value on CASI0-15 is left shifted and added to DOUT0-19. The amount of the shift is determined by bits 7-8 of the Initialization register. While this mode is intended primarily for cascading, it may also be used to add an offset value, such as to increase the brightness of the convolved image. When the Cascade mode bit is set to a '1', this bus is used for interfacing to external row buffers. In this mode the bus is divided into two 8-bit busses (CASI0-7 and CASI8-15), thus allowing two additional pixel data inputs. The cascade data is sent directly to the internal multiplier array which allows for larger row sizes without using multiple HSP48908s.
CASO0-7	73-75, 77-81	O	Cascade Output bus. This bus is used primarily during cascading to handle larger frames and/or kernel sizes. This output data is the data on DIN0-7 delayed by twice the programmed internal row buffer length.
FRAME#	46	I	Frame# is an asynchronous new frame or vertical sync input. A low on this input resets all internal circuitry except for the Coefficient, ALU, AMC, EOR and INT registers. Thus, after a Frame# reset has occurred, a new frame of pixels may be convolved without reloading these registers.
EALU	28	I	Enable ALU Input. This control line gates the clock to the ALU Register. When it is high, the data on CIN0-7 is loaded on the next rising clock edge. When EALU is low, the last value loaded remains in the ALU register.
HOLD	22	I	The Hold Input is used to gate the clock from all of the internal circuitry of the HSP48908. This signal is synchronous, is sampled on the rising edge of CLK and takes effect on the following cycle. While this signal is active (high), the clock will have no effect on the HSP48908 and internal data will remain undisturbed.
RESET#	47	I	Reset is an asynchronous signal which resets all internal circuitry of the HSP48908. All outputs are forced low in the reset state.
OE#	83	I	Output Enable. The OE# input controls the state of the Output Data bus (DOUT0-19). A LOW on this control line enables the port for output. When OE# is HIGH, the output drivers are in the high impedance state. Processing is not interupted by this pin.

Pin Descriptions (Continued)

NAME	PLCC PIN	TYPE	DESCRIPTION
A0-2	25-27	I	Control Register Address. These lines are decoded to determine which register in the control logic is the destination for the data on the CIN0-9 inputs. Register loading is controlled by the A0-2, LD# and CS# inputs.
LD#	23	I	Load Strobe. LD# is used for loading the internal registers of the HSP48908. When CS# and LD# are active, the rising edge of LD# will latch the CIN0-7 data into the register specified by A0-2.
CS#	24	I	Chip Select. The Chip Select input enables loading of the internal registers. When CS# is low, the A0-2 address lines are decoded to determine the meaning of the data on the CIN0-7 bus. The rising edge of LD# will then load the addressed register.

Functional Description

The HSP48908 two-dimensional convolver performs convolution of 3 x 3 filter kernels. It accepts the image data in raster scan, non-interlaced format, convolves it with the filter kernel and outputs the filtered image. The input and filter kernel data are both 8-bits, while the output data is 20-bits to prevent overflow during the convolution operation. The HSP48908 has internal storage for two 3 x 3 filter kernels and is capable of buffering two 1024 x 8-bit rows for true single chip operation at video frame rates. An 8-bit ALU in the input pixel data path allows the user to perform arithmetic and logical operations on the input data in real time during the convolution. Multiple devices can also be cascaded together for larger kernel convolution, larger frame sizes and increased precision.

Image data is input to the convolver via the DIN0-7 bus. The data is then operated on by the ALU, stored in the row buffers and convolved with the 3 x 3 array of filter coefficients. The resultant output data is then latched into the output register. The row buffers are preprogrammed to the length of one row of the input image to enable the user to input the image data one pixel at a time in raster scan format without having to provide external storage.

Initialization of the convolver is done using the CIN0-7 bus to load configuration data, such as the filter kernel(s) and the length of the row buffers. The address lines A0-2 are used to address the internal registers for initialization. The configuration data is loaded using the A0-2, CIN0-9, CS# and LD# controls as address, data, chip select and write enable, respectively. This interface is compatible with standard microprocessors without the use of any additional glue logic.

Filtered image data comes out of the convolver over the DOUT0-19 bus. This output bus is 20-bits wide to provide room for growth during the convolution operation. The 20-bit bus will allow the use of up to 4 x 4 kernels (using multiple 48908's) without overflow. However, in practical applications, much larger kernel sizes can be implemented without overflow since the filter coefficients are typically much smaller than 8-bit full scale values. DOUT0-19 is also a registered, three state bus to facilitate cascading multiple chips and to allow the HSP48908 to reside on a standard microprocessor system bus.

Multiple convolvers can also be cascaded together for kernel sizes larger than 3 x 3 and for convolution on images with row lengths longer than 1024 pixels. The maximum kernel size is dependent upon the magnitude of the image data and the coefficients in a given application; care must always be taken with very large kernel sizes to prevent overflow of the 20-bit output.

Data Input

Image data coming into the 2D Convolver passes through a programmable pipeline delay before being sent to the ALU. The amount of delay (1 to 4 clock cycles) is set in the initialization register during configuration setup (See Control Logic). Delays greater than one are used primarily in cascading multiple HSP48908s to align data sequences for proper output (See Operation).

Arithmetic Logic Unit

The on-chip ALU provides the user with the capability of performing pixel point operations on incoming image data. Depending on the instruction in the ALU microcode register, the ALU can perform any one of 19 arithmetic and logical functions, and shift the resulting number left or right by up to 3 bits. Tables 1 and 2 show the available ALU functions and the 10-bit associated microcode to be loaded into the ALU microcode register. Note that the shifts take place on the output of the ALU and are completely independent of the logical or arithmetic operation being performed. The first input (A) of the ALU is taken from the pixel input bus (DIN0-7). The second input (B) is taken from the ALU Register. The ALU Register is loaded via the CIN0-7 bus while the EALU control line is valid (see EALU).

TABLE 1. ALU SHIFT OPERATIONS

ALU MICROCODE REGISTER			
REGISTER BIT			
9	8	7	OPERATION
0	0	0	No Shift (Default)
0	0	1	Shift Right 1
0	1	0	Shift Right 2
0	1	1	Shift Right 3
1	0	0	Shift Left 1
1	0	1	Shift Left 2
1	1	0	Shift Left 3
1	1	1	Not Valid

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TABLE 2. ALU PIXEL OPERATIONS

REGISTER BIT							OPERATION
6	5	4	3	2	1	0	
0	0	0	0	0	0	0	Logical (00000000)
1	1	1	1	0	0	0	Logical (11111111)
0	0	1	1	0	0	0	Logical (A) (Default)
0	1	0	1	0	0	0	Logical (B)
1	1	0	0	0	0	0	Logical (A#)
1	0	1	0	0	0	0	Logical (B#)
0	1	1	0	0	0	1	Arithmetic (A + B)
1	0	0	1	0	1	0	Arithmetic (A - B)
1	0	0	1	1	0	0	Arithmetic (B - A)
0	0	0	1	0	0	0	Logical (A AND B)
0	0	1	0	0	0	0	Logical (A AND B#)
0	1	0	0	0	0	0	Logical (A# AND B)
0	1	1	1	0	0	0	Logical (A OR B)
1	0	1	1	0	0	0	Logical (A OR B#)
1	1	0	1	0	0	0	Logical (A# OR B)
1	1	1	0	0	0	0	Logical (A NAND B)
1	0	0	0	0	0	0	Logical (A NOR B)
0	1	1	0	0	0	0	Logical (A XOR B)
1	0	0	1	0	0	0	Logical (A XNOR B)

EALU

The EALU control pin enables loading of the ALU Register. While the EALU line is high, the data on CIN0-7 is latched into the ALU Register on the rising edge of CLK. When EALU goes low, the current value in the ALU register is held until EALU is again asserted. Note that the ALU loading operation makes use of the CIN0-7 inputs, but is completely independent of CS# and LD#. Therefore, in order to prevent overwriting an internal register, care must be taken to ensure that CS# and LD# are not active during an EALU cycle.

Programmable Row Buffers

The programmable row buffers are used for buffering raster input data for the convolution operation. They can be thought of as programmable shift registers which can each store up to 1024 8-bit values, thus delaying each pixel by up to 1024 clock cycles. Functionally, each row buffer can be represented as a set of registers connected as a 1024 x 8-bit serial shift register. The output of each buffer can be represented by the equation Q = D(n-r), where Q is the row buffer output, D is the buffer input, n is the current clock cycle and r is the preprogrammed row length of the input image. Since the two buffers are connected in series, the data at the cascade outputs (CASO0-7) is delayed by two row delays and may be used for cascading multiple convolvers for larger kernel sizes and/or row lengths. The programmable row buffers can also be bypassed by selecting the appropriate cascade mode in the initialization register. This mode allows the use of external row buffers for convolving with row lengths longer than 1024 pixels.

8-Bit Multiplier Array

The multiplier array consists of nine 8 x 8 multipliers. Each multiplier forms the product of a filter coefficient with a corresponding pixel in the input image. Input and coefficient data may be in either two's complement or unsigned integer format. The nine coefficients form a 3 x 3 filter kernel which is multiplied by the input pixel data and summed to form a sum of products for implementation of the convolution operation as shown below:

INPUT DATA			FILTER KERNEL
P1	P2	P3	A B C
P4	P5	P6	D E F
P7	P8	P9	G H I

OUTPUT = (A x P1) + (B x P2) + (C x P3)
+ (D x P4) + (E x P5) + (F x P6)
+ (G x P7) + (H x P8) + (I x P9)

Control Logic

The control logic (Figure 1) contains the ALU Microcode Register, the Initialization Register, the Row Length Register, and the Coefficient Registers. The control logic is updated by placing data on the CIN0-9 bus and using the A0-2, CS# and LD# control lines to write to the addressed register (see Address Decoder). All of the control logic registers are loaded with their default values on RESET#, and are unaffected by FRAME#.

ALU Microcode Register

The ALU microcode register is used to store the command word for the ALU. The ALU command word is a 10-bit instruction divided into two fields: the lower 7 bits determine the ALU operation and the upper 3 bits specify the number of shifts which occur. The ALU command words are defined in Tables 1 and 2 (See ALU section).

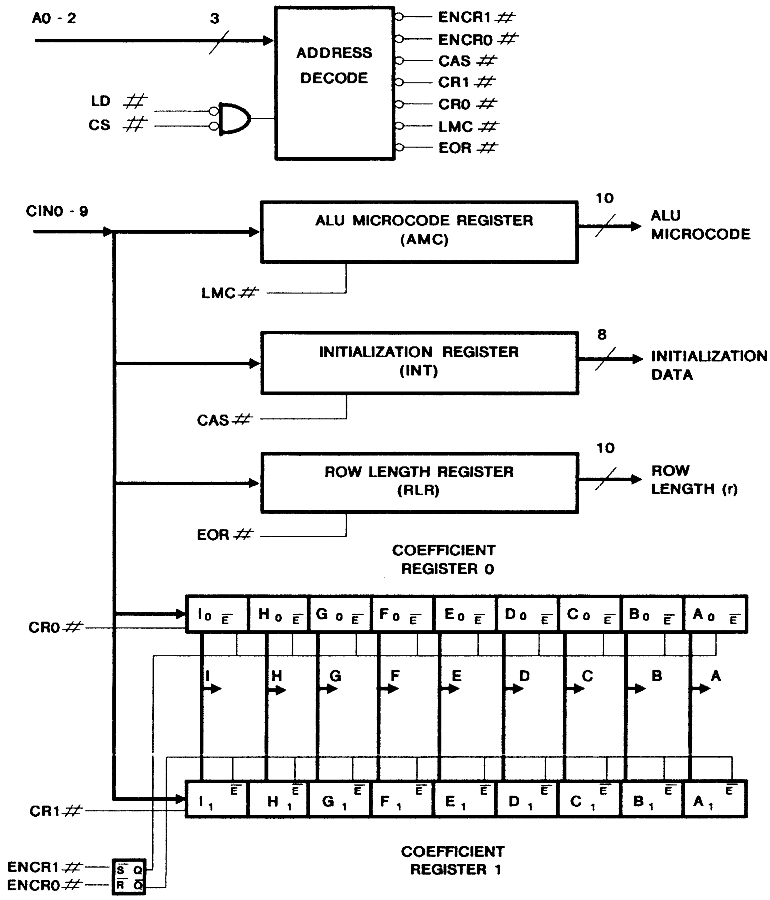

FIGURE 1. CONTROL LOGIC BLOCK DIAGRAM

Initialization Register

The initialization register is used to appropriately configure the convolver for a particular application. It is loaded through the use of the CIN0-7 bus along with the CS# and LD# inputs. Bit 0 defines the type of cascade mode to be used; Bits 1 and 2 select the number of delays to be included in the input pixel data path; Bits 3 and 4 define the input and coefficient data format; Bits 5 and 6 determine the type of rounding to occur on the DOUT0-19 bus; Bits 7 and 8 define the shift applied to the cascade input data. The complete definition of the initialization register bits is given in Table 3.

TABLE 3. INITIALIZATION REGISTER DEFINITION

INITIALIZATION REGISTER		
BIT 0		**FUNCTION = CASCADE MODE**
0		Multiplier input from internal row buffers
1		Multiplier input from external buffers
2	**BIT 1**	**FUNCTION = INPUT DATA DELAY**
0	0	No data delay registers used
0	1	One data delay register used
1	0	Two data delay registers used
1	1	Three data delay registers used
BIT 3		**FUNCTION = INPUT DATA FORMAT**
0		Unsigned integer format
1		Two's complement format
BIT 4		**FUNCTION = COEFFICIENT DATA FORMAT**
0		Unsigned integer format
1		Two's complement format
6	**BIT 5**	**FUNCTION = OUTPUT ROUNDING**
0	0	No Rounding
0	1	Round to 16 bits (i.e. DOUT19-4)
1	0	Round to 8 bits (i.e. DOUT19-12)
1	1	Not Valid
8	**BIT 7**	**FUNCTION = CASI0-15 INPUT SHIFT**
0	0	No Shift
0	1	Shift CASI0-15 left two
1	0	Shift CASI0-15 left four
1	1	Shift CASIO-15 left eight

Row Length Register

The row length register is used to store the programmed number of delays for the internal row buffers. The programmed delay is set equal to the row length (r) of the input image. The input pixel data is stored in the row buffers to allow corresponding pixels of adjacent rows to be synchronously sent to the mutiplier array for the convolution operation. The row length register is programmable with values from 0 to 1023, with 0 defined as a row length of 1024. Row lengths of 1 or 2 lead to meaningless results for a 3 x 3 kernel convolution, while a row length of 3 defines a 1 x 9 filter (See Operation section). The Row Length register is written through the use of A0-2, CS# and LD#. Once the row length register has been loaded, the convolver must be reset before a new row length can be entered, or else the new value will be ignored. After RESET# returns high, the user has 1024 cycles of CLK to load the Row Length Register. After 1024 CLK cycles, the Row Length Register is automatically set to 0 (row length = 1024) and further writes to this register are ignored.

Coefficient Registers (CREG0, CREG1)

The control logic contains two coefficient register banks, CREG0 and CREG1. Each of these register banks is capable of storing nine 8-bit filter coefficient values (3 x 3 Kernel). The output of the registers are connected to the coefficient input of the corresponding multiplier in the 3 x 3 multiplier array (designated A through I). The register bank to be used for the convolution is selectable by writing to the appropriate address (See address decoder). All registers in a given bank are enabled simultaneously, and one of the banks is always active.

For most applications, only one of the register banks is necessary. The user can simply load CREG0 after power up, and use it for the entire convolution operation. (CREG0 is the default register). The alternate register bank allows the user to maintain two sets of filter coefficients and switch between them in real time. The coefficient masks are loaded via the CIN bus by using A0-2, CS# and LD#. The selection of the particular register bank to be used in processing is also done by writing to the appropriate address (See address decoder). For example, if CREG0 is being used to provide coefficients to the multipliers, CREG1 can be updated at a low rate by an external processor; then, at the proper time, CREG1 can be selected, so that the new coefficient mask is used to process the data. Thus, no clock cycles have been lost when changing between alternate 3 x 3 filter kernels.

The nine coefficients must be loaded sequentially over the CIN0-7 bus from A to I. The address of CREG0 or CREG1 is placed on A0-2, and then the nine coefficients are written to the corresponding coefficient register one at a time by using the CS# and LD# inputs.

Address Decoder

The address decoder (See Figure 1) is used for writing to the control logic of the HSP48908. Loading an internal register is done by selecting the destination register with the A0-2 address lines, placing the data on CIN0-9, and asserting the CS# and LD# control lines. When either CS# or LD# goes high, the data on the CIN0-9 lines is latched into the addressed register. The address map for the A0-2 bus is shown in Table 4.

While loading of the control logic registers is asynchronous to CLK, the target register in the control logic is being read synchronous to the internal clock. Therefore, care must be taken when modifying the convolver setup parameters during processing to avoid changing the contents of the registers near a rising edge of CLK. The required setup time relative to CLK is given by the specification TLCS. For example, in order to change the active coefficient register from CREG0 to CREG1 during an active convolution operation, a write will be performed to the address for selecting CREG1 for internal processing (A2-0=110). In order to provide proper uninterrupted operation, LD# should be deasserted at least TLCS prior to the next rising edge of CLK. Failure to meet this setup time may result in unpredictable results on the output of the convolver for one clock cycle. Keep in mind that this requirement applies only to the case where changes are being made in the control logic during an active convolution operation. In a typical convolver configuration routine, this specification would not be applicable.

TABLE 4. ADDRESS MAP

CONTROL LOGIC ADDRESS MAP	
A2-0	**Function**
000	Load Row Length Register (RLR)
001	Load ALU Microcode Register (AMC)
010	Load Coefficient Register 0 (CREG0)
011	Load Coefficient Register 1 (CREG1)
100	Load Initialization Register (INT)
101	Select CREG0 for Internal Processing
110	Select CREG1 for Internal Processing
111	No Operation

Cascade I/O

Cascade Input

The cascade input lines (CASI0-15) have two primary functions. The first is used to allow convolutions with kernel sizes larger than 3 x 3. This can be implemented by connecting the DOUT bus of one convolver to the cascade inputs of another. The second function is for convolution on images wider than 1024 pixels. This type of operation can be implemented by using external row buffers to supply the pixel input data to the CASI0-15 inputs. The cascade input functions are determined by Initialization Register bit 0. When this bit is set to a '0', the cascade input data is added to the convolver output. In this manner, multiple convolvers can be used to implement larger kernel convolution. When Initialization Register bit 0 is a '1', the data on CASI0-15 is divided into two 8-bit portions and is sent to the 3 x 3 multiplier array (Refer to Block Diagram). This mode of operation allows the use of external row buffers for convolution of images with row sizes larger than 1024. Examples of these configurations are given in the Operations section of this specification.

The data on the cascade inputs (CASI0-15) can also be left shifted by 0, 2, 4, or 8 bits. The amount of shift is determined by bits 7 and 8 of the Initialization Register (See Table 3). CASI0-15 is shifted by the specified number of bits and is added to the 20-bit output DOUT 0-19. The shifting function provides a method for cascading multiple HSP48908s and allowing a selectable amount of output growth while maximizing the resolution of the convolver result.

The cascade inputs can also be used as a simple way to add an offset to the convolved image. Bit 0 of the configuration register would be set to '0', and the desired offset placed on the CASI0-15 inputs. While multiple offets can be used and changed during the convolution operation, note that the required data setup and hold times with respect to CLK (TDS and TDH) must be met.

Cascade Output

The cascade output lines (CASO0-7) are outputs from the second row buffer. Data at these outputs is the input pixel data delayed by two times the preprogrammed value in the row length register. The cascade outputs are used to cascade multiple convolvers by connecting the cascade outputs of one device to the data inputs of another (See Operation section).

Control Signals

HOLD

The HOLD control input provides the ability to disable internal clock and stop all operations temporarily. HOLD is sampled on the rising edge of CLK and takes effect during the following clock cycle (Refer to Figure 2). This signal can be used to momentarily ignore data at the input of the convolver while maintaining its current output data and operational state.

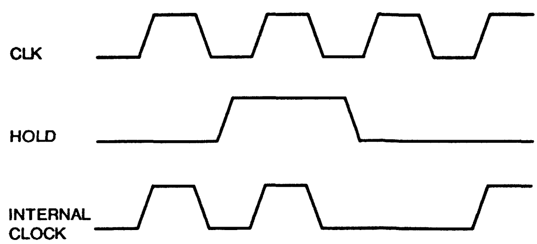

FIGURE 2. HOLD OPERATION

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RESET#

The RESET# signal initializes all internal flip flops and registers in the HSP48908. It is an asynchronous signal, and the convolver will remain in the reset state as long as RESET# is asserted. On reset, all internal registers are set to zero or their default values, and all outputs are forced low. Following a reset, the default values in the internal registers will define the following mode of operation: internal row buffers used, line length = 1024, no input data delay, logical A operation: output of ALU = A input (DIN0-7) output rounding and unsigned input data format.

The convolver can be reset at any time, but must be reset before updating the Row Length register in order to provide proper operation. After RESET# returns high, the user has 1024 cycles of CLK to load the Row Length Register. After 1024 CLK cycles, the Row Length Register is automatically set to 0 (row length = 1024) and further writes to this register are ignored.

FRAME#

This FRAME# input initializes all internal flip flops and registers except for the coefficient, ALU, ALU microcode, row length, and initialization registers. It is used to reset the convolver between video frames and eliminates the need to re-initialize the entire convolver or reload the coefficients. FRAME# is an asynchronous input and may occur at any time. However, it must be deasserted at least TFS ns prior to the rising clock edge that is to begin operation for the next frame. While FRAME# is asserted, the registers and flip-flops will remain in the reset state.

Operation

The HSP48908 has three basic modes of operation: single chip mode, operation with external row buffers and multiple devices cascaded together for larger convolution kernels and/or longer row lengths. The mode of operation is defined by the contents of the initialization register, and can be modified at any time by a microprocessor or other external means.

Single Chip Mode

A single HSP48908 can be used to perform 3 x 3 convolution on 8-bit image data with row lengths up to 1024. A block diagram of this configuration is shown in Figure 3. In this mode of operation, the image data is input into the DIN0-7 bus in a raster scan order starting with the upper left pixel. To perform the convolution operation, a group of nine image pixels is multiplied by the 3 x 3 array of filter coefficients and their products are summed and sent to the output. For the example in Figure 3, the pixel value in the output image at location (m, n) is given by:

$$
\begin{aligned}
P_{OUT(m,n)} \quad & (A \times P_{m-1,n-1}) + (B \times P_{m-1,n}) + (C \times P_{m-1,n+1}) \\
& + (D \times P_{m,n-1}) + (E \times P_{m,n}) + (F \times P_{m,n+1}) \\
& + (G \times P_{m+1,n-1}) + (H \times P_{m+1,n}) + (I \times P_{m+1,n+1})
\end{aligned}
$$

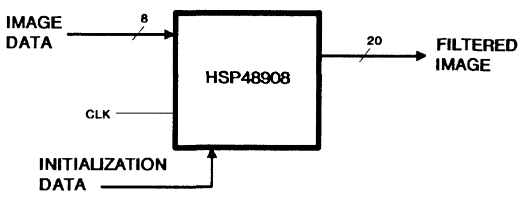
This process is continually repeated until the last pixel of the last row of the image has been input. It can then start again with the first row of the next frame. The FRAME# pin is used to clear the row buffers, multiplier input latches and DOUT0-19 registers between frames.

The setup for single chip operation is straightforward. After reset, the convolver is configured for row lengths of 1024 pixels, no input data delay, no ALU pixel point operations, no output rounding, and an unsigned input format. The user can change this default setup by loading new values into the ALU microcode, initialization and row length registers. RESET# also clears the coefficient registers and CREG0 is selected for internal processing. The user can now load the coefficients one at a time from A to I via the CIN0-7 inputs and the LD# and CS# control lines.

Multiple filter kernels can also be used on the same image data using the dual coefficient registers CREG0 and CREG1. This type of filtering is used when the characteristics of the input pixel data change over the image in such a way that no single filter produces satisfactory results for the entire image. In order to filter such an image, the characteristics of the filter itself must change while the image is being processed. The HSP48908 can perform this function with the use of an external processor. The processor is used to calculate the required new filter coefficients, loads them into the coefficient register not in use, and selects the newly loaded coefficient register at the proper time. The first coefficient register can then be loaded with new coefficients in preparation for the next change. This can be carried out with no interruption in processing, provided that the new register is selected synchronous to the convolver CLK signal.

The HSP48908 can also operate as a one dimensional 9 tap FIR filter by programming the row buffer length register with a value of 3 and setting the initialization register bit 0 to a '0'. This configuration will provide for nine sequential input values in the input to be multiplied by the coefficient values in the selected coefficient register and provide the proper filtered output. The equation for the output then becomes:

$$
\begin{aligned}
D_{OUTn} = \; & A \times D_{n-8} + B \times D_{n-7} + C \times D_{n-6} + D \times D_{n-5} \\
& + E \times D_{n-4} + F \times D_{n-3} + G \times D_{n-2} + H \times D_{n-1} \\
& + I \times D_n
\end{aligned}
$$



FILTER KERNEL	IMAGE DATA		
A B C	$P_{m-1,n-1}$	$P_{m-1,n}$	$P_{m-1,n+1}$
D E F	$P_{m,n-1}$	$P_{m,n}$	$P_{m,n+1}$
G H I	$P_{m+1,n-1}$	$P_{m+1,n}$	$P_{m+1,n+1}$

FIGURE 3. 3 x 3 KERNEL ON AN 8-BIT, 1024 x N IMAGE

Use Of External Row Buffers

External row buffers may be used when frames with row sizes larger than 1024 pixels are desired. To use the HSP48908 in this mode, the cascade mode control bit (bit 0) of the initialization register is set to '1' to allow the data on the cascade inputs CASI0-15 to go to the multiplier array. The inputs of one external row buffer (such as the HSP9500) are connected to the input data in parallel with the DIN0-7 lines of the convolver; and its outputs are connected to the CASI0-7 inputs (See Figure 4). A second external row buffer is connected between the outputs of the first row buffer and the CASI8-15 inputs of the convolver. The convolution operation can then be performed by the HSP48908 in the same manner as the single chip mode. The row length in this configuration is limited only by the maximum length of the external row buffers. Note that when using the convolver in this configuration, the programmable input data delays and ALU will only operate on the data entering the DIN0-7 inputs (i.e. the bottom row of the 3 x 3 sum of products). If higher order filters or pixel point operations are required when using external row buffers, these functions must be implemented externally by the user.

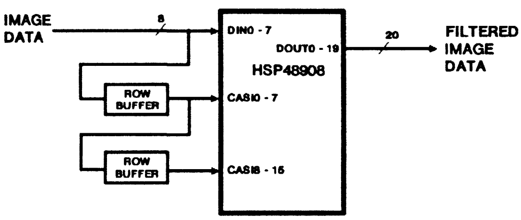


FIGURE 4. USING EXTERNAL ROW BUFFERS WITH THE HSP48908

Cascading Multiple HSP48908's

Multiple HSP48908s are capable of being cascaded to perform convolution on images with row lengths longer than 1024 pixels and with kernel sizes larger than 3 x 3. Figure 5 illustrates the use of two HSP48908s to perform a 3 x 3 kernel convolution on a 2K x N frame. In this case, the cascade mode control bit (Bit 0) of both initialization registers are set to a '0'. The loading of the coefficients is accomplished just as before. However, the 3 x 3 mask is divided into two portions for proper convolution output as follows: Convolver #1 = DEF000GHI and Convolver #2 = ABC000000.

3 x 3 FILTER KERNEL	COEFFICIENT MASKS	
	CONVOLVER #1	CONVOLVER #2
ABC DEF GHI	DEF 000 GHI	ABC 000 000

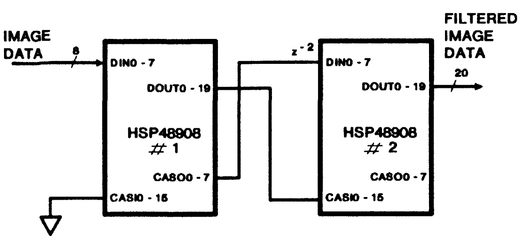
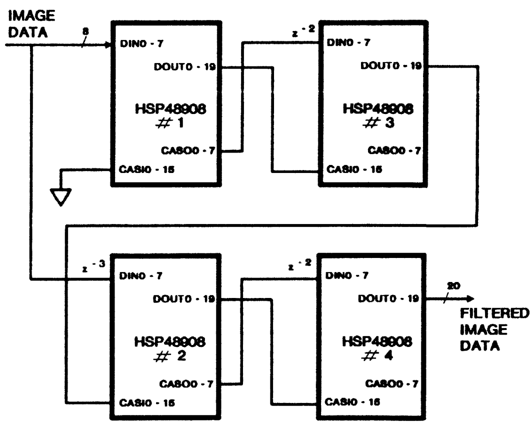


FIGURE 5. 3 x 3 KERNEL CONVOLUTION ON A 2K x N IMAGE

The same configuration can be used to perform 3 x 5 convolution on a 1K x N frame simply by setting up the coefficients of the convolvers to implement the 3 x 5 mask as indicated below:

3 x 5 FILTER KERNEL	COEFFICIENT MASKS	
	CONVOLVER #1	CONVOLVER #2
ABC DEF GHI JKL MNO	GHI JKL MNO	ABC DEF 000

In addition to larger frames, larger kernels can also be addressed through cascadability. An example of the configuration for a 5 x 5 kernel convolution on a 1K x N frame is shown in Figure 6. Note that in this configuration, convolver #2 incorporates a 3 clock cycle delay (z -3) and convolvers 3 and 4 incorporate 2 clock cycle delays (z -2) at their pixel inputs. These delays are required to ensure proper data alignment in the final sum of products output of the cascaded convolvers. The number of delays required at the pixel input is programmable through the use of bits 1 and 2 of the initialization register (Refer to Table 3).



5 X 5 FILTER KERNEL	CONVOLVER COEFFICIENT MASKS	
ABCDE FGHIJ KLMNO PQRST UVWXY	0KL 0PQ 0UV MNO RST WXY	0AB 0FG 000 CDE HIJ 000

FIGURE 6. 5 x 5 KERNEL CONVOLUTION ON A 1K x N IMAGE

In any of the cascade configurations, only 16 bits of the 20-bit output (DOUT0-19) can be connected to the 16 cascade inputs (CASI0-15) of another convolver. Which 16 bits are chosen depends upon the amount of growth expected at the convolver output. The amount of growth is dependent on the input pixel data and the coefficients selected for the convolution operation. The maximum possible growth is calculated in advance by the user, and the convolvers are set up to appropriately shift the cascade input data through the use of bits 7 and 8 of the initialization register (See Cascade I/O). Refering to Figure 6, if the maximum growth out of convolver #1 extends into bit 16 or 17, then DOUT2-17 are connected to the cascade inputs of convolver #3, which is programmed to shift the input data left by two bits. Likewise, if the data out of convolver #3 grows into bit 18 or 19, then DOUT4-19 are connected to the CASI0-15 inputs of convolver #2, which is programmed to shift the input left by 4 bits.

Cascading For Row Sizes Larger Than 1024

Combining large images with large kernels is accomplished by implementing external row buffers, external data delay registers and external adders. Figure 7 illustrates a circuit for implementation of a 5 x 5 convolution on a 2K x N image. The 5 x 5 coefficient mask is again distributed among the four HSP48908's. The width of the DOUT path to be used in this case is dependent on the amount of resolution required and the amount of growth expected at the output.

Frame Rate

The total time to process an image is given by the formula:

$T = R \times C / F$

where:

T = time to process a frame
R = number of rows in the image
C = number of pixels in a row
F = clock rate of the HSP48908

Note that the size of the kernel does not enter into the equation. Convolvers cascaded for larger kernels or larger frame sizes, as in the examples shown, process the image in the same amount of time as a single HSP48908 convolving the image with a 3 x 3 kernel. Therfore, there is no performance degradation when cascading multiple HSP48908s.

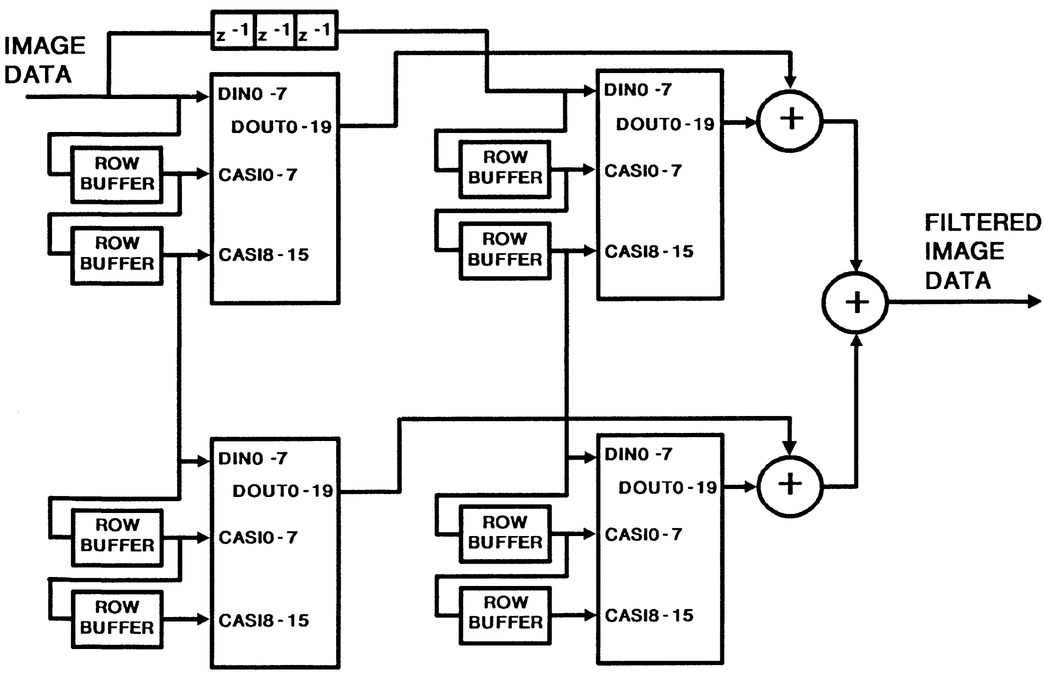


FIGURE 7. 5 x 5 KERNEL CONVOLUTION ON A 2K x N IMAGE

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output or I/O Voltage Applied .... GND -0.5V to V_{CC} +0.5V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation @ 70°C .... 1.67W (MQFP), 2.46W (PLCC), 3.04W (PGA)
Thermal Impedance Junction To Case (θ_{jc}) .... 10.0°C/W (PLCC), 7.7°C/W (PGA)
Thermal Impedance Junction To Ambient (θ_{ja}) .... 48°C/W (MQFP), 32.5°C/W (PLCC), 35.0°C/W (PGA)
Gate Count .... 190,000 Transistors
Maximum Junction Temperature (T_J) .... 150°C (PLCC, MQFP), 175°C (PGA)
Lead Temperature (Soldering, Ten Seconds) .... +300°C
ESD Classification .... Class 1

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.75V to +5.25V
Operating Temperature Range .... 0°C to +70°C

D.C. Electrical Specifications (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.0	-	V	V_{CC} = 5.25V
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = 4.75V
High Level Clock Input	V_{IHC}	3.0	-	V	V_{CC} = 5.25V
Low Level Clock Input	V_{ILC}	-	0.8	V	V_{CC} = 4.75V
Output HIGH Voltage	V_{OH}	2.6	-	V	I_{OH} = -400µA, V_{CC} = 4.75V
Output LOW Voltage	V_{OL}	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.75V
Input Leakage Current	I_I	-10	10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V
I/O Leakage Current	I_O	-10	10	µA	V_{OUT} = V_{CC} or GND
Standby Power Supply Current	I_{CCSB}	-	500	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Outputs Open
Operating Power Supply Current	I_{CCOP}	-	140	mA	f = 20MHz, V_{IN} = V_{CC} or GND Note 1

Capacitance (T_A = +25°C, Note 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_{IN}	-	10	pF	FREQ = 1MHz, V_{CC} = Open, all measurements are referenced to device ground.
Output Capacitance	C_O	-	12	pF	

NOTES: 1. Power supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 7.0mA/MHz.
2. Not tested, but characterized at initial design and at major process/design changes.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

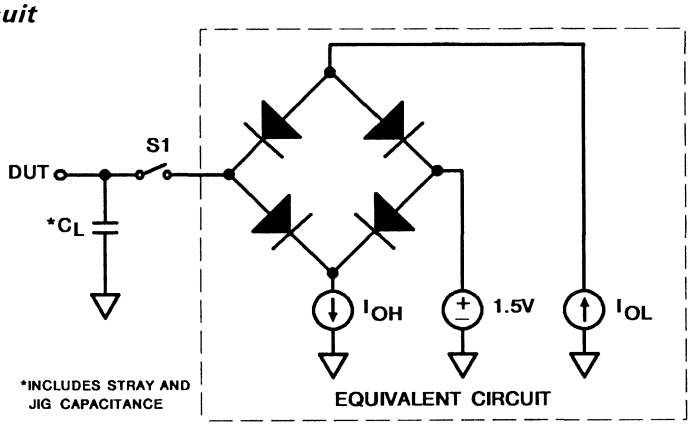
A.C. Electrical Specifications (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	-32 (32MHz)		-20 (20MHz)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Clock Period	T_{CYCLE}	31	-	50	-	ns	
Clock Pulse Width High	T_{PWH}	12	-	20	-	ns	
Clock Pulse Width Low	T_{PWL}	13	-	20	-	ns	
Data Input Setup Time	T_{DS}	13	-	14	-	ns	
Data Input Hold Time	T_{DH}	0	-	0	-	ns	
Clock to Data Out	T_{OUT}	-	16	-	22	ns	
Address Setup Time	T_{AS}	13	-	13	-	ns	
Address Hold Time	T_{AH}	0	-	0	-	ns	
Configuration Data Setup Time	T_{CDS}	14	-	16	-	ns	
Configuration Data Hold Time	T_{CDH}	0	-	0	-	ns	
LD# Pulse Width	T_{LPW}	12	-	20	-	ns	
LD# Setup Time	T_{LCS}	25	-	30	-	ns	Note 1
CIN0-7 Setup to CLK	T_{CS}	14	-	16	-	ns	
CS# Setup To LD#	T_{CSS}	0	-	0	-	ns	
CIN0-7 Hold Time From CLK	T_{CH}	0	-	0	-	ns	
CS# Hold From LD#	T_{CSH}	0	-	0	-	ns	
RESET# Pulse Width	T_{RPW}	31	-	50	-	ns	
FRAME# Setup To Clock	T_{FS}	21	-	25	-	ns	Note 2
FRAME# Pulse Width	T_{FPW}	31	-	50	-	ns	
EALU Setup Time	T_{ES}	12	-	14	-	ns	
EALU Hold Time	T_{EH}	0	-	0	-	ns	
HOLD Setup Time	T_{HS}	11	-	12	-	ns	
HOLD Hold Time	T_{HH}	1	-	1	-	ns	
Output Enable Time	T_{EN}	-	16	-	22	ns	Note 3
Output Disable Time	T_{OZ}	-	28	-	32	ns	Note 5
Output Rise Time	T_R	-	6	-	6	ns	From 0.8 to 2.0 V Note 5
Output Fall Time	T_F	-	6	-	6	ns	From 2.0 to 0.8 V Note 5

NOTES:
1. This specification applies only to the case where the HSP48908 is being written to during an active convolution cycle. It must be met in order to acheive predictable results at the next rising clock edge. In most applications, the configuration data and coefficients are loaded asynchronously and the T_{LCS} specification may be disregarded.
2. While FRAME# is an asynchronous signal, it must be deasserted a minimum of T_{FS} ns prior to the rising clock edge which is to begin loading pixel data for a new frame.
3. Transition is measured at ± 200 mV from steady state voltage with loading as specified in test load circuit with C_L = 40pF.
4. A.C. Testing is performed as follows: Input levels (CLK Input) 4.0 and 0V, Input levels (All other Inputs) 0V and 3.0V, Timing reference levels (CLK) = 2.0V, (Others) = 1.5V, Output load per test load circuit with C_L = 40pF. Output transition is measured at $V_{OH} \geq$ 1.5V and $V_{OL} \leq$ 1.5V.
5. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

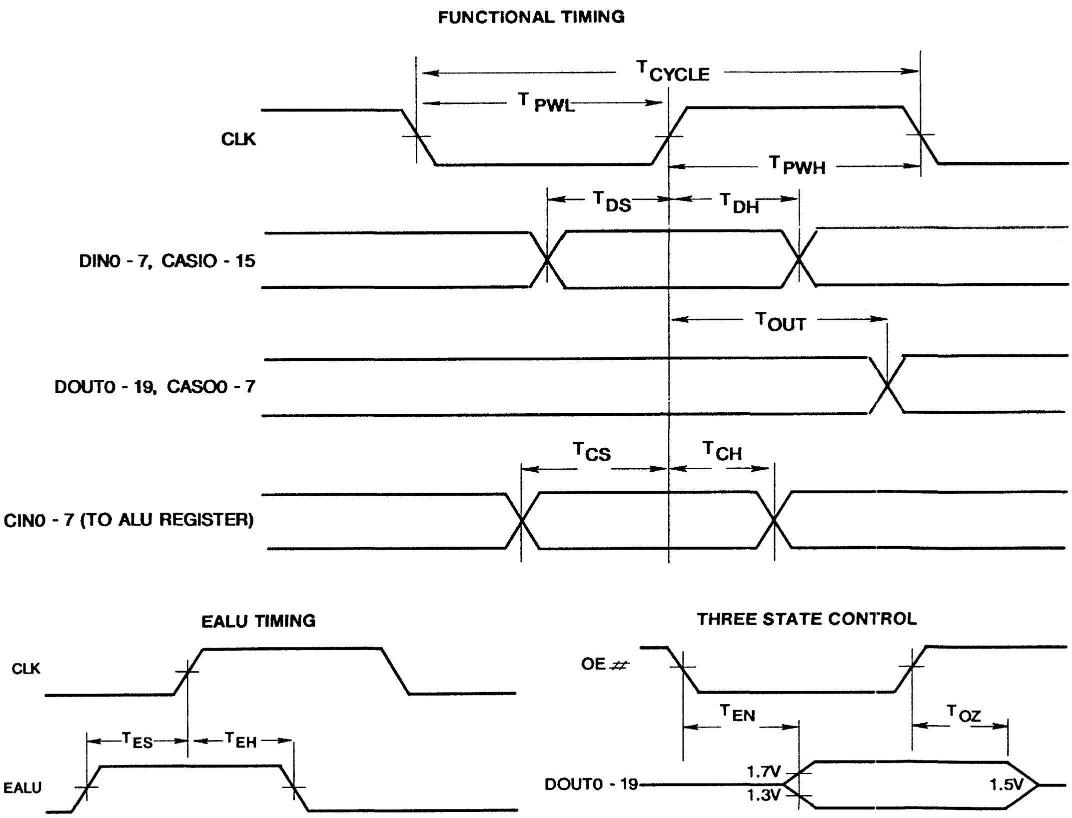
CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Test Load Circuit



Switch S1 Open for I_{CCSB} and I_{CCOP} Tests

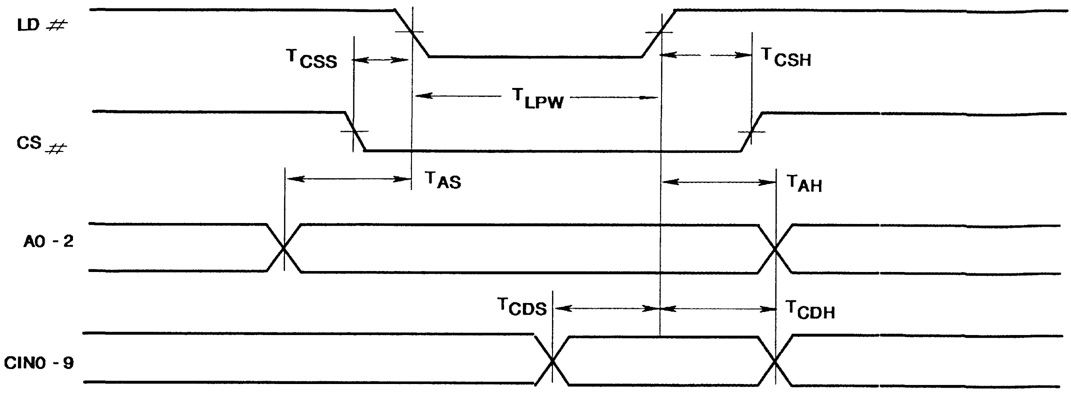
Timing Waveforms



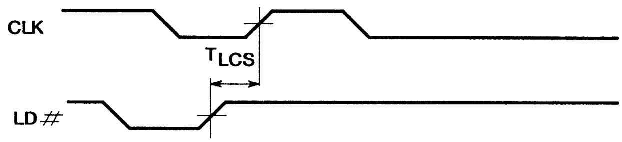
4 VIDEO PROCESSING

Timing Waveforms (Continued)

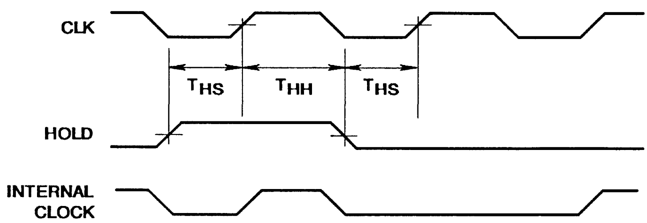
CONFIGURATION TIMING



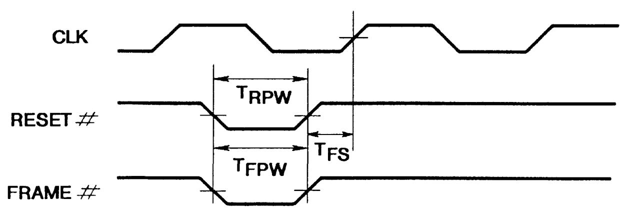
SYNCHRONOUS LOAD TIMING



HOLD TIMING



FRAME#/RESET# TIMING



HSP48908/883

January 1994

Two Dimensional Convolver

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Single Chip 3 x 3 Kernel Convolution
- Programmable On-Chip Row Buffers
- DC to 27MHz Clock Rate
- Cascadable for Larger Kernels and Images
- On-Chip 8-Bit ALU
- Dual Coefficient Mask Registers, Switchable in a Single Clock Cycle
- 8-Bit Signed or Unsigned Input and Coefficient Data
- 20-Bit Extended Precision Output
- Standard μP Interface

Applications

- Image Filtering
- Edge Detection
- Adaptive Filtering
- Real Time Video Filters

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HSP48908GM-20/883	-55°C to +125°C	84 Lead PGA
HSP48908GM-27/883	-55°C to +125°C	84 Lead PGA

Description

The Harris HSP48908/883 is a high speed Two Dimensional Convolver which provides a single chip implementation of a video data rate 3 x 3 kernel convolution on two dimensional data. It eliminates the need for external data storage through the use of the on-chip row buffers which are programmable for row lengths up to 1024 pixels.

There are internal register banks for storing two independent 3 x 3 filter kernels, thus facilitating the implementation of adaptive filters and multiple filter operations on the same data. The pixel data path also includes an on-chip ALU for performing real-time arithmetic and logical pixel point operations.

Data is provided to the HSP48908/883 in a raster scan non-interlaced fashion, and is internally buffered on images up to 1024 pixels wide for the 3 x 3 convolution operation. Images with larger rows and convolution with larger kernel sizes can be accommodated by using external row buffers and/or multiple HSP48908/883s. Coefficient and pixel input data are 8-bit signed or unsigned integers, and the 20-bit convolver output guarantees no overflow for kernel sizes up to 4 x 4. Larger kernel sizes can be implemented however, since the filter coefficients will normally be less than their maximum 8-bit values.

The HSP48908/883 is manufactured using an advanced CMOS process, and is a low power fully static design. The configuration of the device is controlled through a standard microprocessor interface and all inputs/outputs are TTL compatible.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

Pinout

HSP48908/883 (PGA)
TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L
11	CASO6	DOUT0	DOUT1	GND	DOUT5	DOUT6	DOUT8	DOUT10	DOUT12	DOUT13	DOUT15
10	CASO4	CASO5	CASO7	DOUT2	DOUT4	DOUT9	GND	DOUT11	DOUT14	GND	DOUT17
9	CASO3	GND			DOUT3	DOUT7	V_{CC}			DOUT16	DOUT18
8	CASO1	CASO2								DOUT19	GND
7	OE #	GND	V_{CC}						CASI1	FRAME #	CASI0
6	DIN1	CASO0	DIN0						CASI2	V_{CC}	RESET #
5	DIN2	DIN3	DIN4						CASI5	CASI4	CASI3
4	DIN5	DIN6								CASI7	CASI6
3	DIN7	CIN1			CIN9	HOLD	LD #			CASI10	CASI8
2	CIN0	CIN3	CIN4	CIN7	GND	V_{CC}	A2	EALU	CASI13	CASI11	CASI9
1	CIN2	CIN5	CIN6	CIN8	CLK	A1	CS #	A0	CASI15	CASI14	CASI12

84 PIN PGA

TOP VIEW

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output or I/O Voltage Applied .... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering 10 sec) .... +300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic PGA Package	35.0°C/W	7.7°C/W

Maximum Package Power Dissipation at +125°C
Ceramic PGA Package 1.45W
Gate Count.............................. 190,000 Transistors

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range ....-55°C to +125°C
Operating Voltage Range .... +4.5V to +5.5V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical 1 Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	2.2	-	V
Logical 0 Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.8	V
Clock Input High	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400mA V_{CC} = 4.5V (Note 1)	1, 2, 3	$-55^oC \le T_A \le +125^oC$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC} = 4.5V (Note 1)	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.4	V
Input Leakage Current	I_I	$V_{IN} = V_{CC}$ or GND V_{CC} = 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-10	+10	µA
Output or I/O Leakage Current	I_O	$V_{OUT} = V_{CC}$ or GND V_{CC} = 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-10	+10	µA
Standby Power Supply Current	I_{CCSB}	$V_{IN} = V_{CC}$ or GND V_{CC} = 5.5V Outputs Open (Note 4)	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 20.0MHz V_{CC} = 5.5V Outputs Open, (Notes 2, 4)	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	160.0	mA
Functional Test	FT	(Notes 3, 4)	7, 8	$-55^oC \le T_A \le +125^oC$	-	-	-

NOTES:
1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 8.0mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, $V_{OH} \ge$ 1.5V, $V_{OL} \le$ 1.5V, V_{IHC} = 3.4V, and V_{ILC} = 0.4V.
4. Loading is a specified in the test load circuit with C_L = 40pF.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C (Note 4)

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS -27 (27MHz) MIN	LIMITS -27 (27MHz) MAX	LIMITS -20 (20MHz) MIN	LIMITS -20 (20MHz) MAX	UNITS
Clock Period	T_{CYCLE}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	37	-	50	-	ns
Clock Pulse Width High	T_{PWH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	20	-	ns
Clock Pulse Width Low	T_{PWL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	20	-	ns
Data Input Setup Time	T_{DS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	16	-	17	-	ns
Data Input Hold Time	T_{DH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Clock to Data Out	T_{OUT}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	19	-	28	ns
Address Setup Time	T_{AS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	15	-	ns
Address Hold Time	T_{AH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Configuration Data Setup Time	T_{CDS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	17	-	20	-	ns
Configuration Data Hold Time	T_{CDH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
LD# Pulse Width	T_{LPW}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	20	-	ns
LD# Setup Time	T_{LCS}	Note 1	9, 10, 11	$-55^oC \le T_A \le +125^oC$	30	-	37	-	ns
CIN7-0 Setup to CLK	T_{CS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	17	-	20	-	ns
CIN7-0 Hold from CLK	T_{CH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
CS# Setup to LD#	T_{CSS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
CS# Hold from LD#	T_{CSH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
RESET# Pulse Width	T_{RPW}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	37	-	50	-	ns
FRAME# Setup to CLK	T_{FS}	Note 2	9, 10, 11	$-55^oC \le T_A \le +125^oC$	25	-	30	-	ns
FRAME# Pulse Width	T_{FPW}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	37	-	50	-	ns
EALU Setup Time	T_{ES}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	17	-	ns
EALU Hold Time	T_{EH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
HOLD Setup Time	T_{HS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	13	-	14	-	ns
HOLD Hold Time	T_{HH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	2	-	2	-	ns
Output Enable Time	T_{EN}	Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	19	-	28	ns

NOTES:
1. This specification applies only to the case where the HSP48908/883 is being written to during an active convolution cycle. It must be met in order to achieve predictable results at the next rising clock edge. In most applications, the configuration data and coefficients are loaded asynchronously and the T_{LCS} specification may be disregarded.
2. While FRAME# is an asynchronous signal, it must be deasserted a minimum of T_{FS} ns prior to the rising clock edge which is to begin loading pixel data for a new frame.
3. Transition is measured at ±200mV from steady state voltage with loading as specified in test load circuit with C_L = 40pF.
4. A.C. Testing is performed as follows: Input levels (CLK Input) 4.0V and 0V, Input levels (All other Inputs) 0V and 3.0V, Timing Reference Levels (CLK) = 2.0V, (Others) = 1.5V. Output load per test load circuit with C_L = 40pF. Output transition is measured at $V_{OH} \ge$ 1.5V and $V_{OL} \le$ 1.5V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS -27 MIN	LIMITS -27 MAX	LIMITS -20 MIN	LIMITS -20 MAX	UNITS
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	10	-	10	pF
Output Capacitance	C_O	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	12	-	12	pF
Output Disable Time	T_{OZ}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	35	-	40	ns
Output Rise Time	T_R	From 0.8V to 2.0V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	6	-	6	ns
Output Fall Time	T_F	From 2.0V to 0.8V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	6	-	6	ns

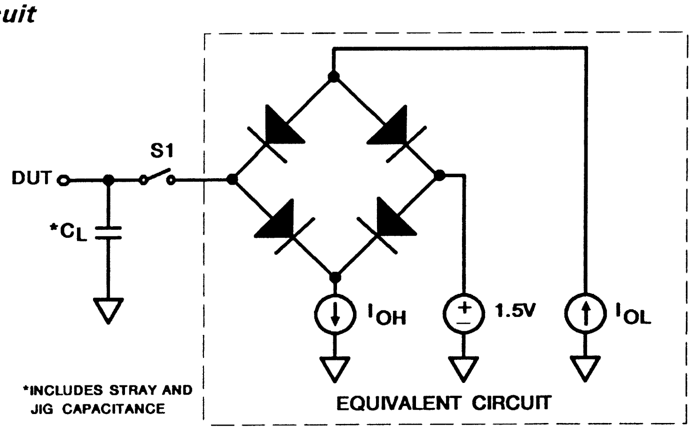
NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Test Load Circuit



Switch S1 Open for I_{CCSB} and I_{CCOP} Tests

4 VIDEO PROCESSING

Burn-In Circuit

	A	B	C	D	E	F	G	H	J	K	L
11	CASO6	DOUT0	DOUT1	GND	DOUT5	DOUT6	DOUT8	DOUT10	DOUT12	DOUT13	DOUT15
10	CASO4	CASO5	CASO7	DOUT2	DOUT4	DOUT9	GND	DOUT11	DOUT14	GND	DOUT17
9	CASO3	GND			DOUT3	DOUT7	V_{CC}			DOUT16	DOUT18
8	CASO1	CASO2								DOUT19	GND
7	OE #	GND	V_{CC}						CASI1	FRAME #	CASI0
6	DIN1	CASO0	DIN0			84 PIN PGA TOP VIEW			CASI2	V_{CC}	RESET #
5	DIN2	DIN3	DIN4						CASI5	CASI4	CASI3
4	DIN5	DIN6								CASI7	CASI6
3	DIN7	CIN1			CIN9	HOLD	LD #			CASI10	CASI8
2	CIN0	CIN3	CIN4	CIN7	GND	V_{CC}	A2	EALU	CASI13	CASI11	CASI9
1	CIN2	CIN5	CIN6	CIN8	CLK	A1	CS #	A0	CASI15	CASI14	CASI12

PGA BURN-IN SCHEMATIC

PIN NAME	PGA PIN	BURN-IN SIGNAL
CIN2	A1	F13
CIN0	A2	F12
DIN7	A3	F7
DIN5	A4	F5
DIN2	A5	F2
DIN1	A6	F1
OE	A7	F10
CASO.1	A8	$V_{CC}/2$
CASO.3	A9	$V_{CC}/2$
CASO.4	A10	$V_{CC}/2$
CASO.6	A11	$V_{CC}/2$
CIN5	B1	F12
CIN3	B2	F13
CIN1	B3	F12
DIN6	B4	F6
DIN3	B5	F3
CASO.0	B6	$V_{CC}/2$
GND	B7	GND
CASO.2	B8	$V_{CC}/2$
GND	B9	GND
CASO.5	B10	$V_{CC}/2$
POUT0	B11	$V_{CC}/2$
CIN6	C1	F13
CIN4	C2	F13
DIN4	C5	F4
DIN0	C6	F0
V_{CC}	C7	V_{CC}
CASO.7	C10	$V_{CC}/2$

PIN NAME	PGA PIN	BURN-IN SIGNAL
POUT1	C11	$V_{CC}/2$
CIN8	D1	F14
CIN7	D2	F12
POUT2	D10	$V_{CC}/2$
GND	D11	GND
CLK	E1	F0
GND	E2	GND
CIN9	E3	F14
POUT3	E9	$V_{CC}/2$
POUT4	E10	$V_{CC}/2$
POUT5	E11	$V_{CC}/2$
A1	F1	F13
V_{CC}	F2	V_{CC}
HOLD	F3	F14
POUT7	F9	$V_{CC}/2$
POUT9	F10	$V_{CC}/2$
POUT6	F11	$V_{CC}/2$
CS	G1	F12
A2	G2	F14
LOAD	G3	F11
V_{CC}	G9	V_{CC}
GND	G10	GND
POUT8	G11	$V_{CC}/2$
A0	H1	F12
EALU	H2	F8
POUT11	H10	$V_{CC}/2$
POUT10	H11	$V_{CC}/2$
CASI.15	J1	F7

PIN NAME	PGA PIN	BURN-IN SIGNAL
CASI.13	J2	F5
CASI.5	J5	F5
CASI.2	J6	F2
CASI.1	J7	F1
POUT14	J10	$V_{CC}/2$
POUT12	J11	$V_{CC}/2$
CASI.14	K1	F6
CASI.11	K2	F3
CASI.10	K3	F2
CASI.7	K4	F7
CASI.4	K5	F4
V_{CC}	K6	V_{CC}
FRAME	K7	F15
POUT19	K8	$V_{CC}/2$
POUT16	K9	$V_{CC}/2$
GND	K10	GND
POUT13	K11	$V_{CC}/2$
CASI.12	L1	F4
CASI.9	L2	F1
CASI.8	L3	F0
CASI.6	L4	F6
CASI.3	L5	F3
RESET	L6	F16
CASI.0	L7	F0
GND	L8	GND
POUT18	L9	$V_{CC}/2$
POUT17	L10	$V_{CC}/2$
POUT15	L11	$V_{CC}/2$

NOTES:
1. $V_{CC}/2$ (2.7V ± 10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5 ± 0.5V.
4. 0.1μF (min) capacitor between V_{CC} and GND per position.
5. F0 = 100kHz ± 10%, F1 = F0/2, F2 = F1/2 . . . F11 = F10/2, 40-60% Duty Cycle.
6. Input Voltage Limits: V_{IL} = 0.8V max., V_{IH} = 4.5V ± 10%.

Die Characteristics

DIE DIMENSIONS:
341 x 322 x 19 ± 1 mils

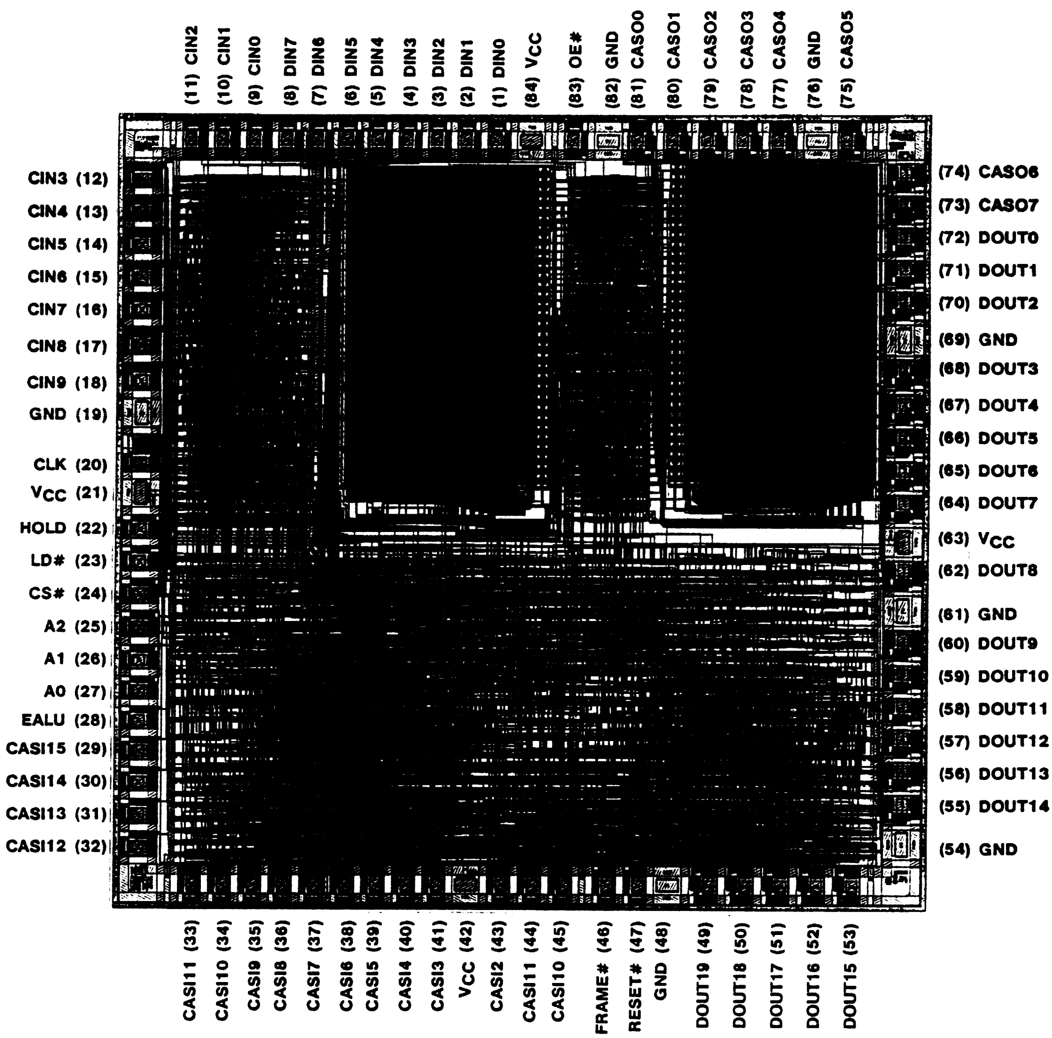
METALLIZATION:
Type: Si - Al or Si-Al-Cu
Thickness: 8kÅ

WORST CASE CURRENT DENSITY:
$2 \times 10^5 A/cm^2$

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

Metallization Mask Layout

HSP48908/883



HARRIS SEMICONDUCTOR

HSP9501

January 1994

Programmable Data Buffer

Features

- DC to 32MHz Operating Frequency
- Programmable Buffer Length from 2 to 1281 Words
- Supports Data Words to 10-Bits
- Clock Select Logic for Positive or Negative Edge System Clocks
- Data Recirculate or Delay Modes of Operation
- Expandable Data Word Width or Buffer Length
- Three-State Outputs
- TTL Compatible Inputs/Outputs
- Low Power CMOS

Applications

- Sample Rate Conversion
- Data Time Compression/Expansion
- Software Controlled Data Alignment
- Programmable Serial Data Shifting
- Audio/Speech Data Processing Video/Image Processing

Video/Image Processing

- 1-H Delay Line of 910 NTSC, 1135 PAL or 1280 Samples:
  - High Resolution Monitor Delay Line
  - Comb Filter Designs
  - Progressive Scanning Display
  - TV Standards Conversion
  - Image Processing

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP9501JC-25	0°C to +70°C	44 Lead PLCC
HSP9501JC-32	0°C to +70°C	44 Lead PLCC

Description

The HSP9501 is a 10-Bit wide programmable data buffer designed for use in high speed digital systems. Two different modes of operation can be selected through the use of the MODSEL input. In the delay mode, a programmable data pipeline is created which can provide 2 to 1281 clock cycles of delay between the input and output data. In the data recirculate mode, the output data path is internally routed back to the input to provide a programmable circular buffer.

The length of the buffer or amount of delay is programmed through the use of the 11-bit length control input port (LC0-10) and the length control enable (LCEN#). An 11-bit value is applied to the LC0-10 inputs, LCEN# is asserted, and the next selected clock edge loads the new count value into the length control register. The delay path of the HSP9501 consists of two registers with a programmable delay RAM between them, therefore, the value programmed into the length control register is the desired length - 2. The range of values which can be programmed into the length control register are from 0 to 1279, which in turn results in an overall range of programmable delays from 2 to 1281.

Clock select logic is provided to allow the use of a positive or negative edge system clock as the CLK input to the HSP9501. The active edge of the CLK input is controlled through the use of the CLKSEL input. All synchronous timing (i.e. data setup, hold and output delays) are relative to the clock edge selected by CLKSEL. An additional clock enable input (CLKEN#) provides a means of disabling the internal clock and holding the existing contents temporarily. All outputs of the HSP9501 are three-state outputs to allow direct interfacing to system or multi-use busses.

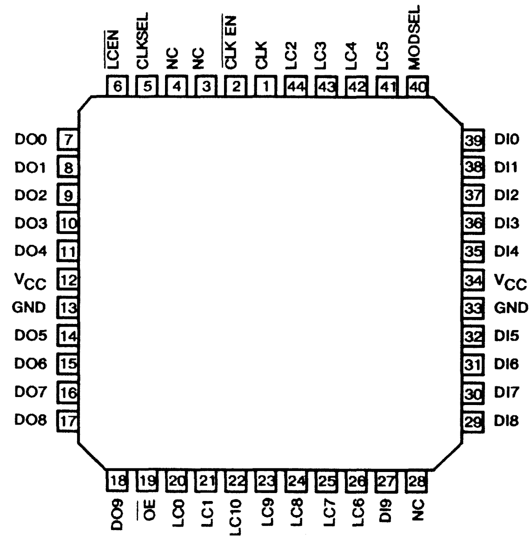
The HSP9501 is recommended for digital video processing or any applications which require a programmable delay or circular data buffer.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

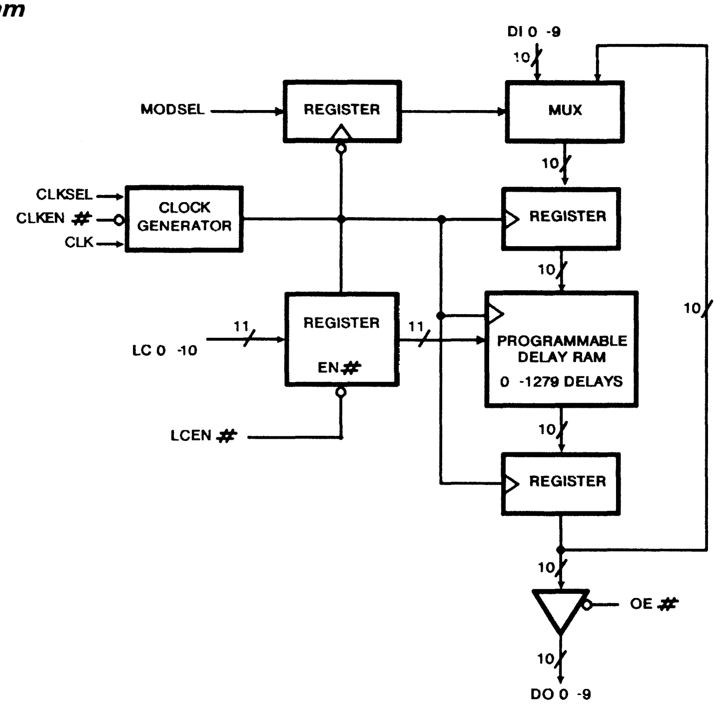
File Number 2786.3

Pinout

44 PIN PLASTIC LEADED CHIP CARRIER (PLCC)
TOP VIEW



Block Diagram



Pin Descriptions

NAME	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	12, 34		The +5V power supply pin. A 0.1μF capacitor between the V_{CC} and GND pin is recommended.
GND	13, 33		The device ground.
CLK	1	I	Input Clock. This clock signal is used to control the data movement through the programmable buffer. It is also the signal which latches the input data, length control word and mode select. Input setup and hold times with respect to the clock must be met for proper operation.
DI0-9	27, 29-32, 35-39	I	Data Inputs. This 10-bit input port is used to provide the input data. When MODSEL is low, data on the DI0-9 inputs is latched on the clock edge selected by CLKSEL.
DO0-9	7-11, 14-18	O	Data Outputs. This 10-bit port provides the output data from the internal delay registers. Data latched into the DI0-9 inputs will appear at the DO0-9 outputs on the Nth clock cycle, where N is the total delay programmed.
LC0-10	20-26, 41-44	I	Length Control Inputs. These inputs are used to specify the number of clock cycles of delay between the DI0-9 inputs and the DO0-9 outputs. An integer value between 0 and 1279 is placed on the LC0-10 inputs, and the total delay length (N) programmed is the LC0-10 value plus 2. In order to properly load an active length control word, the value must be presented to the LC0-10 inputs and LCEN# must be asserted during an active clock edge selected by CLKSEL.
LCEN#	6	I	Length Control Enable. LCEN# is used in conjuction with LC0-10 and CLK to load a new length control word. An 11-bit value is loaded on the LC0-10 inputs, LCEN# is asserted, and the next selected clock edge will load the new count value. Since this operation is synchronous, LCEN# must meet the specified setup/hold times with respect to CLK for proper operation.
OE#	19	I	Output Enable. This input controls the state of the DO0-9 output port. A low on this control line enables the port for output. When OE# is high, the output drivers are in the high impedance state. Internal latching or transfer of data is not affected by this input.
MODSEL	40	I	Mode Select. This input is used to control the mode of operation of the HSP9501. A low on MODSEL causes the device to latch new data at the DI0-9 inputs on every clock cycle, and operate as a programmable pipeline register. When MODSEL is high, the HSP9501 is in the recirculate mode, and will operate as a programmable length circular buffer. This control signal may be used in a synchronous fashion during device operation, however, care must be taken to ensure the required setup/hold times with respect to CLK are met.
CLKSEL	5	I	Clock Select Control. This input is used to determine which edge of the CLK signal is used for controlling all internal events. A low on CLKSEL selects the negative going edge, therefore, all setup, hold, and output delay times are with respect to the negative edge of CLK. When CLKSEL is high, the positive going edge is selected and all synchronous timing is with respect to the positive edge of the CLK signal.
CLKEN#	2	I	Clock Enable. This control signal can be used to enable or disable the CLK input. When low, the CLK input is enabled and will operate in a normal fashion. A high on CLKEN# will disable the CLK input and will "hold" all internal operations and data. This control signal may also be used in a synchronous fashion, however, setup and hold requirements with respect to CLK must be met for proper device operation. This signal takes effect on the clock following the one that latches it in.

Functional Description

The HSP9501 is a 10-bit wide programmable length data buffer. The length of delay is programmable from 2 to 1281 delays in single delay increments.

Data into the delay line may be selected from the data input bus (DI0-9) or as recirculated output, depending on the state of the mode select (MODSEL) control input.

Mode Select

The MODSEL control pin selects the source of the data moving into the delay line. When MODSEL is low, the data input bus (DI0-9) is the source of the data. When MODSEL is high, the output of the HSP9501 is routed back to the input to form a circular buffer.

The MODSEL control line is latched at the input by the CLK signal. The edge which latches this control signal is determined by the CLKSEL control line. In either case, the MODSEL line is latched on one edge of the CLK signal with the following edge moving data into and through the HSP9501. Refer to the functional timing waveforms for specific timing references.

Clock Select Logic

The clock select logic is provided to allow the use of positive or negative edge system clocks. The active edge of the CLK input to the HSP9501 is controlled through the use of the CLKSEL input.

When CLKSEL is low, the negative going edge of CLK is used to control all internal operations. A high on CLKSEL selects the positive going edge of CLK.

All synchronous timing (i.e. setup, hold and output propagation delay times are relative to the CLK edge selected by CLKSEL. Functional timing waveforms for each state of CLKSEL are provided (refer to timing waveforms for details).

Delay Path Control

The HSP9501 buffer length is programmable from 2 to 1281 data words in one word increments. The minimum number of delays which can be programmed is two, consisting of the input and output buffer registers only.

The Length control inputs (LC0-10) are used to set the length of the programmable delay ram which can vary in length from 0 to 1279. The total length of the HSP9501 data buffer will then be equal to the programmed value on LC0-10 plus 2. The programmed delay is established by the 11-bit integer value of the LC0-10 inputs with LC10 as the MSB and LC0 as the LSB.

For example,

LC10	9	8	7	6	5	4	3	2	1	LC0
0	0	0	0	1	0	0	0	0	0	1

programs a length value of $2^6 + 2^0 = 65$. The total length of the delay will be 65 + 2 or 67 delays.

Table 1 indicates several programming values. The decimal value placed on LC0-10 must not exceed 1279. Controlled operation with larger values is not guaranteed.

Values on LC0-10 are latched on the CLK edge selected by the CLKSEL control line, when LCEN# is active. LC0-10 and LCEN# must meet the specified setup and hold times relative to the selected CLK edge for proper device operation.

TABLE 1. LENGTH CONTROL PROGRAMMING EXAMPLES

LC10 2^{10}	LC9 2^9	LS8 2^8	LC7 2^7	LC6 2^6	LC5 2^5	LC4 2^4	LC3 2^3	LC2 2^2	LC1 2^1	LC0 2^0	PROGRAMMED LENGTH	TOTAL LENGTH N
0	0	0	0	0	0	0	0	0	0	0	0	2
0	0	0	0	1	1	1	0	1	1	0	118	120
0	1	1	0	0	1	0	1	0	0	0	808	810
1	0	0	0	0	0	1	1	0	0	1	1049	1051
1	0	0	1	1	1	1	1	1	1	1	1279	1281

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input or Output Voltage Applied .... GND -0.5V to V_{CC} +0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +150°C
Maximum Package Power Dissipation 1.7W
θ_{JC} .... 16.4°C/W
θ_{JA} .... 45.2°C/W
Lead Temperature (Soldering, Ten Seconds) .... +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.75V to +5.25V
Operating Temperature Range .... 0°C to +70°C

D.C. Electrical Specifications (V_{CC} = 5.0V + 5%, T_A = 0°C to +70°C, Commercial)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.0	-	V	V_{CC} = 5.25V
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = 4.75V
Output HIGH Voltage	V_{OH}	2.4	-	V	I_{OH} = -4mA V_{CC} = 4.75V
Output LOW Voltage	V_{OL}	-	0.4	V	I_{OL} = +4.0mA V_{CC} = 4.75V
Input Leakage Current	I_I	-10	10	μA	V_{IN} = GND or V_{CC} V_{CC} = 5.25V
Output Leakage Current	I_O	-10	10	μA	V_{OUT} = GND or V_{CC} V_{CC} = 5.25V
Standby Current	I_{CCSB}	-	500	μA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Note 2
Operating Power Supply Current	I_{CCOP}	-	125	mA	f = 25MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.25V, Note 1, 2
Input Capacitance	C_{IN}	-	10	pF	FREQ = 1MHz, V_{CC} = Open, All measurements are referenced to device GND
Output Capacitance	C_O	-	10	pF	

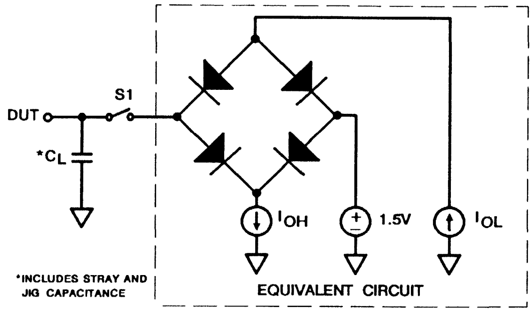
A.C. Electrical Specifications (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C, Commercial), (Note 4)

PARAMETER	SYMBOL	-32		-25		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Clock Period	T_{CP}	31	-	40	-	ns	
Clock Pulse Width High	T_{PWH}	12	-	15	-	ns	
Clock Pulse Width Low	T_{PWL}	12	-	15	-	ns	
Data Input Setup Time	T_{DS}	10	-	12	-	ns	
Data Input Hold Time	T_{DH}	2	-	2	-	ns	
Output Enable Time	T_{ENA}	-	20	-	25	ns	
Output Disable Time	T_{DIS}	-	24	-	25	ns	Note 3
CLKEN# to Clock Setup	T_{ES}	10	-	12	-	ns	
CLKEN# to Clock Hold	T_{EH}	2	-	2	-	ns	
LC0-10 Setup Time	T_{LS}	10	-	13	-	ns	
LC0-10 Hold Time	T_{LH}	2	-	2	-	ns	
LCEN# to Clock Setup	T_{LES}	10	-	13	-	ns	
LCEN# to Clock Hold	T_{LEH}	2	-	2	-	ns	
MODSEL Setup Time	T_{MS}	10	-	13	-	ns	
MODSEL Hold Time	T_{MH}	2	-	2	-	ns	
Clock to Data Out	T_{OUT}	-	16	-	22	ns	
Output Hold from Clock	T_{OH}	4	-	4	-	ns	
Rise, Fall Time	T_{RF}	-	6	-	6	ns	Note 3

NOTES:

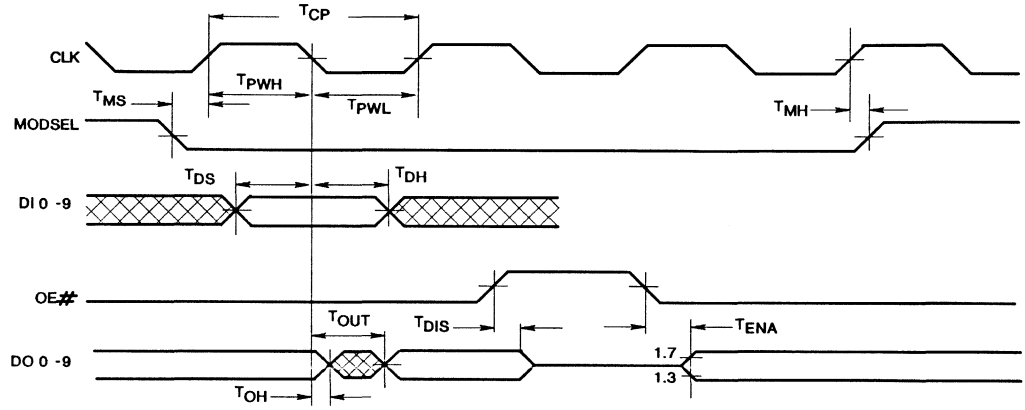
1. Power supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 5mA/MHz.
2. Output load per test load circuit with switch open and C_L = 40pF.
3. Controlled by design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
4. A.C. Testing is performed as follows: Input levels: 0V and 3.0V, Timing reference levels = 1.5V, Input rise and fall times driven at 1ns/V, Output load C_L = 40pF.

Test Load Circuit

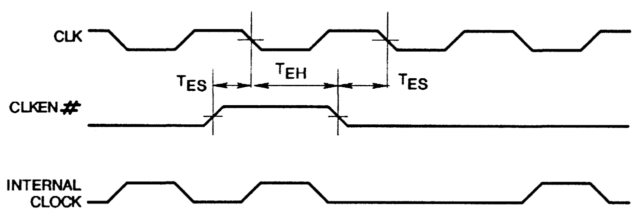


Switch S1 Open for I_{CCSB} and I_{CCOP} Tests

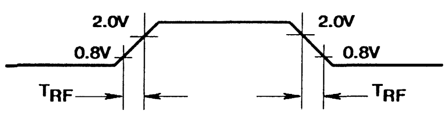
Timing Waveforms



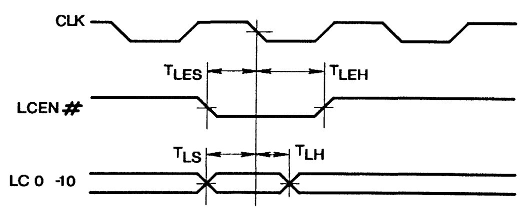
FUNCTIONAL TIMING (CLKSEL = LOW)



CLKEN# TIMING (CLKSEL = LOW)

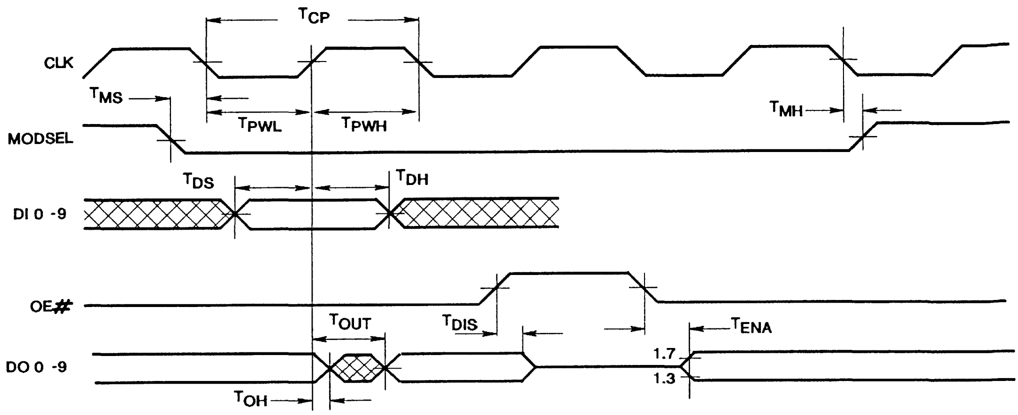


OUTPUT RISE AND FALL TIMES

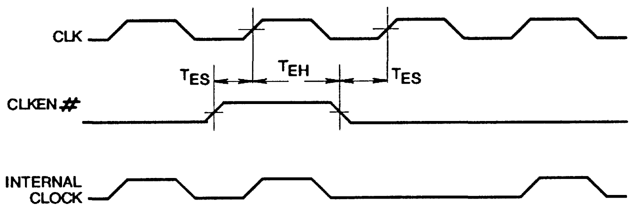


LENGTH CONTROL TIMING (CLKSEL = LOW)

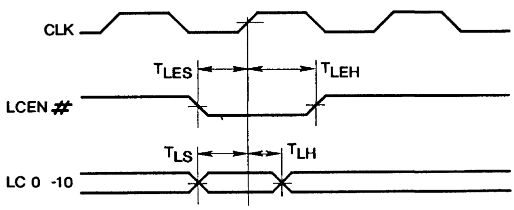
Timing Waveforms (Continued)



FUNCTIONAL TIMING (CLKSEL = HIGH)



CLKEN# TIMING (CLKSEL = HIGH)



LENGTH CONTROL TIMING (CLKSEL = HIGH)

DSP 5

SIGNAL SYNTHESIZERS

HARRIS SEMICONDUCTOR

HSP45102

January 1994

12-Bit Numerically Controlled Oscillator

Features

- 33MHz, 40MHz Versions
- 32-Bit Frequency Control
- BFSK, QPSK Modulation
- Serial Frequency Load
- 12-Bit Sine Output
- Offset Binary Output Format
- 0.009Hz Tuning Resolution at 40MHz
- Spurious Frequency Components < -69dBc
- Fully Static CMOS
- Low Cost

Applications

- Direct Digital Synthesis
- Modulation

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP45102PC-33	0°C to +70°C	28 Lead Plastic DIP
HSP45102PC-40	0°C to +70°C	28 Lead Plastic DIP
HSP45102PI-33	-40°C to +85°C	28 Lead Plastic DIP
HSP45102PI-40	-40°C to +85°C	28 Lead Plastic DIP
HSP45102SC-33	0°C to +70°C	28 Lead SOIC
HSP45102SC-40	0°C to +70°C	28 Lead SOIC
HSP45102SI-33	-40°C to +85°C	28 Lead SOIC
HSP45102SI-40	-40°C to +85°C	28 Lead SOIC

Description

The Harris HSP45102 is Numerically Controlled Oscillator with 32 bit frequency resolution and 12 bit output. With over 69dB of spurious free dynamic range and worst case frequency resolution of 0.009Hz, the NCO12 provides dramatic improvements in accuracy over other frequency synthesis solutions at a competitive price.

The frequency to be generated is selected from two frequency control words. A single control pin selects which word is used to determine the output frequency. Switching from one frequency to another occurs in one clock cycle, with a 6 clock pipeline delay from the time that the new control word is loaded until the new frequency appears on the output.

Two pins, P0-1, are provided for phase modulation. They are encoded and added to the top two bits of the phase accumulator to offset the phase in 90o increments.

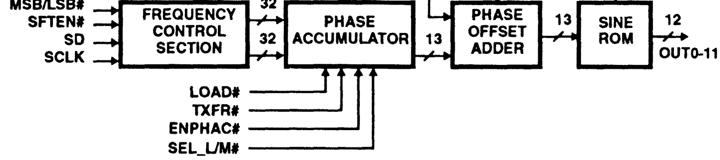
The 13 bit output of the Phase Offset Adder is mapped to the sine wave amplitude via the Sine ROM. The output data format is offset binary to simplify interfacing to D/A converters. Spurious frequency components in the output sinusoid are less than -69dBc.

The NCO12 has applications as a Direct Digital Synthesizer and modulator in low cost digital radios, satellite terminals, and function generators.

5

SIGNAL SYNTHESIZERS

Block Diagram

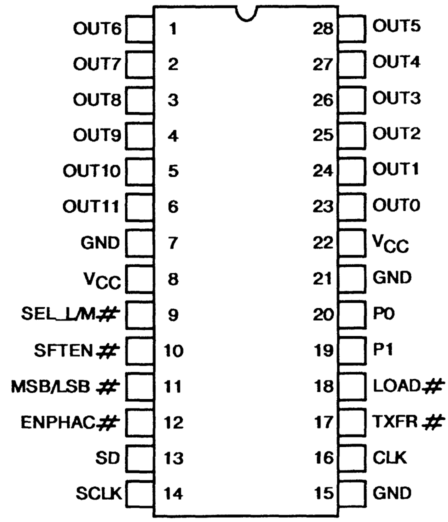


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2810.4

Pinout

28 PIN DIP, 28 PIN SOIC
TOP VIEW



Pin Description

NAME	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	8, 22		+5V power supply pin.
GND	7, 15, 21		Ground
P0-1	19, 20	I	Phase modulation inputs (become active after a pipeline delay of four clocks). A phase shift of 0, 90, 180, or 270 degrees can be selected (Table 1).
CLK	16	I	NCO clock. (CMOS level)
SCLK	14	I	This pin clocks the frequency control shift register.
SEL_L/M#	9	I	A high on this input selects the least significant 32 bits of the 64 bit frequency register as the input to the phase accumulator; a low selects the most significant 32 bits.
SFTEN#	10	I	The active low input enables the shifting of the frequency register.
MSB/LSB#	11	I	This input selects the shift direction of the frequency register. A low on this input shifts in the data LSB first; a high shifts in the data MSB first.
ENPHAC#	12	I	This pin, when low, enables the clocking of the Phase Accumulator. This input has a pipeline delay of four clocks.
SD	13	I	Data on this pin is shifted into the frequency register by the rising edge of SCLK when SFTEN# is low.
TXFR#	17	I	This active low input is clocked onto the chip by CLK and becomes active after a pipeline delay of four clocks. When low, the frequency control word selected by SEL_L/M# is transferred from the frequency register to the phase accumulator's input register.
LOAD#	18	I	This input becomes active after a pipeline delay of five clocks. When low, the feedback in the phase accumulator is zeroed.
OUT0-11	1-6, 23-28	O	Output data. OUT0 is LSB. Unsigned.

All inputs are TTL level, with the exception of CLK.

sign designates active low signals.

Functional Description

The NCO12 produces a 12 bit sinusoid whose frequency and phase are digitally controlled. The frequency of the sine wave is determined by one of two 32 bit words. Selection of the active word is made by SEL_L/M#. The phase of the output is controlled by the two bit input P0-1, which is used to select a phase offset of 0^{o}, 90^{o}, 180^{o}, or 270^{o}.

As shown in the Block Diagram, the NCO12 consists of a Frequency Control Section, a Phase Accumulator, a Phase Offset Adder and a Sine ROM. The Frequency Control section serially loads the frequency control word into the frequency register. The Phase Accumulator and Phase Offset Adder compute the phase angle using the frequency control word and the two phase modulation inputs. The Sine ROM generates the sine of the computed phase angle. The format of the 12 bit output is offset binary.

Frequency Control Section

The Frequency Control Section (Figure 1), serially loads the frequency data into a 64 bit, bidirectional shift register. The shift direction is selected with the MSB/LSB# input. When this input is high, the frequency control word on the SD input is shifted into the register MSB first. When MSB/LSB# is low the data is shifted in LSB first. The register shifts on the rising edge of SCLK when SFTEN# is low. The timing of these signals is shown in Figure 2.

The 64 bits of the frequency register are sent to the Phase Accumulator Section where 32 bits are selected to control the frequency of the sinusoidal output.

Phase Accumulator Section

The phase accumulator and phase offset adder compute the phase of the sine wave from the frequency control word and the phase modulation bits P0-1. The architecture is shown in Figure 1. The most significant 13 bits of the 32 bit phase accumulator are summed with the two bit phase offset to generate the 13 bit phase input to the Sine Rom. A value of 0 corresponds to 0^{o}, a value of 1000 hexadecimal corresponds to a value of 180^{o}.

The phase accumulator advances the phase by the amount programmed into the frequency control register. The output frequency is equal to $N*Fclk/2^{32}$, where N is the selected 32 bits of the frequency control word. For example, if the control word is 20000000 hexadecimal and the clock frequency is 30Mhz, then the output frequency would be Fclk/8 or 3.75Mhz.

The frequency control multiplexer selects the least significant 32 bits from the 64 bit frequency control register when SEL_L/M# is high, and the most significant 32 bits when SEL_L/M# is low. When only one frequency word is desired, SEL_L/M# and MSB/LSB# must be either both high or both low. This is due to the fact that when a frequency control word is loaded into the shift register LSB first, it enters through the most significant bit of the register. After 32 bits have been shifted in, they will reside in the 32 most significant bits of the 64 bit register.

When TXFR# is asserted, the 32 bits selected by the frequency control multiplexer are clocked into the phase accumulator input register. At each clock, the contents of this register are summed with the current contents of the accumulator to step to the new phase. The phase accumulator stepping may be inhibited by holding ENPHAC# high. The phase accumulator may be loaded with the value in the input register by asserting LOAD#, which zeroes the feedback to the phase accumulator.

The phase adder sums the encoded phase modulation bits P0-1 and the output of the phase accumulator to offset the phase by 0, 90, 180 or 270 degrees. The two bits are encoded to produce the phase mapping shown in Table 1. This phase mapping is provided for direct connection to the in-phase and quadrature data bits for QPSK modulation.

TABLE 1

P0-1 CODING		
P1	P0	PHASE SHIFT (DEGREES)
0	0	0
0	1	90
1	0	270
1	1	180

ROM Section

The ROM section generates the 12 bit sine value from the 13 bit output of the phase adder. The output format is offset binary and ranges from 001 to FFF hexadecimal, centered around 800 hexadecimal.

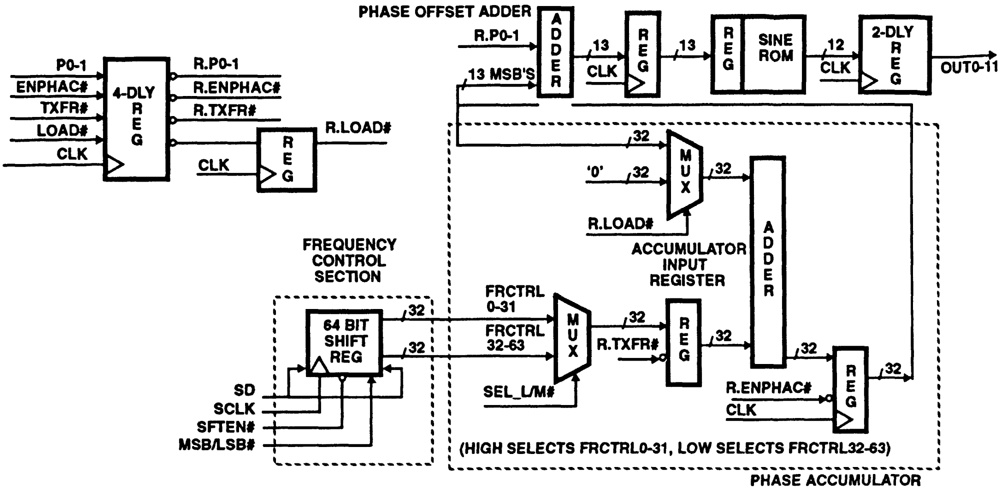


FIGURE 1. NCO-12 FUNCTIONAL BLOCK DIAGRAM

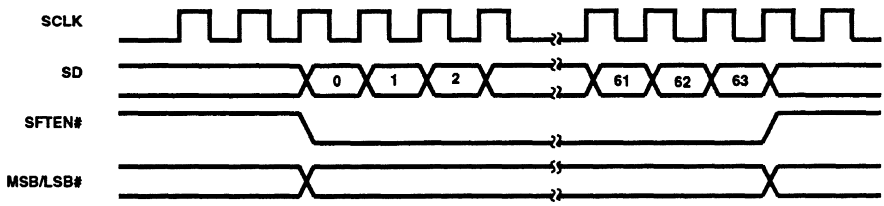


FIGURE 2A. FREQUENCY LOADING ENABLED BY SFTEN#

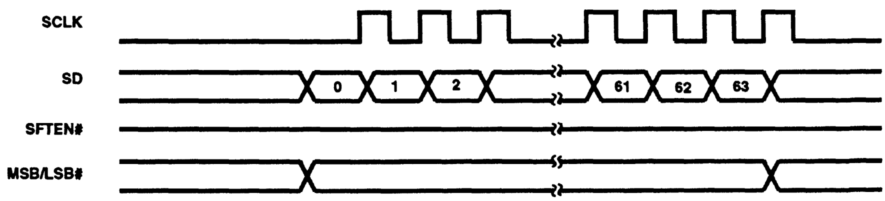


FIGURE 2B. FREQUENCY LOADING CONTROLLED BY SCLK

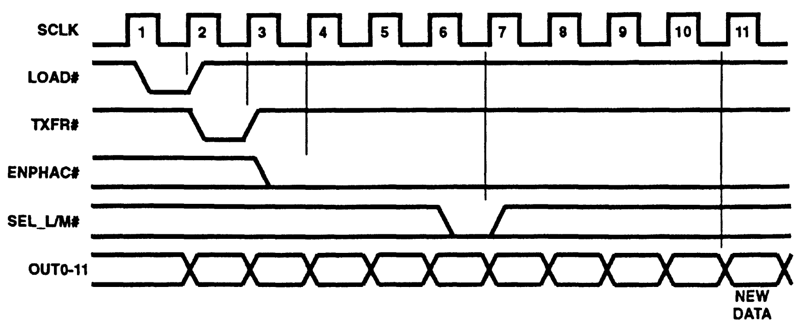


FIGURE 3. I/O TIMING

Absolute Maximum Ratings

Supply Voltage	+8.0V
Input, Output or I/O Voltage Applied	GND -0.5V to V_{CC} +0.5V
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Maximum Package Power Dissipation (Commercial)	1.5W (DIP), 1.1W (SOIC)
Maximum Package Power Dissipation (Industrial)	1.3°C/W (DIP), 0.9°C/W (SOIC)
θjc	20.3°C/W (DIP), 21.6°C/W (SOIC)
θja	50.1°C/W (DIP), 71.4°C/W (SOIC)
Device Count	32,528 Transistors
Lead Temperature (Soldering, Ten Seconds)	+300°C
ESD Classification	Class 1

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range (Commercial, Industrial)	+4.75V to +5.25V
Operating Temperature Range (Commercial)	0°C to +70°C
Operating Temperature Range (Industrial)	-40°C to +85°C

D.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0	-	V	V_{CC} = 5.25V
V_{IL}	Logical Zero Input Voltage	-	0.8	V	V_{CC} = 4.75V
V_{IHC}	High Level Clock Input	3.0	-	V	V_{CC} = 5.25V
V_{ILC}	Low Level Clock Input	-	0.8	V	V_{CC} = 4.75V
V_{OH}	Output HIGH Voltage	2.6	-	V	I_{OH} = -400μA, V_{CC} = 4.75V
V_{OL}	Output LOW Voltage	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.75V
I_I	Input Leakage Current	-10	10	μA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V
I_{CCSB}	Standby Power Supply Current	-	500	μA	V_{IN} = V_{CC} or GND V_{CC} = 5.25V, Note 3
I_{CCOP}	Operating Power Supply Current	-	99	mA	f = 33MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.25V, Notes 1 and 3

Capacitance (T_A = +25°C, Note 2)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	-	10	pF	FREQ = 1MHz, V_{CC} = Open, All measurements are referenced to device ground
C_O	Output Capacitance	-	10	pF	

NOTES:

1. Power supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 3mA/MHz.
2. Not tested, but characterized at initial design and at major process/design changes.
3. Output load per test load circuit with switch open and C_L = 40pF.

5

SIGNAL SYNTHESIZERS

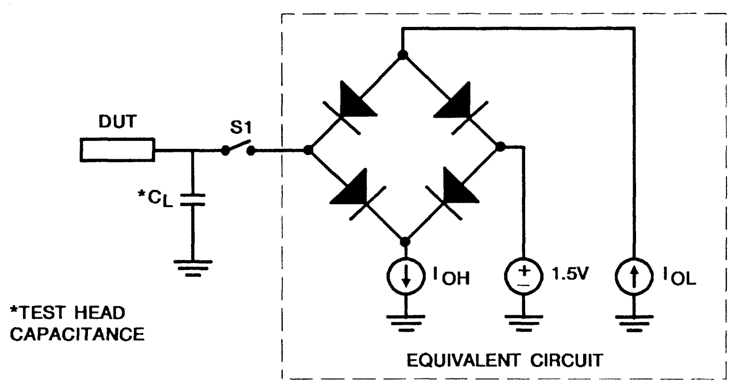
A.C. Electrical Specifications V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C, T_A = -40°C to +85°C (Note 1)

SYMBOL	PARAMETER	-33 (33MHz)		-40 (40MHz)		COMMENTS
		MIN	MAX	MIN	MAX	
T_{CP}	Clock Period	30	-	25	-	ns
T_{CH}	Clock High	12	-	10	-	ns
T_{CL}	Clock Low	12	-	10	-	ns
T_{SW}	SCLK High/Low	12	-	10	-	ns
T_{DS}	Set-up Time SD to SCLK Going High	12	-	12	-	ns
T_{DH}	Hold Time SD from SCLK Going High	0	-	0	-	ns
T_{MS}	Set-up Time SFTEN#, MSB/LSB# to SCLK Going HGgh	15	-	12	-	ns
T_{MH}	Hold Time SFTEN#, MSB/LSB# from SCLK Going High	0	-	0	-	ns
T_{SS}	Set-up Time SCLK High to CLK Going High	16	-	15	-	ns, Note 2
T_{PS}	Set-up Time P0-1 to CLK Going High	15	-	12	-	ns
T_{PH}	Hold Time P0-1 from CLK Going High	1	-	1	-	ns
T_{ES}	Set-up Time LOAD#, TXFR#, ENPHAC#, SEL_L/M# to CLK Going High	15	-	13	-	ns
T_{EH}	Hold Time LOAD#, TXFR#, ENPHAC#, SEL_L/M# from CLK Going High	1	-	1	-	ns
T_{OH}	CLK to Output Delay	2	15	2	13	ns
T_{RF}	Output Rise, Fall Time	8	-	8	-	ns, Note 3

NOTES

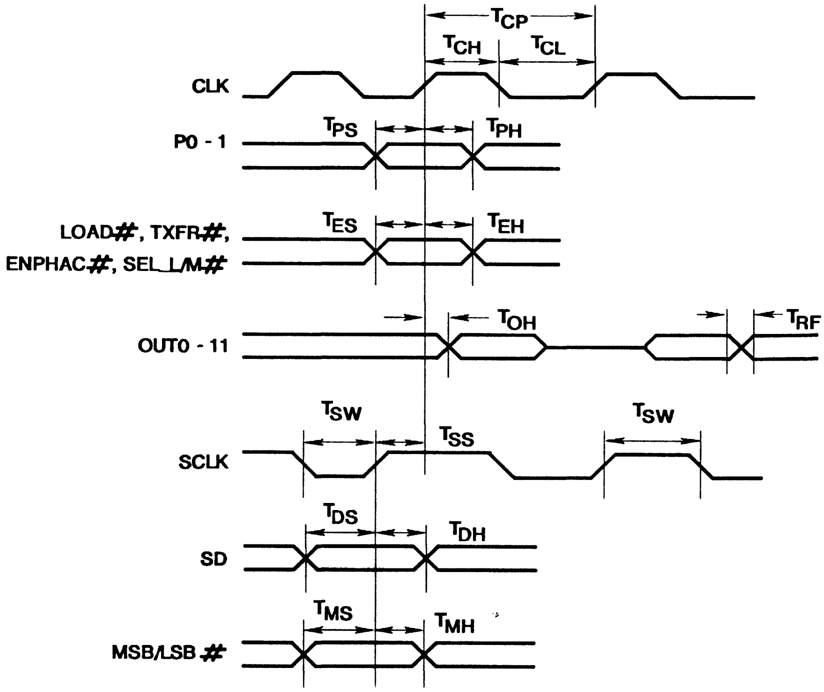
1. A.C. testing is performed as follows: Input levels (CLK Input) 4.0V and 0V; Input levels (all other inputs) 0V and 3.0V; Timing reference levels (CLK) 2.0V; All others 1.5V. Output load per test load circuit with switch closed and C_L = 40 pF. Output transition is measured at $V_{OH} \geq$ 1.5V and $V_{OL} \leq$ 1.5V.
2. If TXFR# is active, care must be taken to not violate set-up and hold times as data from the shift registers may not have settled before CLK occurs.
3. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

A.C. Test Load Circuit



Switch S1 open for I_{CCSB} and I_{CCOP}

Waveforms



TCP
TCH
TCL
CLK
P0 - 1
TPS
TPH
LOAD#, TXFR#,
ENPHAC#, SEL_L/M#
TES
TEH
OUT0 - 11
TOH
TRF
TSW
TSS
TSW
SCLK
TDS
TDH
SD
TMS
TMH
MSB/LSB#

HARRIS SEMICONDUCTOR

HSP45106

January 1994

16-Bit Numerically Controlled Oscillator

Features

- **25.6MHz, 33MHz Versions**
- **32-Bit Center and Offset Frequency Control**
- **16-Bit Phase Control**
- **8 Level PSK Supported Through Three Pin Interface**
- **Simultaneous 16-Bit Sine and Cosine Outputs**
- **Output in Two's Complement or Offset Binary**
- **<0.008Hz Tuning Resolution at 33MHz**
- **Serial or Parallel Outputs**
- **Spurious Frequency Components < -90dBc**
- **16-Bit Microprocessor Compatible Control Interface**

Applications

- **Direct Digital Synthesis**
- **Quadrature Signal Generation**
- **Modulation - FM, FSK, PSK (BPSK, QPSK, 8PSK)**
- **Precision Signal Generation**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP45106JC-25	0°C to +70°C	84 Lead PLCC
HSP45106JC-33	0°C to +70°C	84 Lead PLCC
HSP45106GC-25	0°C to +70°C	85 Lead PGA
HSP45106GC-33	0°C to +70°C	85 Lead PGA

Description

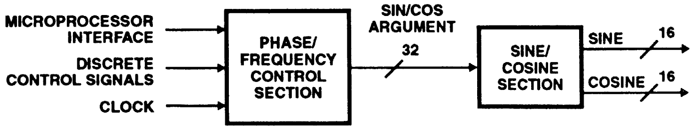
The Harris HSP45106 is a high performance 16-bit quadrature numerically controlled oscillator (NCO16). The NCO16 simplifies applications requiring frequency and phase agility such as frequency-hopped modems, PSK modems, spread spectrum communications, and precision signal generators. As shown in the block diagram, the HSP45106 is divided into a Phase/Frequency Control Section (PFCS) and a Sine/Cosine Section.

The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The frequency resolution is 32-bits, which provides for resolution of better than 0.008Hz at 33MHz. User programmable center frequency and offset frequency registers give the user the capability to perform phase coherent switching between two sinusoids of different frequencies. Further, a programmable phase control register allows for phase control of better than 0.006°. In applications requiring up to 8-level PSK, three discrete inputs are provided to simplify implementation.

The output of the PFCS is a 32-bit phase which is input to the Sine/Cosine Section for conversion into sinusoidal amplitude.The outputs of the sine/cosine section are two 16-bit quadrature signals. The spurious free dynamic range of this complex vector is greater than 90dBc.

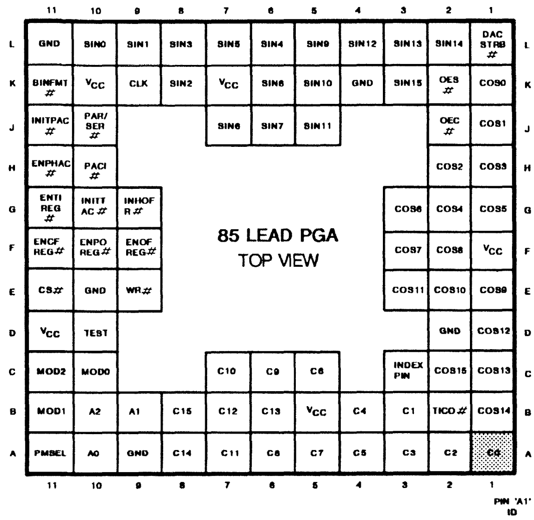
For added flexibility when using the NCO16 in conjunction with DAC's, a choice of either parallel of serial outputs with either two's complement or offset binary encoding is provided. In addition, a synchronization signal is available which signals serial word boundaries.

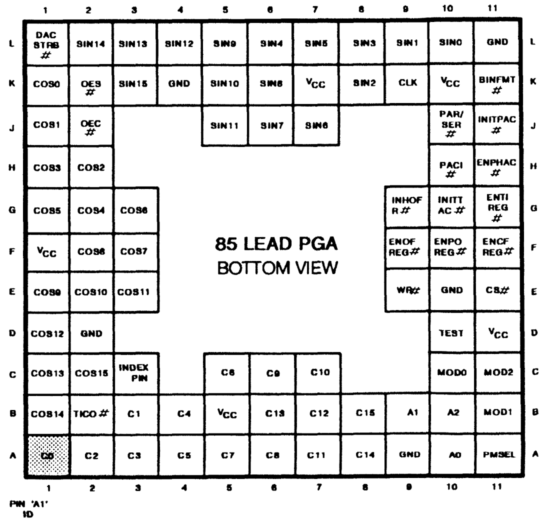
Block Diagram

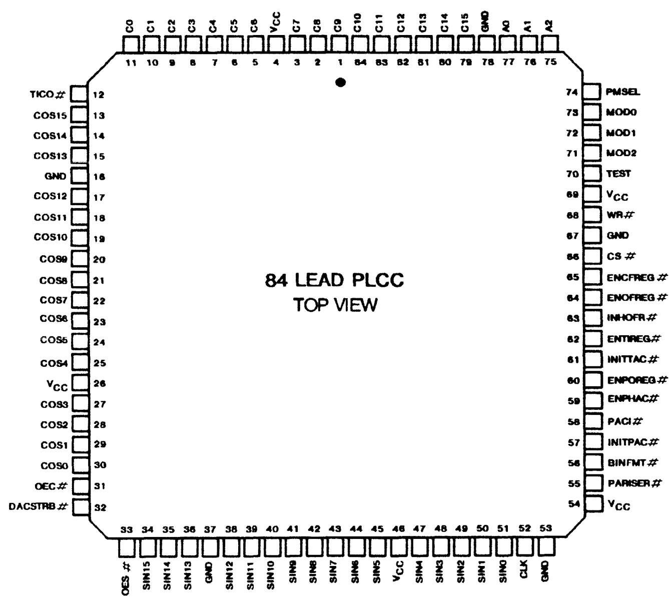


File Number **2809.2**

Pinouts


85 LEAD PGA
TOP VIEW
11 10 9 8 7 6 5 4 3 2 1
L GND SIN0 SIN1 SIN3 SIN5 SIN4 SIN9 SIN12 SIN13 SIN14 DAC STRB #
K BINFMT # VCC CLK SIN2 VCC SIN8 SIN10 GND SIN15 OES # COS0
J INITPAC # PAR/ SER # SIN6 SIN7 SIN11 OEC # COS1
H ENPHAC # PACI # COS2 COS3
G ENTI REG # INITT AC # INHOF R # COS6 COS4 COS5
F ENCF REG# ENPO REG# ENOF REG# COS7 COS8 VCC
E CS# GND WR# COS11 COS10 COS9
D VCC TEST GND COS12
C MOD2 MOD0 C10 C9 C6 INDEX PIN COS15 COS13
B MOD1 A2 A1 C15 C12 C13 VCC C4 C1 TICO# COS14
A PMSEL A0 GND C14 C11 C8 C7 C5 C3 C2 C0
PIN 'A1' ID


85 LEAD PGA
BOTTOM VIEW
1 2 3 4 5 6 7 8 9 10 11
L DAC STRB # SIN14 SIN13 SIN12 SIN9 SIN4 SIN5 SIN3 SIN1 SIN0 GND
K COS0 OES # SIN15 GND SIN10 SIN8 VCC SIN2 CLK VCC BINFMT #
J COS1 OEC # SIN11 SIN7 SIN6 PAR/ SER # INITPAC #
H COS3 COS2 PACI # ENPHAC #
G COS5 COS4 COS6 INHOF R# INITT AC # ENTI REG #
F VCC COS8 COS7 ENOF REG# ENPO REG# ENCF REG#
E COS9 COS10 COS11 WR# GND CS#
D COS12 GND TEST VCC
C COS13 COS15 INDEX PIN C6 C9 C10 MOD0 MOD2
B COS14 TICO# C1 C4 VCC C13 C12 C15 A1 A2 MOD1
A C0 C2 C3 C5 C7 C8 C11 C14 GND A0 PMSEL
PIN 'A1' ID


84 LEAD PLCC
TOP VIEW
11 C0, 10 C1, 9 C2, 8 C3, 7 C4, 6 C5, 5 C6, 4 VCC, 3 C7, 2 C8, 1 C9, 84 C10, 83 C11, 82 C12, 81 C13, 80 C14, 79 C15, 78 GND, 77 A0, 76 A1, 75 A2
12 TICO#, 13 COS15, 14 COS14, 15 COS13, 16 GND, 17 COS12, 18 COS11, 19 COS10, 20 COS9, 21 COS8, 22 COS7, 23 COS6, 24 COS5, 25 COS4, 26 VCC, 27 COS3, 28 COS2, 29 COS1, 30 COS0, 31 OEC#, 32 DACSTRB#
33 OES#, 34 SIN15, 35 SIN14, 36 SIN13, 37 GND, 38 SIN12, 39 SIN11, 40 SIN10, 41 SIN9, 42 SIN8, 43 SIN7, 44 SIN6, 45 SIN5, 46 VCC, 47 SIN4, 48 SIN3, 49 SIN2, 50 SIN1, 51 SIN0, 52 CLK, 53 GND
74 PMSEL, 73 MOD0, 72 MOD1, 71 MOD2, 70 TEST, 69 VCC, 68 WR#, 67 GND, 66 CS#, 65 ENCFREG#, 64 ENOFREG#, 63 INHOFR#, 62 ENTIREG#, 61 INITTAC#, 60 ENPOREG#, 59 ENPHAC#, 58 PACI#, 57 INITPAC#, 56 BINFMT#, 55 PARISER#, 54 VCC

Pin Description

NAME	PGA PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	B5, D11, F1, K7, K10		+5 power supply pin.
GND	A9, D2, E10, K4, L11		Ground
C0-15	A1-8, B3-4 B6-8, C5-7	I	Control input bus for loading phase, frequency, and timer data into the PFCS. C0 is LSB.
A0-2	A10, B9-10	I	Address pins for selecting destination of C0-15 data (Table 2).
CS#	E11	I	Chip select (Active low). Enables data to be written into control registers by WR#.
WR#	E9	I	Write enable (Active low). Data is clocked into the register selected by A0-2 on the rising edge of WR# when CS# is low.
CLK	K9	I	Clock. All registers, except the control registers clocked with WR#, are clocked (when enabled) by the rising edge of CLK.
ENPOREG#	F10	I	Phase Offset Register Enable (Active low). Registered on chip by CLK. When active, after being clocked onto chip, ENPOREG# enables the clocking of data into the Phase Offset Register. Allows ROM address to be updated regardless of ENPHAC#.
ENOFREG#	F9	I	Offset Frequency Register Enable (Active low). Registered on chip by CLK. When active, after being clocked onto chip, ENOFREG# enables the clocking of data into the Offset Frequency Register.
ENCFREG#	F11	I	Center Frequency Register Enable (Active low). Registered on chip by CLK. When active, after being clocked onto chip, ENCFREG# enables the clocking of data into the Center Frequency Register.
ENPHAC#	H11	I	Phase Accumulator Register Enable (Active low). Registered on chip by CLK. When active, after being clocked onto chip, ENPHAC#enables the clocking of data into the Phase Accumulator Register.
ENTIREG#	G11	I	Timer Increment Register Enable (Active low). Registered on chip by CLK. When active, after being clocked onto chip, ENTIREG# enables the clocking of data into the Timer Increment Register.
INHOFR#	G9	I	Inhibit Offset Frequency Register Output (active low). Registered on chip by CLK. When active, after being clocked onto chip, INHOFR# zeroes the data path from the Offset Frequency Register to the Frequency Adder. New data can be still clocked into the Offset Frequency Register. INHOFR# does not affect the contents of the register.
INITPAC#	J11	I	Initialize Phase Accumulator (Active low). Registered on chip by CLK. Zeroes the feedback path in the Phase Accumulator. Does not clear the Phase Accumulator Register.
MOD0-2	B11, C10-11	I	Modulation Control Inputs. When selected with the PMSEL line, these bits add an offset of 0, 45, 90, 135, 180, 225, 270, or 315 degrees to the current phase (i.e., modulate the output). The lower 13 bits of the phase control are set to zero. These bits are registered when the Phase Offset Register is enabled.
PMSEL	A11	I	Phase Modulation Select input. Registered on chip by CLK. This input determines the source of the data clocked into the Phase Offset Register. When high, the Phase Input Register is selected. When low, the external modulation pins (MOD0-2) control the three most significant bits of the Phase Offset Register and the 13 least significant bits are set to zero.
PACI#	H10	I	Phase Accumulator Carry Input (Active low). Registered on chip by CLK.
INITTAC#	G10	I	Initialize Timer Accumulator (Active low). This input is registered on chip by CLK. When active, after being clocked onto chip, INITTAC# enables the clocking of data into the Timer increment Register, and also zeroes the feedback path in the Timer Accumulator.
TEST	D10	I	Test select input. Registered on chip by CLK. This input is active high. When active, this input enables test busses to the outputs instead of the sine and cosine data.
PAR/SER#	J10	I	Parallel/Serial Output Select. This input is registered on chip by CLK. When low, the sine and cosine outputs are in serial mode. The output shift registers will load in new data after ENPHAC# goes low and will start shifting the data out after ENPHAC# goes high. When this input is high, the output registers are loaded every clock and no shifting takes place.
BINFMT#	K11	I	Format. This input is registered on chip by CLK. When low, the MSB of the SIN and COS are inverted to form an offset binary (unsigned) number.
OES#	K2	I	Three-state control for bits SIN0-15. Outputs are enabled when OES# is low.
OEC#	J2	I	Three-state control for bits COS0-15. Outputs are enabled when OEC# is low.
TICO#	B2	O	Timer Accumulator Carry Output. Active low, registered. This output goes low when a carry is generated by the Timer Accumulator.

Pin Description (Continued)

NAME	PGA PIN NUMBER	TYPE	DESCRIPTION
DACSTRB#	L1	O	DAC Strobe (Active low). In serial mode, this output will go low when the first bit of a new output word is valid at the shift register output. This pin is active only in serial mode.
SIN0-15	J5-7, K3, K5-6, K8, L2-10	O	Sine output data. When parallel mode is enabled, data is output on SIN0-15. When serial mode is enabled, output data bits are shifted out of SIN15 and SIN0. The bit stream on SIN 15 is provided MSB first while the bit stream on SIN0 is provided LSB first.
COS0-15	B1, C1-2, D1, E1-3, F2-3, G1-3, H1-2, J1, K1	O	Cosine output data. When parallel mode is enabled, data is output on COS0-15. When serial mode is enabled, output data bits are shifted out of COS15 and COS0. The bit stream on COS15 is provided LSB first.
Index Pin	C3		Used to align chip in socket or on circuit board. Must be left as a no connect in circuit.

Functional Description

The 16-bit Numerically Controlled Oscillator (NCO16) produces a digital complex sinusoid waveform whose frequency and phase are controlled through a standard microprocessor interface and discrete inputs. The NCO16 generates 16-bit sine and cosine vectors at a maximum sample rate of 40MHz. The NCO16 can be preprogrammed to produce a constant (CW) sine and cosine output for Direct Digital Synthesis (DDS) applications. Alternatively, the phase and frequency inputs can be updated in real time to produce a FM, PSK, FSK, or MSK modulated waveform. To simplify PSK generation, a 3 pin interface is provided to support modulation of up to 8 levels.

As shown in the Block Diagram, the NCO16 is comprised of a Phase and Frequency Control Section (PFCS) and Sine/Cosine Section. The PFCS stores the phase and frequency control inputs and uses them to calculate the phase angle of a rotating complex vector. The Sine/Cosine Section performs a lookup on this phase and generates the appropriate amplitude values for the sine and cosine. These quadrature outputs may be configured as serial or parallel with either two's complement or offset binary format.

Phase/Frequency Control Section

The phase and frequency of the quadrature outputs are controlled by the PFCS (Figure 1). The PFCS generates a 32 bit word which represents the instantaneous phase (Sin/Cos argument) of the sine and cosine waves being generated. This phase is incremented on the rising edge of each CLK by the preprogrammed amounts in the phase and frequency control registers. As the instantaneous phase steps from 0 through full scale (2^{32} - 1), the phase of the quadrature outputs proceeds from 0° around the unit circle counter clockwise.

The PFCS is comprised of a Phase Accumulator Section, Phase Offset adder, Input Section, and a Timer Accumulator Section. The Phase Accumulator computes the instantaneous phase angle from user programmed values in the Center and Offset Frequency Registers. This angle is then fed into the Phase Offset adder where it is offset by the preprogrammed value in the Phase Offset Register. The Input Section routes data from a microprocessor compatible control bus and discrete input signals into the appropriate configuration registers. The Timer Accumulator supplies a pulse to mark the passage of a user programmed period of time.

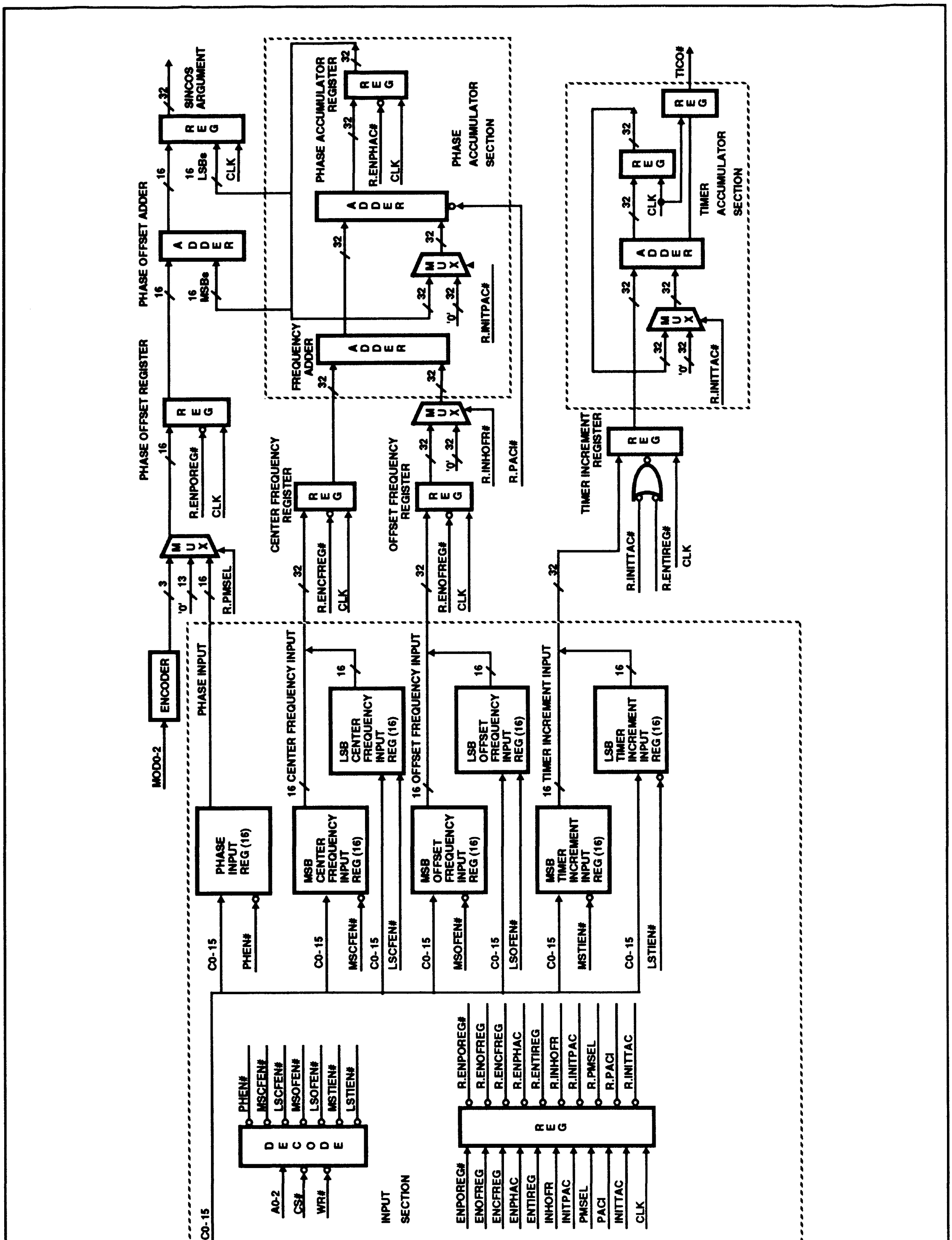
Input Section

The Input Section loads the data on C0-15 into one of the seven input registers, the LSB and MSB Center Frequency Input Registers, the LSB and MSB Offset Frequency Registers, the LSB and MSB Timer Input Registers, and the Phase Input Register. The destination depends on the state of A0-2 when CS# and WR# are low (Table 1).

TABLE 1

A2-0 DECODING					
A2	A1	A0	CS#	WR#	FUNCTION
0	0	0	0	↑	Load least significant bits of Center Frequency input.
0	0	1	0	↑	Load most significant bits of Center Frequency input.
0	1	0	0	↑	Load least significant bits of Offset Frequency input.
0	1	1	0	↑	Load most significant bits of Offset Frequency input.
1	0	0	0	↑	Load least significant bits of Timing Interval input.
1	0	1	0	↑	Load most significant bits of Timing Interval input.
1	1	0	0	↑	Load Phase Register
1	1	1	0	↑	Reserved
X	X	X	1	X	Input Disabled

Once the input registers have been loaded, the control inputs ENCFREG#, ENOFREG#, ENTIREG#, ENCTIREG#, and ENPOREG# will allow the input registers to be downloaded to the PFCS control registers with the input CLK. The control inputs are latched on the rising edge of CLK and the control registers are updated on the rising edge of the following CLK. For example, to load the Center Frequency Register, the data is loaded into the LSB and MSB Center Frequency Input Register, and ENCFREG# is set to zero; the next rising edge of CLK will pass the registered version of ENCFREG#, R.ENCFREG#, to the



SINCOS ARGUMENT
REG
PHASE OFFSET ADDER
ADDER
16 LSBs
16 MSBs
CLK
PHASE ACCUMULATOR REGISTER
R.ENPHAC#
PHASE ACCUMULATOR SECTION
FREQUENCY ADDER
MUX
R.INITPAC#
R.PAC#
R.INHOFR#
PHASE OFFSET REGISTER
R.ENPOREG#
R.PMSEL
ENCODER
MOD0-2
CENTER FREQUENCY REGISTER
R.ENCFREG#
OFFSET FREQUENCY REGISTER
R.ENOFREG#
TIMER INCREMENT REGISTER
R.INITTAC#
R.ENTIREG#
TIMER ACCUMULATOR SECTION
TICO#
PHASE INPUT
PHASE INPUT REG (16)
16 CENTER FREQUENCY INPUT
MSB CENTER FREQUENCY INPUT REG (16)
LSB CENTER FREQUENCY INPUT REG (16)
16 OFFSET FREQUENCY INPUT
MSB OFFSET FREQUENCY INPUT REG (16)
LSB OFFSET FREQUENCY INPUT REG (16)
16 TIMER INCREMENT INPUT
MSB TIMER INCREMENT INPUT REG (16)
LSB TIMER INCREMENT INPUT REG (16)
C0-15
PHEN#
MSCFEN#
LSCFEN#
MSOFEN#
LSOFEN#
MSTIEN#
LSTIEN#
DECODE
A0-2
CS#
WR#
INPUT SECTION
R.ENPOREG#
R.ENOFREG
R.ENCFREG
R.ENPHAC
R.ENTIREG
R.INHOFR
R.INITPAC
R.PMSEL
R.PACI
R.INITTAC
ENPOREG#
ENOFREG
ENCFREG
ENPHAC
ENTIREG
INHOFR
INITPAC
PMSEL
PACI
INITTAC
CLK

FIGURE 1

clock enable of the Center Frequency Register; this register then gets loaded on the following rising edge of CLK. The contents of the input registers are downloaded to the control registers every clock if the control inputs are enabled.

Phase Accumulator Section

The Phase Accumulator adds the 32 bit output of the Frequency Adder with the contents of a 32 bit Phase Accumulator Register on every clock cycle. When the sum causes the adder to overflow, the accumulation continues with the least significant 32 bits of the result.

Initializing the Phase Accumulator Register is done by putting a low on the INITPAC# and ENPHAC# lines. This zeroes the feedback path to the accumulator, so that the register is loaded with the current value of the Frequency Adder on the next clock.

The frequency of the quadrature outputs is based on the number of clock cycles required to step from 0 to full scale. The number of steps required for this transition depends on the phase increment calculated by the frequency adder. For example, if the Center and Offset Frequency registers are programmed such that the output of the Frequency Adder is 4000 0000 hex, the Phase Accumulator will step the phase from 0 to 360 degrees every 4 clock cycles. Thus, for a 30 MHz CLK, the quadrature outputs will have a frequency of 30/4 MHz or 7.5MHz. In general, the frequency of the quadrature output is determined by N x FCLK/2^{32}, where N is the output of the Frequency Adder and FCLK is the frequency of CLK.

The Frequency Adder sums the contents of both the Center and Offset Frequency Registers to produce a phase increment. By enabling INHOFR#, the output of the Offset Frequency Register is disabled so that the output frequency is determined from the Center Frequency Register alone. For 8FSK modems, INHOFR# can be asserted/ de-asserted to toggle the quadrature outputs between two programmed frequencies. Note: enabling/disabling INHOFR# preserves the contents of the Offset Frequency Register.

Phase Offset Adder

The output of the Phase Accumulator goes to the Phase Offset Adder, which adds the 16 bit contents of the Phase Offset Register to the 16 MSB's of the phase. The resulting 32-bit number forms the instantaneous phase which is fed to the Sine/Cosine Section.

The user has the option of loading the Phase Offset Registers with the contents of the Phase Input Register or the MOD0-2 inputs depending on the state of PMSEL. When PMSEL is high, the contents of the Phase Input Register are loaded. If PMSEL is low, MOD0-2 encode the upper 3 bits of the Phase Offset Register while the lower 13 bits are cleared. The MOD0-2 inputs simplify PSK modulation by providing a 3 input interface to phase modulate the carrier as shown in Table 2. The control input ENPOREG# acts as a clock enable and must be low to enable clocking of data into the Phase Offset Register.

TABLE 2

MOD2-0 DECODING			
MOD2	MOD1	MOD0	PHASE SHIFT (DEGREES)
0	0	0	0
0	0	1	45
0	1	0	90
0	1	1	135
1	0	0	270
1	0	1	315
1	1	0	180
1	1	1	225

Timer Accumulator Section

The Timer Accumulator consists of a register which is incremented on every clock. The amount by which it increments is loaded into the Timer Increment Input Registers and is latched into the Timer Increment Register on rising edges of CLK while ENTIREG# is low. The output of the Timer Accumulator is the accumulator carry out, TICO#. TICO# can be used as a timer to enable the periodic sampling of the output of the NCO-16. The number programmed into this register equals (2^{32} x CLK period)/ (desired time interval).

Sine/Cosine Section

The Sine/Cosine Section (Figure 2) converts the instantaneous phase from the PFCS Section into the appropriate amplitude values for the sine and cosine outputs. It takes the most significant 20 bits of the PFCS output and passes them through a Sine/Cosine look up to form the 16 bit quadrature outputs. The sine and cosine values are computed to reduce the amount of ROM needed. The magnitude of the error in the computed value of the complex vector is less than -90.2dB. The error in the sine or cosine alone is approximately 2dB better. The 20 bit phase word maps into 2π radians so that the angular resolution is $(2\pi)/2^{20}$. An address of zero corresponds to 0 radians and an address of hex FFFFF corresponds to $2\pi-((2\pi)/2^{20})$ radians. The outputs of the Sine/Cosine Section are two's complement sine and cosine values. The ROM contents have been scaled by $(2^{16}-1)/(2^{16}+1)$ for symmetry about zero.

To simplify interfacing with D/A converters, the format of the sine/cosine outputs may be changed to offset binary by enabling BINFMT#. When BINFMT# is enabled, The MSB of the Sine and Cosine outputs (SIN15 and COS15 when the outputs are in parallel mode) are inverted. Depending upon the state of BINFMT#, the output is centered around midscale and ranges from 8001H to 7FFFH (two's complement mode) or 0001H to FFFFH (offset binary mode).

Serial output mode may is chosen by enabling PAR/SER#. In this mode the user loads the output shift registers with Sine/Cosine ROM output by enabling ENPHAC#. After ENPHAC# goes inactive the data is shifted out serially. For example, to clock out one 16 bit sine/cosine output, ENPHAC# would be active for one cycle to load the output shift register, and would then go inactive for the following 15 cycles to clock the remaining bits out. Output bit streams are provided in formats with either MSB first or LSB first. The MSB first format is available on the SIN15 and COS15 output pins. The LSB first format is available on the SIN0 and COS0 output pins. In MSB first format, zero's follow the LSB if a new output word is not loaded into the shift register. In LSB first format, the sine extension bit follows the MSB if a new data word is not loaded. The output signal DACSTRB# is provided to signal the first bit of a new output word is valid (Figure 3). Note: all unused pins of SIN0-15 and COS0-15 should be left floating.

A test mode is supplied which enables the user to access the phase input to the Sine/Cosine ROM. If TEST and PAR/ SER# are both high, the 28 MSB's of the phase input to the Sine/ Cosine Section are made available on SIN0-15 and COS4-15. The SIN0-15 outputs represent the MSW of the address.

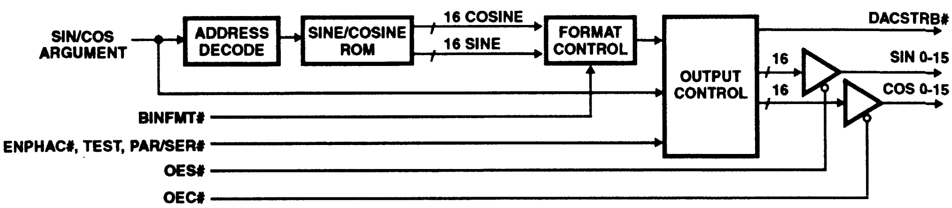


FIGURE 2. SINE/COSINE BLOCK DIAGRAM

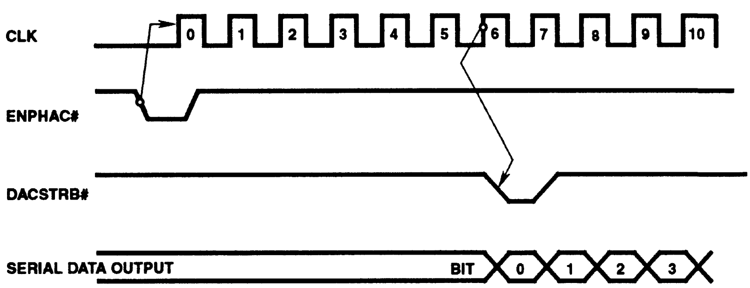


FIGURE 3. SERIAL OUTPUT I/O TIMING DIAGRAM

Absolute Maximum Ratings

Supply Voltage	+8.0V
Input, Output or I/O Voltage Applied	GND -0.5V to V_{CC} +0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	2.3W (PLCC), 2.9W (PGA)
θ_{jc}	11.3°C/W (PLCC), 10.0°C/W (PGA)
θ_{ja}	34.0°C/W (PLCC), 36°C/W (PGA)
Component Count	75,000 Transistors
Junction Temperature	+150°C (PLCC), +175°C (PGA)
Lead Temperature (Soldering, Ten Seconds)	+300°C
ESD Classification	Class 1

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range	+4.75V to +5.25V
Operating Temperature Range	0°C to +70°C

D.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0	-	V	V_{CC} = 5.25V
V_{IL}	Logical Zero Input Voltage	-	0.8	V	V_{CC} = 4.75V
V_{IHC}	High Level Clock Input	3.0	-	V	V_{CC} = 5.25V
V_{ILC}	Low Level Clock Input	-	0.8	V	V_{CC} = 4.75V
V_{OH}	Output HIGH Voltage	2.6	-	V	I_{OH} = -400µA, V_{CC} = 4.75V
V_{OL}	Output LOW Voltage	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.75V
I_I	Input Leakage Current	-10	10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V
I_O	I/O Leakage Current	-10	10	µA	V_{OUT} = V_{CC} or GND, V_{CC} = 5.25V
I_{CCSB}	Standby Power Supply Current	-	500	µA	V_{IN} = V_{CC} or GND V_{CC} = 5.25V, Note 3
I_{CCOP}	Operating Power Supply Current	-	180	mA	f = 25.6MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.25V, Notes 1 and 3

Capacitance (T_A = +25°C, Note 2)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	-	10	pF	FREQ = 1MHz, V_{CC} = Open, All measurements are referenced to device ground
C_O	Output Capacitance	-	10	pF	

NOTES:

1. Power supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 7mA/MHz.
2. Not tested, but characterized at initial design and at major process/design changes.
3. Output load per test load circuit with switch open and C_L = 40pF.

5

SIGNAL SYNTHESIZERS

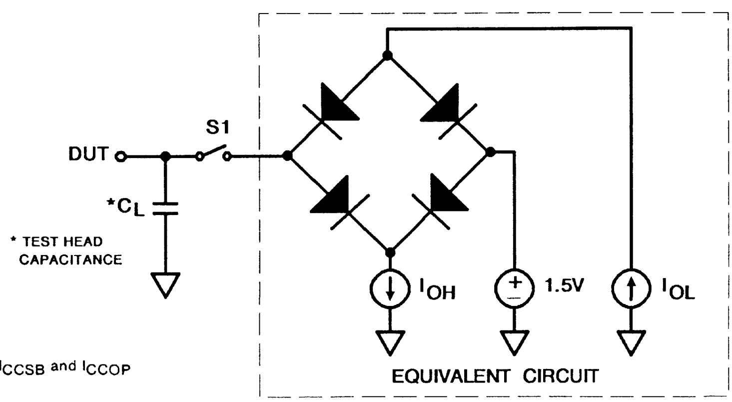
A.C. Electrical Specifications V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C (Note 1)

SYMBOL	PARAMETER	25.6MHz MIN	25.6MHz MAX	33MHz MIN	33MHz MAX	COMMENTS
T_{CP}	CLK Period	39	-	30	-	ns
T_{CH}	CLK High	15	-	12	-	ns
T_{CL}	CLK Low	15	-	12	-	ns
T_{WP}	WR# Period	39	-	30	-	ns
T_{WH}	WR# High	15	-	12	-	ns
T_{WL}	WR# Low	15	-	12	-	ns
T_{AWS}	Set-up Time A0-2, CS# to WR# Going High	13	-	13	-	ns
T_{AWH}	Hold Time A0-2, CS# from WR# Going High	1	-	1	-	ns
T_{CWS}	Set-up Time C0-15 to WR# Going High	15	-	15	-	ns
T_{CWH}	Hold Time C0-15 from WR# Going High	0	-	0	-	ns
T_{WC}	Set-up Time WR# High to CLK High	16	-	12	-	ns, Note 2
T_{MCS}	Set-up Time MOD0-2 to CLK Going High	15	-	15	-	ns
T_{MCH}	Hold Time MOD0-2 from CLK Going High	0	-	0	-	ns
T_{ECS}	Set-up Time ENPOREG#, ENOFREG#, ENCFREG#, ENPHAC#, ENTIREG#, INHOFR#, PMSEL#, INITPAC#, BINFMT#, TEST, PAR/SER#, PACI#, INITTAC# to CLK Going High	12	-	12	-	ns
T_{ECH}	Hold Time ENPOREG#, ENOFREG#, ENCFREG#, ENPHAC#, ENTIREG#, INHOFR#, PMSEL#, INITPAC#, BINFMT#, TEST,PAR/SER# , PACI#, INITTAC# from CLK Going High	0	-	0	-	ns
T_{DO}	CLK to Output Delay SIN0-15, COS0-15, TICO#	-	18	-	15	ns
T_{DSO}	CLK to Output Delay DACSTRB#	2	18	2	15	ns
T_{OE}	Output Enable Time	-	12	-	12	ns
T_{OD}	Output Disable Time	-	15	-	15	ns, Note 3
T_{RF}	Output Rise, Fall Time	-	8	-	8	ns, Note 3

NOTES:

1. A.C. testing is performed as follows: Input levels (CLK Input) 4.0V and 0V; Input levels (all other inputs) 0V and 3.0V; Timing reference levels (CLK) 2.0V; All others 1.5V. Output load per test load circuit with switch closed and C_L = 40 pF. Output transition is measured at $V_{OH} \geq 1.5V$ and $V_{OL} \leq 1.5V$.
2. If ENOFREG#, ENCFREG#, ENTIREG#, OR ENPOREG# are active, care must be taken to not violate set-up and hold times to these registers when writing data into the chip via the C0-15 port.
3. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.

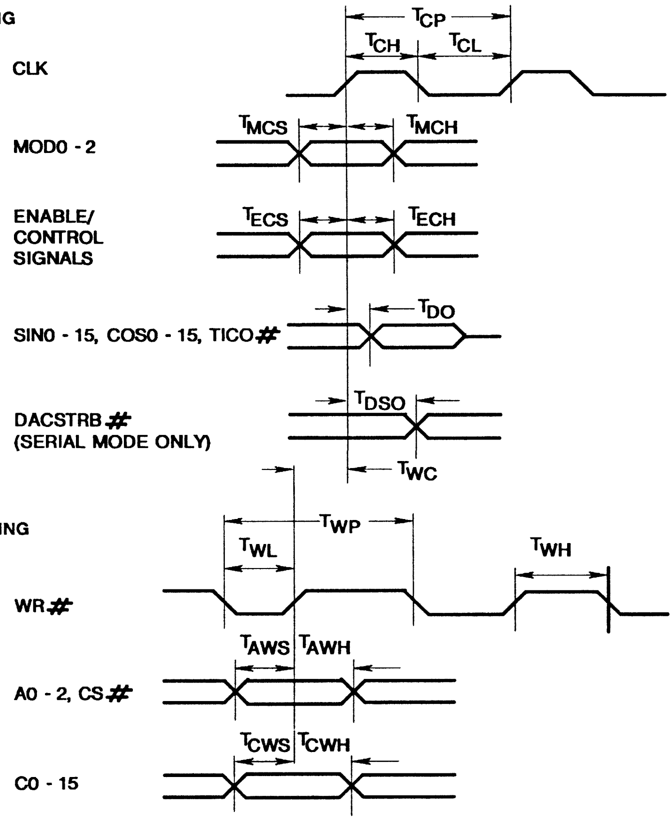
A.C. Test Load Circuit



Switch S1 open for I_{CCSB} and I_{CCOP}

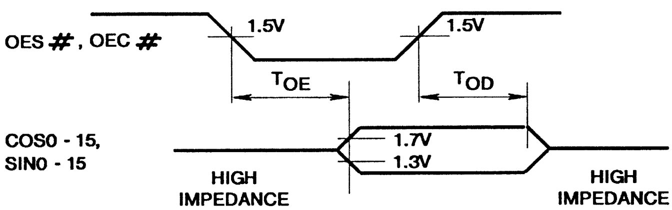
Waveforms

SYNCHRONOUS TIMING

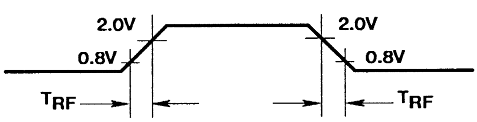


ASYNCHRONOUS TIMING

OUTPUT ENABLE, DISABLE TIMING



OUTPUT RISE AND FALL TIMES



HARRIS SEMICONDUCTOR

HSP45106/883

January 1994

16-Bit Numerically Controlled Oscillator

Features

- **This Circuit Is Processed In Accordance to MIL-STD-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **25.6MHz Clock Rate**
- **32-Bit Center and Offset Frequency Control**
- **16-Bit Phase Control**
- **8 Level PSK Supported Through Three Pin Interface**
- **Simultaneous 16-Bit Sine and Cosine Outputs**
- **Output In Two's Complement or Offset Binary**
- **<0.006Hz Tuning Resolution at 25.6MHz**
- **Serial or Parallel Outputs**
- **Spurious Frequency Components < -90dBc**
- **16-Bit Microprocessor Compatible Control Interface**

Applications

- **Direct Digital Synthesis**
- **Quadrature Signal Generation**
- **Modulation - FM, FSK, PSK (BPSK, QPSK, 8PSK)**
- **Precision Signal Generation**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP45106GM-25/883	-55°C to +125°C	85 Lead PGA

Description

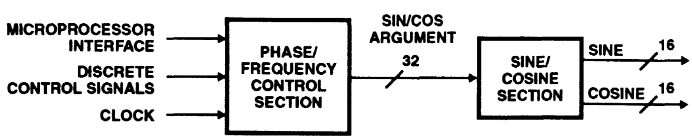
The Harris HSP45106/883 is a high performance 16-bit quadrature numerically controlled oscillator (NCO16). The NCO16 simplifies applications requiring frequency and phase agility such as frequency-hopped modems, PSK modems, spread spectrum communications, and precision signal generators. As shown in the block diagram, the HSP45106/883 is divided into a Phase/Frequency Control Section (PFCS) and a Sine/Cosine Section.

The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The frequency resolution is 32-bits, which provides for resolution of better than 0.006Hz at 25.6MHz. User programmable center frequency and offset frequency registers give the user the capability to perform phase coherent switching between two sinusoids of different frequencies. Further, a programmable phase control register allows for phase control of better than 0.006°. In applications requiring up to 8 level PSK, three discrete inputs are provided to simplify implementation.

The output of the PFCS is a 32-bit phase argument which is input to the sine/cosine section for conversion into sinusoidal amplitude. The outputs of the sine/cosine section are two 16-bit quadrature signals. The spurious free dynamic range of this complex vector is greater than 90dBc.

For added flexibility when using the NCO16 in conjunction with DAC's, a choice of either parallel of serial outputs with either two's complement or offset binary encoding is provided. In addition, a synchronization signal is available which signals serial word boundaries.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2815.2**

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output Voltage Applied .... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering, Ten Seconds) .... +300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic PGA Package	36.0°C/W	11.6°C/W

Maximum Package Power Dissipation at +125°C
Ceramic PGA Package .... 1.39 Watt
Gate Count .... 18,750 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range .... -55°C to +125°C

TABLE 1. HSP45106/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	+10	µA
Output Leakage Current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	+10	µA
Clock Input High	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V, (Note 4)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 25.6MHz V_{CC} = 5.5V (Notes 2, 4)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	205	mA
Functional Test	FT	(Note 3)	7, 8	-55°C ≤ T_A ≤ +125°C	-	-	-

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 8mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, V_{OH} ≥ 1.5V, V_{OL} ≤ 1.5V, V_{IHC} = 3.4V, and V_{ILC} = 0.4V.
4. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS -25 (25.6MHz) MIN	MAX	UNITS
CLK Period	T_{CP}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	39	-	ns
CLK High	T_{CH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	ns
CLK Low	T_{CL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	ns
WR# Period	T_{WP}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	39	-	ns
WR# High	T_{WH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	ns
WR# Low	T_{WL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	ns
Set-up Time A0-2, CS# to WR# Going High	T_{AWS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	13	-	ns
Hold Time A0-2, CS# from WR# Going High	T_{AWH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	2	-	ns
Set-up Time C0-15 to WR# Going High	T_{CWS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	ns
Hold Time C0-15 from WR# Going High	T_{CWH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	1	-	ns
Set-up Time WR# High to CLK High	T_{WC}	Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	16	-	ns
Set-up Time MOD0-2 to CLK Going High	T_{MCS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	ns
Hold Time MOD0-2 from CLK Going High	T_{MCH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	1	-	ns
Set-up Time ENPOREG#, ENOFREG#, ENCFREG#, ENPHAC#, ENTIREG#, INHOFR#, PMSEL#, INITPAC#, BINFMT#, TEST, PAR/SER#, PACI#, INITTAC# to CLK Going High	T_{ECS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	12	-	ns
Hold Time ENPOREG#, ENOFREG#, ENCFREG#, ENPHAC#, ENTIREG#, INHOFR#, PMSEL#, INITPAC#, BINFMT#, TEST, PAR/SER#, PACI#, INITTAC# from CLK Going High	T_{ECH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	1	-	ns
CLK to Output Delay SIN0-15, COS0-15, TICO#	T_{DO}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	18	ns
CLK to Output Delay DACSTRB#	T_{DSO}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	2	18	ns
Output Enable Time	T_{OE}	Note 2	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	12	ns

NOTES:

1. A.C. Testing: V_{CC} = 4.5V and 5.5V. Inputs are driven to 3.0V for a Logic "1" and 0.0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a Logic "1" and "0". CLK is driven at 4.0V and 0V and measured at 2.0V. Output load per test load circuit with switch closed and C_L = 40pF.
2. Transition is measured at ±200mV from steady state voltage with loading as specified by test load circuit and C_L = 40pF.
3. If ENOFRCTL#, ENCFRCTL#, ENTICTL# or ENPHREG# are active, care must be taken to not violate set-up and hold times to these registers when writing data into the chip via the C0-15 port.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS -25 (25.6MHz) MIN	LIMITS -25 (25.6MHz) MAX	UNITS
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	10	pF
Output Capacitance	C_{OUT}	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	10	pF
Output Disable Delay	T_{OEZ}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	15	ns
Output Rise Time	T_{OR}	From 0.8V to 2.0V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	8	ns
Output Fall Time	T_{OF}	From 2.0V to 0.8V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	8	ns

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Loading is as specified in the test load circuit with switch closed and C_L = 40pF.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Burn-In Circuit

HSP45106/883 PIN GRID ARRAY (PGA)

	11	10	9	8	7	6	5	4	3	2	1	
L	GND	SIN0	SIN1	SIN3	SIN5	SIN4	SIN9	SIN12	SIN13	SIN14	DAC STRB #	L
K	FMT	V_{CC}	CLK	SIN2	V_{CC}	SIN8	SIN10	GND	SIN15	OES #	COS0	K
J	INITPAC #	PAR/ SEL #			SIN6	SIN7	SIN11			OEC #	COS1	J
H	ENPHAC #	PACI #								COS2	COS3	H
G	ENTI REG #	INITT AC #	INHOF R #						COS6	COS4	COS5	G
F	ENCF REG#	ENPO REG#	ENOF REG#			85 LEAD PGA TOP VIEW			COS7	COS8	V_{CC}	F
E	CS#	GND	WR#						COS11	COS10	COS9	E
D	V_{CC}	TEST								GND	COS12	D
C	MOD2	MOD0			C10	C9	C6		INDEX PIN	COS15	COS13	C
B	MOD1	A2	A1	C15	C12	C13	V_{CC}	C4	C1	TICO#	COS14	B
A	PMSEL	A0	GND	C14	C11	C8	C7	C5	C3	C2	C0	A PIN 'A1' ID
	11	10	9	8	7	6	5	4	3	2	1	

PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	C0	F7	B11	MOD1	F13	F9	ENOFREG#	F8	K2	OES#	F14
A2	C2	F7	C1	COS13	$V_{CC}/2$	F10	ENPOREG#	F4	K3	SIN15	$V_{CC}/2$
A3	C3	F7	C2	COS15	$V_{CC}/2$	F11	ENCFREG#	F7	K4	GND	GND
A4	C5	F8	C5	C6	F8	G1	COS5	$V_{CC}/2$	K5	SIN10	$V_{CC}/2$
A5	C7	F8	C6	C9	F10	G2	COS4	$V_{CC}/2$	K6	SIN8	$V_{CC}/2$
A6	C8	F10	C7	C10	F10	G3	COS6	$V_{CC}/2$	K7	V_{CC}	V_{CC}
A7	C11	F10	C10	MOD0	F12	G9	INHOFR#	F11	K8	SIN2	$V_{CC}/2$
A8	C14	F11	C11	MOD2	F14	G10	INITTAC#	F13	K9	CLK	F0
A9	GND	GND	D1	COS12	$V_{CC}/2$	G11	ENTIREG#	F12	K10	V_{CC}	V_{CC}
A10	A0	F8	D2	GND	GND	H1	COS3	$V_{CC}/2$	K11	BINFMT#	F6
A11	PMSEL	F14	D10	TEST	F14	H2	COS2	$V_{CC}/2$	L1	DACSTRB#	$V_{CC}/2$
B1	COS14	$V_{CC}/2$	D11	V_{CC}	V_{CC}	H10	PACI#	F11	L2	SIN14	$V_{CC}/2$
B2	TICO#	$V_{CC}/2$	E1	COS9	$V_{CC}/2$	H11	ENPHAC#	F10	L3	SIN13	$V_{CC}/2$
B3	C1	F7	E2	COS10	$V_{CC}/2$	J1	COS1	$V_{CC}/2$	L4	SIN12	$V_{CC}/2$
B4	C4	F8	E3	COS11	$V_{CC}/2$	J2	OEC#	F14	L5	SIN9	$V_{CC}/2$
B5	V_{CC}	V_{CC}	E9	WR#	F4	J5	SIN11	$V_{CC}/2$	L6	SIN4	$V_{CC}/2$
B6	C13	F11	E10	GND	GND	J6	SIN7	$V_{CC}/2$	L7	SIN5	$V_{CC}/2$
B7	C12	F11	E11	CS#	F6	J7	SIN6	$V_{CC}/2$	L8	SIN3	$V_{CC}/2$
B8	C15	F11	F1	V_{CC}	V_{CC}	J10	PAR/SER#	F13	L9	SIN1	$V_{CC}/2$
B9	A1	F7	F2	COS8	$V_{CC}/2$	J11	INITPAC#	F12	L10	SIN0	$V_{CC}/2$
B10	A2	F10	F3	COS7	$V_{CC}/2$	K1	COS0	$V_{CC}/2$	L11	GND	GND

NOTES:

1. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5V ±0.5V.
4. 0.1µF (min) capacitor between V_{CC} and GND per position.
5. F0 = 100kHz ±10%, F1 = F0/2, F2 = F1/2 . . . , F11 = F10/2, 40% - 60% Duty Cycle.
6. Input voltage limits: V_{IL} = 0.8V Max V_{IH} = 4.5V ±10%

Die Characteristics

DIE DIMENSIONS:
251 x 240 x 19 ±1 mils

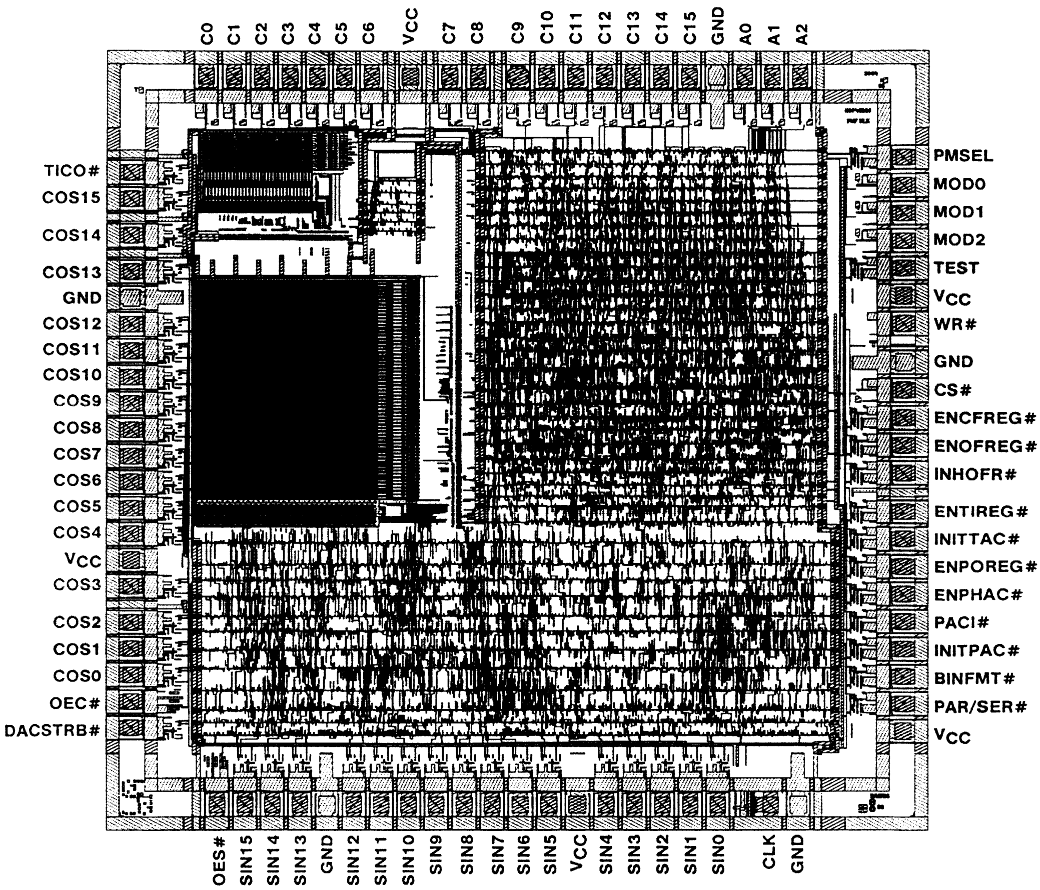
METALLIZATION:
Type: Si-Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY: 0.8×10^5 A/cm^2

Metallization Mask Layout

HSP45106/883



HARRIS SEMICONDUCTOR

HSP45116

Numerically Controlled Oscillator/Modulator

February 1994

Features

- NCO and CMAC on One Chip
- 15MHz, 25.6MHz, 33MHz Versions
- 32-Bit Frequency Control
- 16-Bit Phase Modulation
- 16-Bit CMAC
- 0.008Hz Tuning Resolution at 33MHz
- Spurious Frequency Components < -90dBc
- Fully Static CMOS

Applications

- Frequency Synthesis
- Modulation - AM, FM, PSK, FSK, QAM
- Demodulation, PLL
- Phase Shifter
- Polar to Cartesian Conversions

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP45116VC-15	0°C to +70°C	160 Lead MQFP
HSP45116VC-25	0°C to +70°C	160 Lead MQFP
HSP45116VC-33	0°C to +70°C	160 Lead MQFP
HSP45116GC-15	0°C to +70°C	145 Lead PGA
HSP45116GC-25	0°C to +70°C	145 Lead PGA
HSP45116GC-33	0°C to +70°C	145 Lead PGA
HSP45116TM-15	-55°C to +125°C	156 Lead TAB
HSP45116TM-25	-55°C to +125°C	156 Lead TAB
HSP45116AVC-52	0°C to +70°C	160 Lead MQFP

Description

The Harris HSP45116 combines a high performance quadrature numerically controlled oscillator (NCO) and a high speed 16-bit Complex Multiplier/Accumulator (CMAC) on a single IC. This combination of functions allows a complex vector to be multiplied by the internally generated (cos, sin) vector for quadrature modulation and demodulation. As shown in the block diagram, the HSP45116 is divided into three main sections. The Phase/Frequency Control Section (PFCS) and the Sine/Cosine Section together form a complex NCO. The CMAC multiplies the output of the Sine/Cosine Section with an external complex vector.

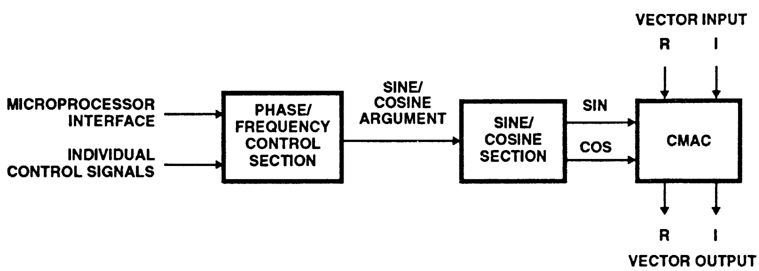
The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The phase resolution of the PFCS is 32-bits, which results in frequency resolution better than 0.008Hz at 33MHz.The output of the PFCS is the argument of the sine and cosine. The spurious free dynamic range of the complex sinusoid is greater than 90dBc.

The output vector from the Sine/Cosine Section is one of the inputs to the Complex Multiplier/Accumulator. The CMAC multiplies this (cos, sin) vector by an external complex vector and can accumulate the result. The resulting complex vectors are available through two 20-bit output ports which maintain the 90dB spectral purity. This result can be accumulated internally to implement an accumulate and dump filter.

A quadrature down converter can be implemented by loading a center frequency into the Phase/Frequency Control Section. The signal to be downconverted is the Vector Input of the CMAC, which multiplies the data by the rotating vector from the Sine/Cosine Section. The resulting complex output is the down converted signal.

The pinout for the TAB package can be obtained by referring to the Metallization Mask Layout of the HSP45116/883 data sheet.

Block Diagram



File Number 2485.4

Pinouts

145 PIN PGA
TOP VIEW

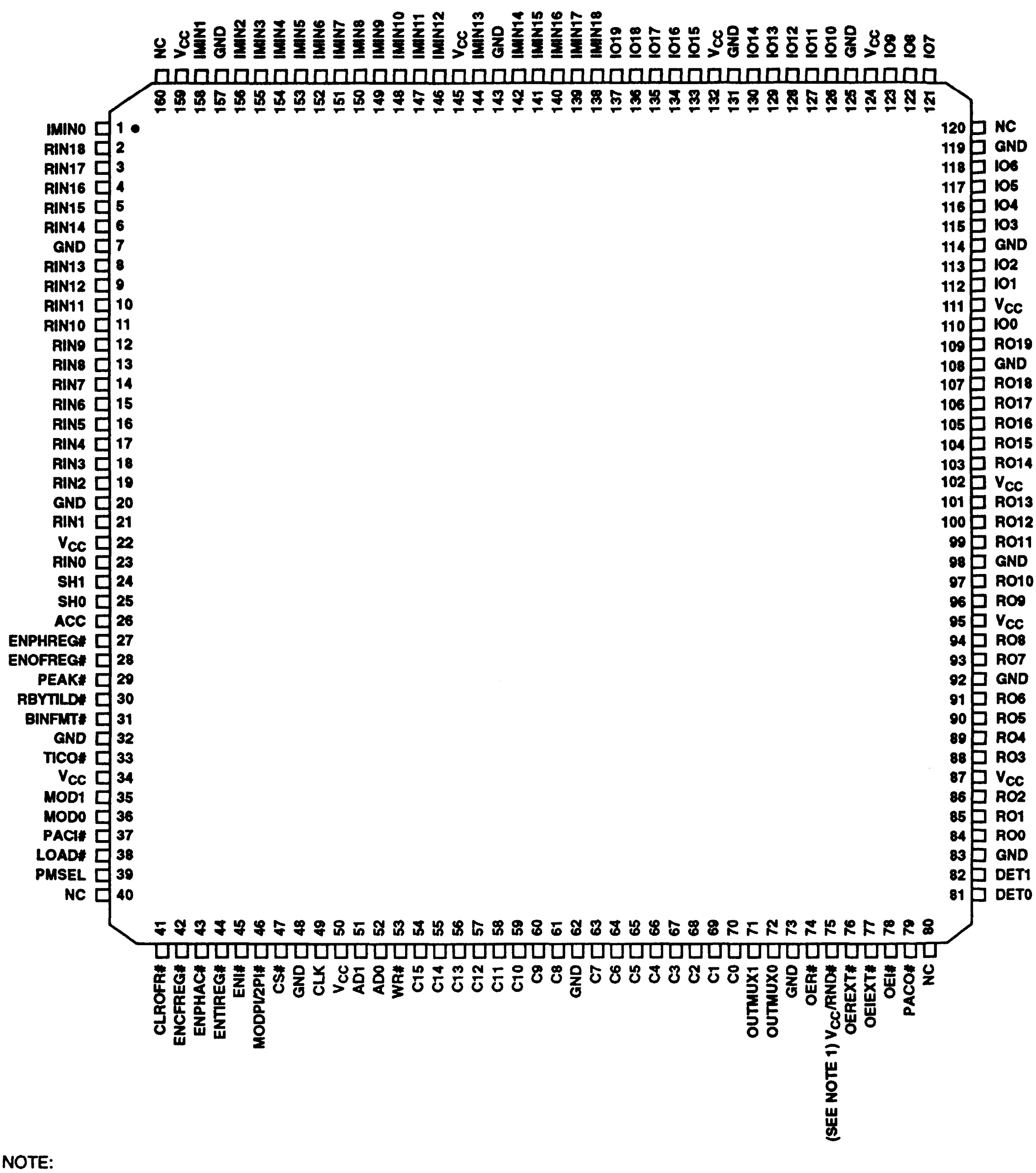
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	VCC	IMIN 4	IMIN 8	IMIN 9	IMIN 11	IMIN 15	IMIN 16	GND	VCC	IO 18	IO 15	IO 12	IO 10	GND	VCC	A
B	GND	IMIN 1	IMIN 5	IMIN 7	IMIN 10	IMIN 13	IMIN 14	IO 19	IO 16	IO 14	IO 11	IO 8	IO 7	IO 5	IO 2	B
C	RIN 15	RIN 18	IMIN 2	IMIN 3	IMIN 6	IMIN 12	IMIN 17	IMIN 18	IO 17	IO 13	IO 9	IO 6	IO 4	IO 1	RO 18	C
D	RIN 13	RIN 17	IMIN 0	INDEX									IO 3	RO 19	RO 17	D
E	RIN 10	RIN 14	RIN 16										IO 0	RO 16	RO 15	E
F	RIN 7	RIN 11	RIN 12										RO 14	RO 13	RO 11	F
G	VCC	RIN 9	RIN 8										RO 9	RO 12	RO 10	G
H	GND	RIN 6	RIN 5										RO 8	RO 7	GND	H
J	RIN 3	RIN 1	RIN 4										RO 5	RO 4	VCC	J
K	RIN 2	RIN 0	SH 1										RO 1	RO 2	RO 6	K
L	SH 0	ACC	RBYTILD #										PACO #	DET 1	RO 3	L
M	ENPHREG #	PEAK #	MOD 1										OEREXT #	OEI #	RO 0	M
N	ENOFREG #	BINFMT #	MOD 0	LOAD #	ENCFREG #	MODPI/2PI #	AD 0	C 14	C 13	C 8	C 2	OUT-MUX 1	OUT-MUX 0	OEIEXT #	DET 0	N
P	TICO #	PACI #	PMSEL	CLROFR #	ENTIREG #	CS #	AD 1	C 15	C 10	C 9	C 6	C 3	C 1	OER #	GND	P
Q	VCC	GND	ENPHAC #	ENI #	CLK	WR #	VCC	GND	C 12	C 11	C 7	C 5	C 4	C 0	VCC	Q
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

BOTTOM VIEW

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VCC	GND	IO 10	IO 12	IO 15	IO 18	VCC	GND	IMIN 16	IMIN 15	IMIN 11	IMIN 9	IMIN 8	IMIN 4	VCC	A
B	IO 2	IO 5	IO 7	IO 8	IO 11	IO 14	IO 16	IO 19	IMIN 14	IMIN 13	IMIN 10	IMIN 7	IMIN 5	IMIN 1	GND	B
C	RO 18	IO 1	IO 4	IO 6	IO 9	IO 13	IO 17	IMIN 18	IMIN 17	IMIN 12	IMIN 6	IMIN 3	IMIN 2	RIN 18	RIN 15	C
D	RO 17	RO 19	IO 3									INDEX	IMIN 0	RIN 17	RIN 13	D
E	RO 15	RO 16	IO 0										RIN 16	RIN 14	RIN 10	E
F	RO 11	RO 13	RO 14										RIN 12	RIN 11	RIN 7	F
G	RO 10	RO 12	RO 9										RIN 8	RIN 9	VCC	G
H	GND	RO 7	RO 8										RIN 5	RIN 6	GND	H
J	VCC	RO 4	RO 5										RIN 4	RIN 1	RIN 3	J
K	RO 6	RO 2	RO 1										SH 1	RIN 0	RIN 2	K
L	RO 3	DET 1	PACO #										RBYTILD #	ACC	SH 0	L
M	RO 0	OEI #	OEREXT #										MOD 1	PEAK #	ENPHREG #	M
N	DET 0	OEIEXT #	OUTMUX 0	OUTMUX 1	C 2	C 8	C 13	C 14	AD 0	MODPI/2PI #	ENCFREG #	LOAD #	MOD 0	BINFMT #	ENOFREG #	N
P	GND	OER #	C 1	C 3	C 6	C 9	C 10	C 15	AD 1	CS #	ENTIREG #	CLROFR #	PMSEL	PACI #	TICO #	P
Q	VCC	C 0	C 4	C 5	C 7	C 11	C 12	GND	VCC	WR #	CLK	ENI #	ENPHAC #	GND	VCC	Q
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Pinouts (Continued)

160 LEAD MQFP
TOP VIEW



NOTE:

1. Pin 75 functions as the round enable (RND#) on the HSP45116A. Pin 75 is V_{CC} on the HSP45116.

Pin Description

NAME	NUMBER	TYPE	DESCRIPTION
V_{CC}	A1, A9, A15, G1, J15, Q1, Q7, Q15		+5 Power supply input
GND	A8, A14, B1, H1, H15, P15, Q2, Q8		Power supply ground input
C0-15	N8-11, P8-13, Q9-14	I	Control input bus for loading phase and frequency data into the PFCS. C15 is the MSB.
AD0-1	N7, P7	I	Address pins for selecting destination of C0-15 data
CS#	P6	I	Chip select (Active Low)
WR#	Q6	I	Write enable. Data is clocked into the register selected by AD0-1 on the rising edge of WR# when the CS# line is low.
CLK	Q5	I	Clock. All registers, except the control registers clocked with WR#,are clocked (when enabled) by the rising edge of CLK.
ENPHREG#	M1	I	Phase register enable. (Active low) Registered on chip by CLK. When active, after being clocked onto chip, ENPHREG# enables the clocking of data into the phase register.
ENOFREG#	N1	I	Frequency offset register enable. (Active Low) Registered on chip by CLK. When active, after being clocked onto chip, ENOFREG# enables clocking of data into the frequency offset register.
ENCFREG#	N5	I	Center frequency register enable. (Active low) Registered on chip by CLK. When active, after being clocked onto chip, ENCFREG# enables clocking of data into the center frequency register.
ENPHAC#	Q3	I	Phase accumulator register enable. (Active low) Registered on chip by CLK. When active, after being clocked onto chip, ENPHAC# enables clocking of the phase accumulator register.
ENTIREG#	P5	I	Time interval control register enable. (Active low) Registered on chip by CLK. When active, after being clocked onto chip, ENTIREG# enables clocking of data into the time accumulator register.
ENI#	Q4	I	Real and imaginary data input register (RIR, IIR) enable. (Active low) Registered on chip by CLK. When active, after being clocked onto chip, ENI# enables clocking of data into the real and imaginary input data register.
MODPI/ 2PI#	N6	I	Modulo $\pi/2\pi$ select. When low, the Sine and Cosine ROMs are addressed modulo 2π (360 degrees). When high, the most significant address bit is held low so that the ROMs are addressed modulo π (180 degrees). This input is registered on chip by clock.
CLROFR#	P4	I	Frequency offset register output zero. (Active low) Registered on chip by CLK. When active, after being clocked onto chip, CLROFR# zeros the data path from the frequency offset register to the frequency adder. New data can still be clocked into the frequency offset register; CLROFR# does not affect the contents of the register.
LOAD#	N4	I	Phase accumulator load control. (Active low) Registered on chip by CLK. Zeroes feedback path in the phase accumulator without clearing the phase accumulator register.
MOD0-1	M3, N3	I	External modulation control bits. When selected with the PMSEL line, these bits add a 0, 90, 180, or 270 degree offset to the current phase in the phase accumulator. The lower 14 bits of the phase control path are set to zero. These bits are loaded into the phase register when ENPHREG# is low.
PMSEL	P3	I	Phase modulation select line. This line determines the source of the data clocked into the phase register. When high, the phase control register is selected. When low, the external modulation pins (MOD0-1) are selected for the most significant two bits and the least significant two bits and the least significant 14 bits are set to zero. This control is registered by CLK.
RBYTILD#	L3	I	ROM bypass, timer load. Active low, Registered by CLK. This input bypasses the sine/ cosine ROM so that the 16 bit phase adder output and lower 16 bits of the phase accumulator go directly to the CMAC's sine and cosine inputs, respectively. It also enables loading of the timer accumulator register by zeroing the feedback in the accumulator.

Pin Description (Continued)

NAME	NUMBER	TYPE	DESCRIPTION
PACI#	P2	I	Phase accumulator carry input. (Active low) A low on this pin causes the phase accumulator to increment by one in addition to the values in the phase accumulator register and frequency adder.
PACO#	L13	O	Phase accumulator carry output. Active low and registered by CLK. A low on this output indicates that the phase accumulator has overflowed, i.e., the end of one sine/cosine cycle has been reached.
TICO#	P1	O	Time interval accumulator carry output. Active low, registered by CLK. This output goes low when a carry is generated by the time interval accumulator. This function is provided to time out control events such as synchronizing register clocking to data timing.
RIN0-18	C1, C2, D1, D2, E1-3, F1-3, G2, G3, H2, H3, J1-3, K1, K2	I	Real input data bus. This is the external real component into the complex multiplier. The bus is clocked into the real input data register by CLK when ENI# is asserted. Two's complement.
IMIN0-18	A2-7, B2-7, C3-8, D3	I	Imaginary input data bus. This is the external imaginary component into the complex multiplier. The bus is clocked into the real input data register by CLK when ENI# is asserted. Two's complement.
SH0-1	K3, L1	I	Shift control inputs. These lines control the input shifters of the RIN and IIN inputs of the complex multiplier. The shift controls are common to the shifters on both of the busses.
ACC	L2	I	Accumulate/dump control. This input controls the complex accumulators and their holding registers. When high, the accumulators accumulate and the holding registers are disabled. When low, the feedback in the accumulators is zeroed to cause the accumulators to load. The holding registers are enabled to clock in the results of the accumulation. This input is registered by CLK.
BINFMT#	N2	I	This input is used to convert the two's complement output to offset binary (unsigned) for applications using D/A converters. When low, bits RO19 and IO19 are inverted from the internal two's complement representation. This input is registered by CLK.
PEAK#	M2	I	This input enables the peak detect feature of the block floating point detector. When high, the maximum bit growth in the output holding registers is encoded and output on the DET0-1 pins. When the PEAK# input is asserted, the block floating point detector output will track the maximum growth in the holding registers, including the data in the holding registers at the time that PEAK# is activated.
OUTMUX0-1	N12, N13	I	These inputs select the data to be output on RO0-19 and IO0-19.
RO0-19	C15, D14, D15 E14, E15, F13-15, G13-15, H13, H14, J13, J14, K13-15, L15, M15	O	Real output data bus. These three state outputs are controlled by OER# and OEREXT#. OUTMUX0-1 select the data output on the bus.
IO0-19	A10-13, B8-15, C9-14, D13, E13	O	Imaginary output data bus.These three state outputs are controlled by OEI# and OEIEXT#. OUTMUX0-1 select the data output on the bus.
DET0-1	N15, L14	O	These output pins indicate the number of bits of growth in the accumulators. While PEAK# is low, these pins indicate the peak growth. The detector examines bits 15-18, real and imaginary accumulator holding registers and bits 30-33 of the real and imaginary CMAC holding registers. The bits indicate the largest growth of the four registers.
OER#	P14	I	Three state control for bits RO0-15. Outputs are enabled when the line is low.
OEREXT#	M13	I	Three state control for bits RO16-19. Outputs are enabled when the line is low.
OEI#	M14	I	Three state control for bits IO0-15. Outputs are enabled when the line is low.
OEIEXT#	N14	I	Three state control for bits IO16-19. Outputs are enabled when the line is low.
RND#	N/A	I	Round Enable (Available on HSP45116A only). This input enables rounding of the output data precision from 9 to 20 bits (see HSP45116A Description and Operation. This input is active "low". This input must be tied either high or low.

Functional Description

The Numerically Controlled Oscillator/Modulator (NCOM) produces a digital complex sinusoid waveform whose amplitude, phase and frequency are controlled by a set of input command words. When used as a Numerically Controlled Oscillator (NCO), it generates 16 bit sine and cosine vectors at a maximum sample rate of 33MHz. The NCOM can be preprogrammed to produce a constant (CW) sine and cosine output for Direct Digital Synthesis (DDS) applications. Alternatively, the phase and frequency inputs can be updated in real time to produce a FM, PSK, FSK, or MSK modulated waveform. The Complex Multiplier/Accumulator (CMAC) can be used to multiply this waveform by an input signal for AM and QAM signals. By stepping the phase input, the output of the ROM becomes an FFT twiddle factor; when data is input to the Vector Inputs (see Block Diagram), the NCOM calculates an FFT butterfly.

As shown in the Block Diagram, the NCOM consists of three parts: Phase and Frequency Control Section (PFCS), Sine/Cosine Generator, and CMAC. The PFCS stores the phase and frequency inputs and uses them to calculate the phase angle of a rotating complex vector. The Sine/Cosine Generator performs a lookup on this phase and outputs the appropriate values for the sine and cosine. The sine and cosine form one set of inputs to the CMAC, which multiplies them by the input vector to form the modulated output.

Phase and Frequency Control Section

The phase and frequency of the internally generated sine and cosine are controlled by the PFCS (Figure 1). The PFCS generates a 32 bit word that represents the current phase of the sine and cosine waves being generated: the Sine/Cosine Argument. Stepping this phase angle from 0 through full scale ($2^{32} - 1$) corresponds to the phase angle of a sinusoid starting at 0° and advancing around the unit circle counterclockwise. The PFCS automatically increments the phase by a preprogrammed amount on every rising edge of the external clock. The value of the phase step (which is the sum of the Center and Offset Frequency Registers) is:

$$\text{Phase Step} = \frac{\text{Signal Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

The PFCS is divided into 2 sections: the Phase Accumulator uses the data on C0-15 to compute the phase angle that is the input to the Sine/Cosine Section (Sine/Cosine Argument); the Time Accumulator supplies a pulse to mark the passage of a preprogrammed period of time.

The Phase Accumulator and Time Accumulator work on the same principle: a 32 bit word is added to the contents of a 32 bit accumulator register every clock cycle; when the sum

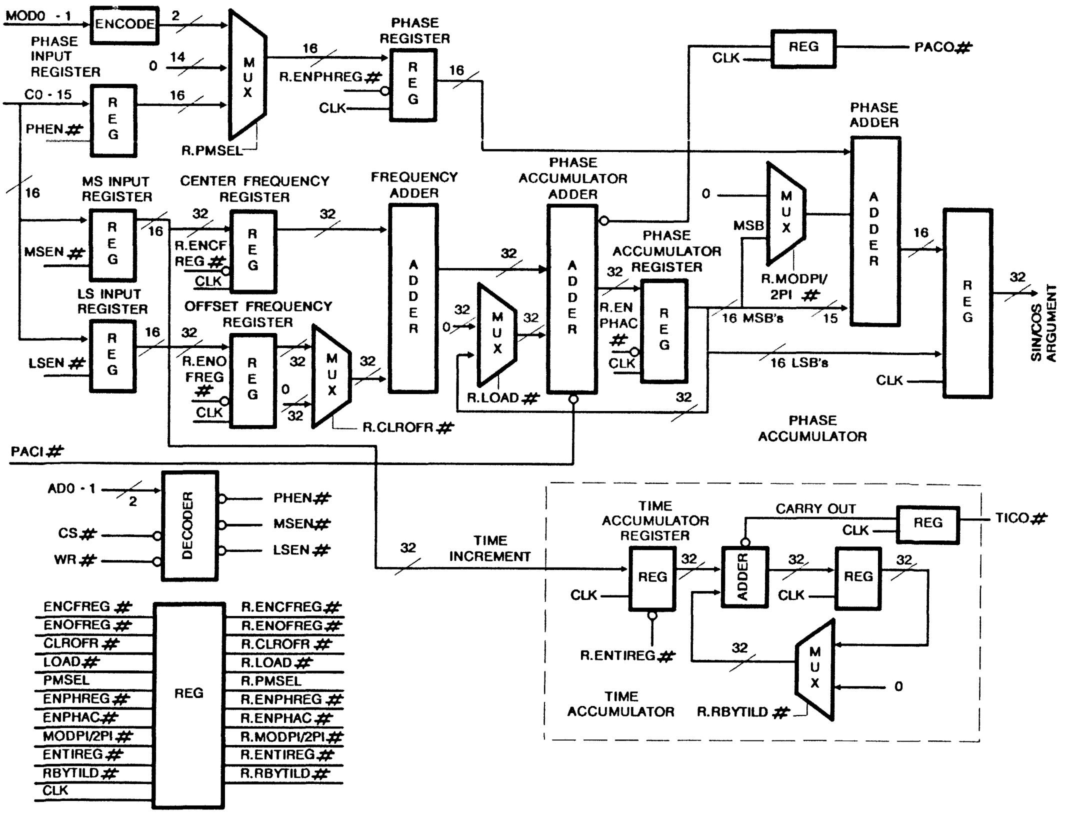


FIGURE 1. PHASE/FREQUENCY CONTROL SECTION BLOCK DIAGRAM

causes the adder to overflow, the accumulation continues with the 32 bits of the adder going into the accumulator register. The overflow bit is used as an output to indicate the timing of the accumulation overflows. In the Time Accumulator, the overflow bit generates TICO#, the Time Accumulator carry out (which is the only output of the Time Accumulator). In the Phase Accumulator, the overflow is inverted to generate the Phase Accumulator Carry Out, PACO#.

The output of the Phase Accumulator goes to the Phase Adder, which adds an offset to the top 16 bits of the phase. This 32 bit number forms the argument of the sine and cosine, which is passed to the Sine/Cosine Generator.

Both accumulators are loaded 16 bits at a time over the C0-15 bus. Data on C0-15 is loaded into one of the three input registers when CS# and WR# are low. The data in the Most Significant Input Register and Least Significant Input Register forms a 32 bit word that is the input to the Center Frequency Register, Offset Frequency Register and Time Accumulator. These registers are loaded by enabling the proper register enable signal; for example, to load the Center Frequency Register, the data is loaded into the LS and MS Input Registers, and ENCFREG# is set to zero; the next rising edge of CLK will pass the registered version of ENCFREG#, R.ENCFREG#, to the clock enable of the Center Frequency Register; this register then gets loaded on the following rising edge of CLK. The contents of the Input Registers will be continuously loaded into the Center Frequency Register as long as R.ENCFREG# is low.

The Phase Register is loaded in a similar manner. Assuming PMSEL is high, the contents of the Phase Input Register is loaded into the Phase Register on every rising clock edge that R.ENPHREG is low. If PMSEL is low, MOD0-1 supply the two most significant bits into the Phase Register (MOD1 is the MSB) and the least significant 14 bits are loaded with 0. MOD0-1 are used to generate a Quad Phase Shift Keying (QPSK) signal (Table 2).

TABLE 1. AD0-1 DECODING

AD1	AD0	CS#	WR#	FUNCTION
0	0	0	↑	Load least significant bits of frequency input
0	1	0	↑	Load most significant bits of frequency input
1	0	0	↑	Load phase register
1	1	X	X	Reserved
X	X	1	X	Reserved

The Phase Accumulator consists of registers and adders that compute the value of the current phase at every clock. It has three inputs: Center Frequency, which corresponds to the carrier frequency of a signal; Offset Frequency, which is the deviation from the Center Frequency; and Phase, which is a 16 bit number that is added to the current phase for PSK modulation schemes. These three values are used by the Phase Accumulator and Phase Adder to form the phase of the internally generated sine and cosine.

The sum of the values in Center and Offset Frequency Registers corresponds to the desired phase increment (modulo 2^{32}) from one clock to the next. For example, loading both registers with zero will cause the Phase Accumulator to add zero to its current output; the output of the PFCS will remain at its current value; i.e., the output of the NCOM will be a DC signal. If a hexadecimal 00000001 is loaded into the Center Frequency Control Register, the output of the PFCS will increment by one after every clock. This will step through every location in the Sine/Cosine Generator, so that the output will be the lowest frequency above DC that can be generated by the NCOM, i.e., the clock frequency divided by 2^{32}. If the input to the Center Frequency Control Register is hex 80000000, the PFCS will step through the Generator with half of the maximum step size, so that frequency of the output waveform will be half of the sample rate.

The operation of the Offset Frequency Control Register is identical to that of the Center Frequency Control Register; having two separate registers allows the user to generate an FM signal by loading the carrier frequency in the Center Frequency Control Register and updating the Offset Frequency Control Register with the value of the frequency offset - the difference between the carrier frequency and the frequency of the output signal. A logic low on CLROFR# disables the output of the Offset Frequency Register without clearing the contents of the register.

TABLE 2. MOD0-1 DECODE

MOD1	MOD0	PHASE SHIFT (DEGREES)
0	0	0
0	1	90
1	0	270
1	1	180

Initializing the Phase Accumulator Register is done by putting a low on the LOAD# line. This zeroes the feedback path to the accumulator, so that the register is loaded with the current value of the phase increment summer on the next clock.

The final phase value going to the Generator can be adjusted using MODPI/2PI# to force the range of the phase to be 0° to 180° (modulo π) or 0° to 360° (modulo 2π). Modulo 2π is the mode used for modulation, demodulation, direct digital synthesis, etc. Modulo π is used to calculate FFTs. This is explained in greater detail in the Applications section.

The Phase Register adds an offset to the output of the Phase Accumulator. Since the Phase Register is only 16 bits, it is added to the top 16 bits of the Phase Accumulator.

The Time Accumulator consists of a register which is incremented on every clock. The amount by which it increments is loaded into the Input Registers and is latched into the Time Accumulator Register on rising edges of CLK while ENTIREG# is low. The output of the Time Accumulator is the accumulator carry out, TICO#. TICO# can be used as a timer to enable the periodic sampling of the output of the NCOM. The number programmed into this register equals 2^{32} x CLK period/desired time interval. TICO# is disabled and its phase is initialized by zeroing the feedback path of the accumulator with RBYTILD#.

Sine/Cosine Section

The Sine/Cosine Section (Figure 2) converts the output of the PFCS into the appropriate values for the sine and cosine. It takes the most significant 20 bits of the PFCS output and passes them through a look up table to form the 16 bit sine and cosine inputs to the CMAC.

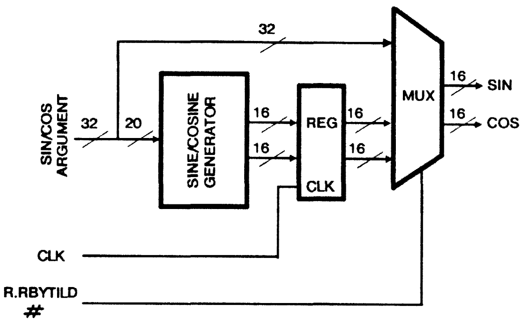


FIGURE 2. SINE/COSINE SECTION

The 20 bit word maps into 2π radians so that the angular resolution is $2\pi/2^{20}$. An address of zero corresponds to 0 radians and an address of hex FFFFF corresponds to $2\pi-(2\pi/2^{20})$ radians. The outputs of the Generator section are 2's complement sine and cosine values. The sine and cosine outputs range from hexadecimal 8001, which represents negative full scale, to 7FFF, which represents positive full scale. Note that the normal range for two's complement numbers is 8000 to 7FFF; the output range of the SIN/COS generator is scaled by one so that it is symmetric about 0.

The sine and cosine values are computed to reduce the amount of ROM needed. The magnitude of the error in the computed value of the complex vector is less than -90.2dB. The error in the sine or cosine alone is approximately 2dB better.

If RBYTILD# is low, the output of the PFCS goes directly to the inputs of the CMAC. If the real and imaginary inputs of the CMAC are programmed to hex 7FFF and 0 respectively, then the output of the PFCS will appear on output bits 0 through 15 of the NCOM with the output multiplexers set to bring out the most significant bits of the CMAC output (OUTMUX = 00). The most significant 16 bits out of the PFCS appears on IOUT0-15 and the least significant bits come out on ROUT0-15.

Complex Multiplier/Accumulator

The CMAC (Figure 3) performs two types of functions: complex multiplication/accumulation for modulation and demodulation of digital signals, and the operations necessary to implement an FFT butterfly. Modulation and demodulation are implemented using the complex multiplier and its associated accumulator; the rest of the circuitry in this section, i.e., the complex accumulator, input shifters and growth detect logic are used along with the complex multiplier/accumulator for FFTs. The complex multiplier performs the complex vector multiplication on the output of the Sine/Cosine Section and the vector represented by the real and imaginary inputs RIN and IIN. The two vectors are combined in the following manner:

ROUT = COS x RIN - SIN x IIN

IOUT = COS x IIN + SIN x RIN

RIN and IIN are latched into the input registers and passed through the shift stages. Clocking of the input registers is enabled with a low on ENI#. The amount of shift on the latched data is programmed with SH0-1 (Table 3). The output of the shifters is sent to the CMAC and the auxiliary accumulators.

TABLE 3. INPUT SHIFT SELECTION

SH1	SH0	SELECTED BITS
0	0	RIN0-15, IMIN0-15
0	1	RIN1-16, IMIN1-16
1	0	RIN2-17, IMIN2-17
1	1	RIN3-18, IMIN3-18

The 33 bit real and imaginary outputs of the Complex Multiplier are latched in the Multiplier Registers and then go through the accumulator section of the CMAC. If the ACC line is high, the feedback to the accumulators is enabled; a low on ACC zeroes the feedback path, so that the next set of real and imaginary data out of the complex multiplier is stored in the CMAC Output Registers.

The data in the CMAC Output Registers goes to the Multiplexer, the output of which is determined by the OUTMUX0- 1 lines (Table 4). BINFMT# controls whether the output of the Multiplexer is presented in two's complement or unsigned format; BINFMT# = 0 inverts ROUT19 and IOUT19 for unsigned output, while BINFMT# = 1 selects two's complement.

TABLE 4. OUTPUT MULTIPLEXER SELECTION

OUT MUX 1	OUT MUX 0	RO16-19	RO0-15	IO16-19	IO0-15
0	0	Real CMAC 31-34	Real CMAC 15-30	Imag CMAC 31-34	Imag CMAC 15-30
0	1	Real CMAC 31-34	0, Real CMAC 0-14	Imag CMAC 31-34	0, Imag CMAC 0-14
1	0	Real Acc 16-19	Real Acc 0-15	Imag Acc 16-19	Imag Acc 0-15
1	1	Reserved	Reserved	Reserved	Reserved

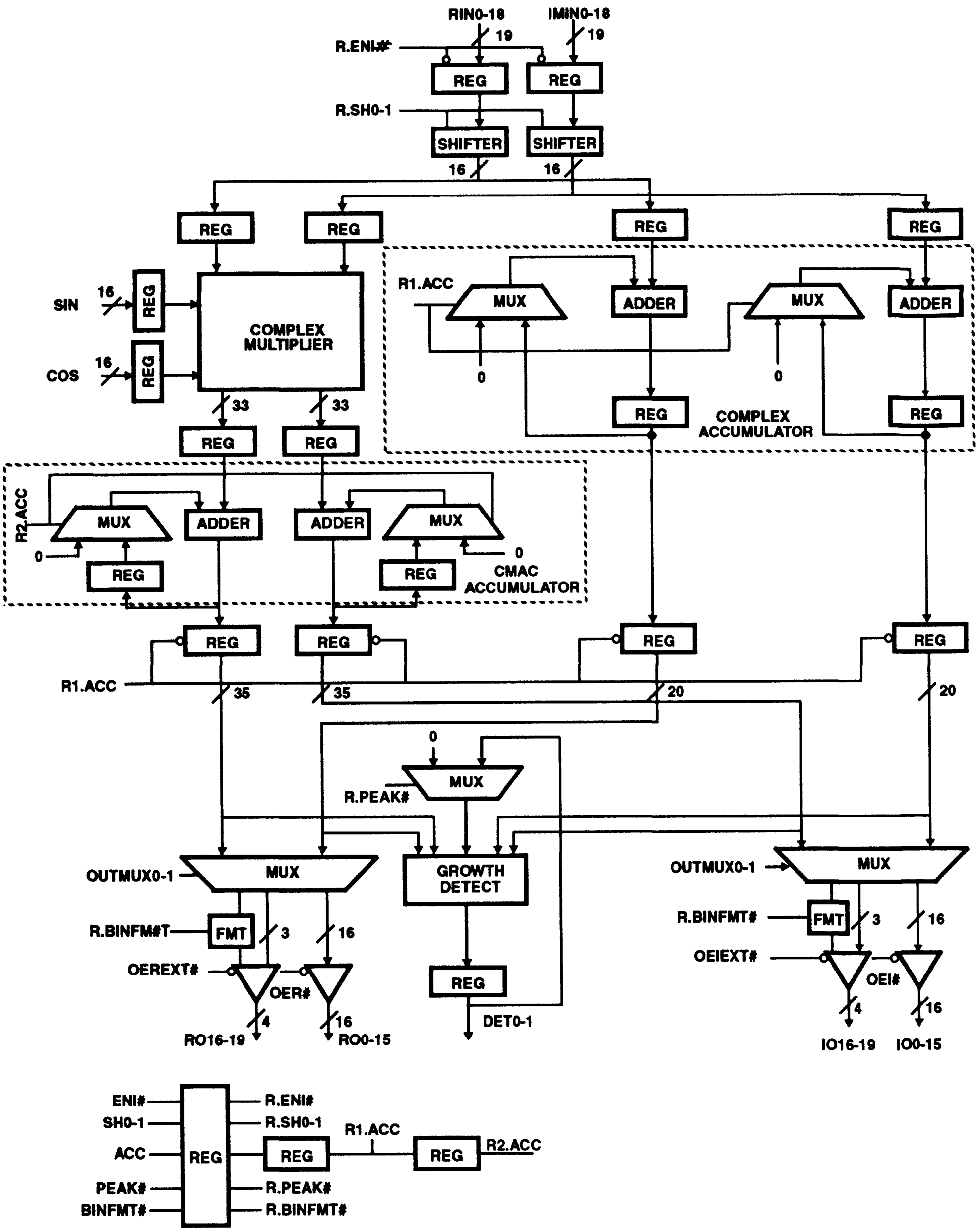


FIGURE 3. COMPLEX MULTIPLIER/ACCUMULATOR; ALL REGISTERS CLOCKED BY CLK

The Complex Accumulator duplicates the accumulator in the CMAC. The input comes from the data shifters, and its 20 bit complex output goes to the Multiplexer. ACC controls whether the accumulator is enabled or not. OUTMUX0-1 determines whether the accumulator output appears on ROUT and IOUT.

The Growth Detect circuitry outputs a two bit value that signifies the amount of growth on the data in the CMAC and Complex Accumulator. Its output, DET0-1, is encoded as shown in Table 5. If PEAK# is low, the highest value of DET0-1 is latched in the Growth Detect Output Register.

The relative weighting of the bits at the inputs and outputs of the CMAC is shown in figure 4. Note that the binary point of the sine, cosine, RIN and IIN is to the right of the most significant bit, while the binary point of RO and IO is to the right of the fifth most significant bit. These CMAC external input and output busses are aligned with each other to facilitate cascading NCOM's for FFT applications.

TABLE 5. GROWTH ENCODING

DET 1	DET 0	NUMBER OF BITS OF GROWTH ABOVE 2^0
0	0	0
0	1	1
1	0	2
1	1	3

SIN/COS INPUT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^0 .	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Radix Point

COMPLEX MULTIPLIER/ACCUMULATOR INPUT (RIN, IIN)
SH = 00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^0 .	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Radix Point

COMPLEX MULTIPLIER/ACCUMULATOR OUTPUT (RO, IO)
OUTMUX = 00

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^4	2^3	2^2	2^1	2^0 .	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Radix Point

COMPLEX MULTIPLIER/ACCUMULATOR OUTPUT (RO, IO)
OUTMUX = 01

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^4	2^3	2^2	2^1	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	0

COMPLEX ACCUMULATOR OUTPUT (RO, IO)
OUTMUX = 10

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^4	2^3	2^2	2^1	2^0 .	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Radix Point

FIGURE 4. BIT WEIGHTING

HSP45116A Description and Operation

The operation of the HSP45116A is identical to the HSP45116 with the exception of a programmable rounding option added for the data outputs. The added functionality was acheived by using one of the HSP45116's reserved configuration registers to specify rounding precision and replacing a V_{CC} pin with a round enable (RND#) input. When RND# is "high", rounding is disabled, and the HSP45116A functions as a pin-for-pin equivatent of the HSP45116. When RND# is active "low" rounding is enabled. The RND# input replaces V_{CC} on PIN 75 of the 160 Lead MQFP package as seen in the pinout diagram.

The Round Control Register is loaded by placing the round control value on C15-0, setting AD1-0 = 11, setting CS# = 0, and forcing a low to high transition on the WR# input. The rounding operation is determined by the least significant 8 bits loaded into the control register as shown in Table 6. The least significant four bits (C3-0) loaded into the register govern rounding of the real and imaginary outputs of the Complex Accumulator (ACC). The next more significant four bits (C7-4) govern the rounding of the complex outputs of the complex multiply accumulator (CMAC). The real and imaginary outputs from the CMAC or ACC are rounded to the same precision. The rounding is perform by adding a "one" to the bit position below the least signifcant bit desired in the output. For example, for a configuration that rounds to the most signifcant 20 bits of the CMAC output, a "one" would be added to bit position 2^{-14} (See Figure 4 for output bit weightings).

TABLE 6. ROUNDING CONTROL

ROUND CONTROL REGISTER			
C15-8	C7-4	C3-0	
UNUSED	CMAC ROUNDING	ACC ROUNDING	ROUNDING OPERATION
XXXXXXXX	0000	0000	No Rounding
XXXXXXXX	0001	0001	CMAC outputs rounded to most significant 20 bits, bit positions -2^4 to 2^{-15} ACC outputs rounded to most significant 20 bits, bit positions -2^4 to 2^{-15}
XXXXXXXX	0010	0010	CMAC outputs rounded to most significant 19 bits, bit positions -2^4 to 2^{-14} ACC outputs rounded to most significant 19 bits, bit positions -2^4 to 2^{-14}
XXXXXXXX	0011	0011	CMAC outputs rounded to most significant 18 bits, bit positions -2^4 to 2^{-13} ACC outputs rounded to most significant 18 bits, bit positions -2^4 to 2^{-13}
XXXXXXXX	0100	0100	CMAC outputs rounded to most significant 17 bits, bit positions -2^4 to 2^{-12} ACC outputs rounded to most significant 17 bits, bit positions -2^4 to 2^{-12}
XXXXXXXX	0101	0101	CMAC outputs rounded to most significant 16 bits, bit positions -2^4 to 2^{-11} ACC outputs rounded to most significant 16 bits, bit positions -2^4 to 2^{-11}
XXXXXXXX	0110	0110	CMAC outputs rounded to most significant 15 bits, bit positions -2^4 to 2^{-10} ACC outputs rounded to most significant 15 bits, bit positions -2^4 to 2^{-10}
XXXXXXXX	0111	0111	CMAC outputs rounded to most significant 14 bits, bit positions -2^4 to 2^{-9} ACC outputs rounded to most significant 14 bits, bit positions -2^4 to 2^{-9}
XXXXXXXX	1000	1000	CMAC outputs rounded to most significant 13 bits, bit positions -2^4 to 2^{-8} ACC outputs rounded to most significant 13 bits, bit positions -2^4 to 2^{-8}
XXXXXXXX	1001	1001	CMAC outputs rounded to most significant 12 bits, bit positions -2^4 to 2^{-7} ACC outputs rounded to most significant 12 bits, bit positions -2^4 to 2^{-7}
XXXXXXXX	1010	1010	CMAC outputs rounded to most significant 11 bits, bit positions -2^4 to 2^{-6} ACC outputs rounded to most significant 11 bits, bit positions -2^4 to 2^{-6}
XXXXXXXX	1011	1011	CMAC outputs rounded to most significant 10 bits, bit positions -2^4 to 2^{-5} ACC outputs rounded to most significant 10 bits, bit positions -2^4 to 2^{-5}
XXXXXXXX	1100	1100	CMAC outputs rounded to most significant 9 bits, bit positions -2^4 to 2^{-4} ACC outputs rounded to most significant 9 bits, bit positions -2^4 to 2^{-4}
XXXXXXXX	1101-1111	1101-1111	Undefined

Applications

The NCOM can be used for Amplitude, Phase and Frequency modulation, as well as in variations and combinations of these techniques, such as QAM. It is most effective in applications requiring multiplication of a rotating complex sinusoid by an external vector. These include AM and QAM modulators and digital receivers. The NCOM implements AM and QAM modulation on a single chip, and is a element in demodulation, where it performs complex down conversion. It can be combined with the Harris HSP43220 Decimating Digital Filter to form the front end of a digital receiver.

Modulation/Demodulation

Figure 5 shows a block diagram of an AM modulator. In this example, the phase increment for the carrier frequency is loaded into the center frequency register, and the modulating input is clocked into the real input of the CMAC, with the imaginary input set to 0. The modulated output is obtained at the real output of the CMAC. With a sixteen bit, two's complement signal input, the output will be a 16 bit real number, on ROUT0-15 (with OUTMUX = 00).

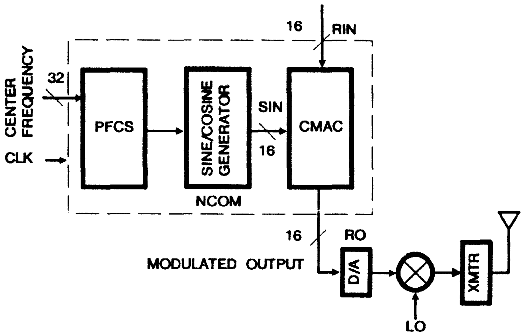


FIGURE 5. AMPLITUDE MODULATION

By replacing the real input with a complex vector, a similar setup can generate QAM signals (Figure 6). In this case, the carrier frequency is loaded into the center frequency register as before, but the modulating vector now carries both amplitude and phase information. Since the input vector and the internally generated sine and cosine waves are both 16 bits, the number of states is only limited by the characteristics of the transmission medium and by the analog electronics in the transmitter and receiver.

The phase and amplitude resolution for the Sine/Cosine section (16 bit output), delivers a spectral purity of greater than 90dBc. This means that the unwanted spectral components due to phase uncertainty (phase noise) will be greater than 90dB below the desired output (dBc, decibels below the carrier). With a 32 bit phase accumulator in the Phase/

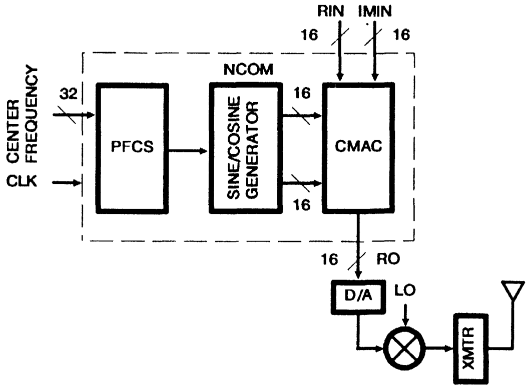


FIGURE 6. QUADRATURE AMPLITUDE MODULATION (QAM)

Frequency Control Section, the frequency tuning resolution equals the clock frequency divided by 2^{32}. For example, a 25MHz clock gives a tuning resolution of 0.006Hz.

The NCOM also works with the HSP43220 Decimating Digital Filter to implement down conversion and low pass filtering in a digital receiver (Figure 7). The NCOM performs complex down conversion on the wideband input signal by multiplying the input vector and the internally generated complex sinusoid. The resulting signal has components at twice the center frequency and at DC. Two HSP43220's, one each on the real and imaginary outputs of the HSP45116, perform low pass filtering and decimation on the down converted data, resulting in a complex baseband signal.

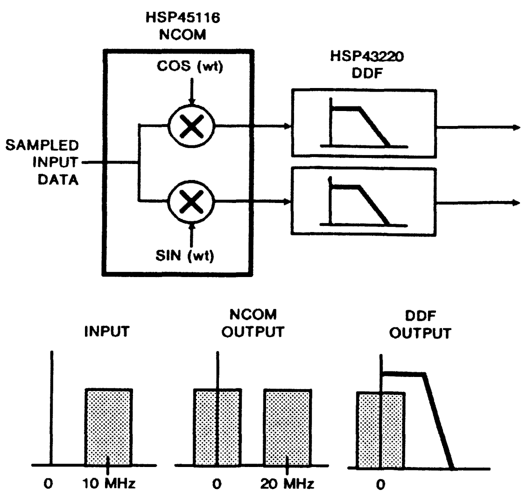


FIGURE 7. CHANNELIZED RECEIVER CHIP SET

FFT Butterfly

Figure 8 shows a Fast Fourier Transform (FFT) implementation. The FFT is a highly efficient way of calculating the Discrete Fourier Transform [1]. The basic building block in FFTs is called the butterfly. The butterfly calculation involves adding complex numbers and multiplying by complex sinusoids. The Phase/Frequency Control Section and Sine/Cosine Generator provide the complex sinusoids and the CMAC performs the complex multiplies and adds.

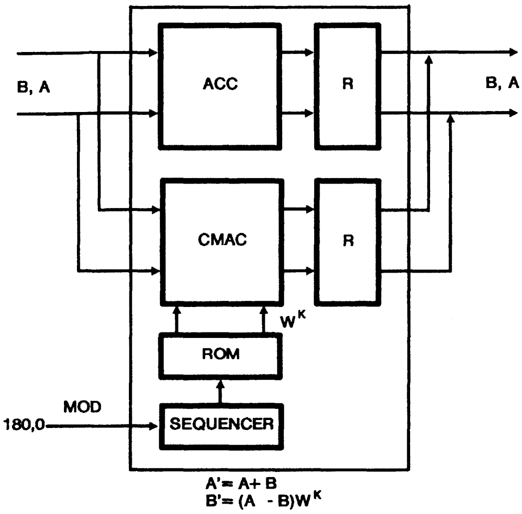


FIGURE 8. RADIX-2 FFT BUTTERFLY

The NCOM circuit shown implements the butterfly shown in Figure 9. The two complex inputs A and B produce two complex outputs A' and B' using the equations A' = A + B, B' = (A - B)W^k where $W^k = e^{-jwk} = \cos(wk) + j\sin(wk)$. Two clock cycles are required to calculate the butterfly. A is clocked into the chip first and then B is clocked in. The complex accumulator in the CMAC section adds A and B. The CMAC calculates (A - B)W^k as $AW^k + B(-W^k)$. $-W^k$ is generated by phase shifting the ROM address 180 degrees using the phase modulation inputs. For radix-2 decimation in frequency FFTs, the phase of the complex sinusoid starts at 0 degrees and increments by a fixed step size (for each pass) after each butterfly. The phase/frequency section is initialized to 0 degrees and the frequency control loaded with the appropriate phase step size for the pass. The resulting words, A' and B', are held in output registers and multiplexed through the output pins for writing to memory. Using a single NCOM clocked at 25MHz, a 1024 point radix-2 FFT can be computed in (CLK period) x ($N\log_2 N$), or 410 microseconds.

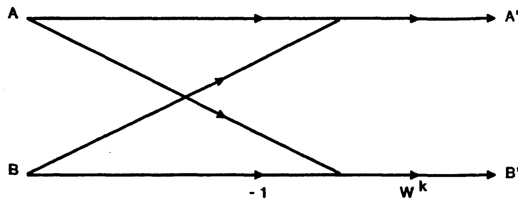


FIGURE 9. DECIMATION IN FREQUENCY BUTTERFLY

Circuitry is included to implement block floating point FFTs. In block floating point, an exponent is generated for an entire block of data. To implement block floating point, the maximum bit growth during a set of calculations is detected. The number of bits of growth is used to adjust the block's exponent and to scale the block on the next set of calculations to maintain a desired number of bits of precision. This technique requires less memory than true floating point and yields better performance than fixed point implementations, though its resolution does not meet that of true floating point implementations.

References

[1] Oppenheim, A. V. and Schafer, R. W., *Discrete Time Signal Processing*, Prentice Hall

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output or I/O Voltage Applied ...... GND -0.5V to V_{CC} +0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature
MQFP .... +150°C
PGA .... +175°C
Lead Temperature (Soldering 10s) .... +150°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
MQFP Package	22.0°C/W	7.7°C/W
PGA Package	23.1°C/W	8.3C/W

Maximum Package Power Dissipation
MQFP 3.6W
PGA 4.55W
Component Count .... 103,000 Transistors

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.75V to +5.25V
Operating Temperature Range .... 0°C to +70°C

DC Electrical Specifications

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.0	-	V	V_{CC} = 5.25V
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = 4.75V
High Level Clock Input	V_{IHC}	3.0	-	V	V_{CC} = 5.25V
Low Level Clock Input	V_{ILC}	-	0.8	V	V_{CC} = 4.75V
Output HIGH Voltage	V_{OH}	2.6	-	V	I_{OH} = -400mA, V_{CC} = 4.75V
Output LOW Voltage	V_{OL}	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.75V
Input Leakage Current	I_I	-10	10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V
I/O Leakage Current	I_O	-10	10	µA	V_{OUT} = V_{CC} or GND, V_{CC} = 5.25V
Standby Power Supply Current	I_{CCSB}	-	500	µA	V_{IN} = V_{CC} or GND V_{CC} = 5.25V, Note 3
Operating Power Supply Current	I_{CCOP}	-	150	mA	f = 15MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Notes 1 and 3

Capacitance T_A = +25°C, Note 2

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_{IN}	-	15	pF	FREQ = 1MHz, V_{CC} = Open, All measurements are referenced to device ground
Output Capacitance	C_O	-	15	pF	

NOTES:

1. Power supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 10mA/MHz.
2. Not tested, but characterized at initial design and at major process/design changes.
3. Output load per test load circuit with switch open and C_L = 40pF.

A.C. Electrical Specifications V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C (Note 1)

SYMBOL	PARAMETER	-15 (15MHz) MIN	-15 (15MHz) MAX	-25 (25.6MHz) MIN	-25 (25.6MHz) MAX	-33 (33MHz) MIN	-33 (33MHz) MAX	UNITS	TEST CONDITIONS
T_{CP}	CLK Period	66		39		30		ns	
T_{CH}	CLK High	26		15		12		ns	
T_{CL}	CLK Low	26		15		12		ns	
T_{WL}	WR# Low	26		15		12		ns	
T_{WH}	WR# High	26		15		12		ns	
T_{AWS}	Set-up Time; AD0-1, CS# to WR# Going High	18		13		13		ns	
T_{AWH}	Hold Time; AD0, AD1, CS# from WR# Going High	0		0		0		ns	
T_{CWS}	Set-up Time C0-15 from WR# Going High	20		15		15		ns	
T_{CWH}	Hold Time C0-15 from WR# Going High	0		0		0		ns	
T_{WC}	Set-up time WR# High to CLK High	20		16		12		ns	Note 3
T_{MCS}	Set-up Time MOD0-1 to CLK Going High	20		15		15		ns	
T_{MCH}	Hold Time MOD0-1 from CLK Going High	0		0		0		ns	
T_{PCS}	Set-up Time PACI# to CLK Going High	25		15		11		ns	
T_{PCH}	Hold Time PACI# from CLK Going High	0		0		0		ns	
T_{ECS}	Set-up ENPHREG#, ENCFREG#, ENOFREG#, ENPHAC#, ENTIREG#, CLROFR#, PMSEL, LOAD#, ENI#, ACC, BINFMT#, PEAK#, MODPI/2PI#, SH0-1, RBYTILD# from CLK Going High	18		12		12		ns	
T_{ECH}	Hold Time ENPHREG#, ENCFREG# ENOFREG#, ENPHAC#, ENTIREG#, CLROFR#, PMSEL, LOAD#, ENI#, ACC, BINFMT#, PEAK#, MODPI/2PI#, SH0-1, RBYTILD# from CLK Going High	0		0		0		ns	
T_{DS}	Set-up Time RIN0-18, IMIN0-18 to CLK Going High	18		12		12		ns	
T_{DH}	Hold Time RIN0-18, IMIN0-18 from CLK Going High	0		0		0		ns	
T_{DO}	CLK to Output Delay RO0-19, IO0-19		40		24		19	ns	
T_{DEO}	CLK to Output Delay DET0-1		40		27		20	ns	
T_{PO}	CLK to Output Delay PACO#		30		20		12	ns	
T_{TO}	CLK to Output Delay TICO#		30		20		12	ns	
T_{OE}	Output Enable Time OER#, OEI#, OEREXT#, OEIEXT#		25		20		20	ns	
T_{MD}	OUTMUX0-1 to Output Delay		40		28		26	ns	
T_{OD}	Output Disable Time		20		15		15	ns	Note 2
T_{RF}	Output Rise, Fall Time		8		8		6	ns	Note 2

NOTES:

1. A.C. testing is performed as follows: Input levels (CLK Input) 4.0V and 0V; Input levels (all other inputs) 0V and 3.0V; Timing reference levels (CLK) 2.0V; All others 1.5V. Output load per test load circuit with switch closed and C_L = 40pF. Output transition is measured at $V_{OH} \geq$ 1.5V and $V_{OL} \leq$ 1.5V.
2. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
3. Applicable only when outputs are being monitered and ENCFREG#, ENPHREG#, or ENTIREG# is active.

Absolute Maximum Ratings

Supply Voltage . . . . +7.0V
Input, Output Voltage . . . . GND -0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . -65°C to +150°C
Junction Temperature . . . . +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C
ESD Classification . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
MQFP Package	22.0°C/W	7.7°C/W

Maximum Package Power Dissipation at TBD
Gate Count . . . . 26,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range
Commercial . . . . +4.75V to +5.25V

Operating Temperature Range
Commercial . . . . 0°C to +70°C

Electrical Specifications (V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Power Supply Current	I_{CCOP}	-	TBD	mA	V_{CC} = Max, CLK Frequency 52.6Mhz Notes 1, 2
Standby Power Supply Current	I_{CCSB}	-	500	µA	V_{CC} = Max, Outputs Not Loaded
Input Leakage Current	I_I	-10	10	µA	V_{CC} = Max, Input = 0V or V_{CC}
Output Leakage Current	I_O	-10	10	µA	V_{CC} = Max, Input = 0V or V_{CC}
Logical One Input Voltage	V_{IH}	2.0	-	V	V_{CC} = Max
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = Min
Logical One Input Voltage: CLK	V_{IHC}	3.0	-	V	V_{CC} = Max
Logical One Output Voltage	V_{OH}	2.6	-	V	I_{OH} = -5mA, V_{CC} = Min
Logical Zero Output Voltage	V_{OL}	-	0.4	V	I_{OL} = 5mA, V_{CC} = Min
Input Capacitance	C_{IN}	-	10	pF	CLK Frequency 1MHz All measurements referenced to GND. T_A = +25°C, Note 3
Output Capacitance	C_{OUT}	-	10	pF	

NOTES:

1. Power supply current is proportional to frequency. Typical rating is TBD mA/MHz. Note that operation at maximum clock frequency will exceed maximum junction temperature of device. Use of a heat sink and/or air flow is required under these conditions: recommended heat sink is TBD.
2. Output load per test circuit and C_L = 40pF.
3. Not tested, but characterized at initial design and at major process/design changes.

AC Electrical Specifications V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C), (Note 1)

PARAMETER	SYMBOL	52MHz (-52) (PRELIMINARY) MIN	MAX	COMMENTS
CLK Period	T_{CP}	19	-	ns
CLK High	T_{CH}	7	-	ns
CLK Low	T_{CL}	7	-	ns
WR# Low	T_{WL}	7	-	ns

AC Electrical Specifications V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C), (Note 1)

PARAMETER	SYMBOL	52MHz (-52) (PRELIMINARY) MIN	MAX	COMMENTS
WR# High	T_{WH}	7	-	ns
Setup Time AD0-1, CS# to WR#	T_{AWS}	10	-	ns
Hold Time AD0-1, CS# from WR#	T_{AWH}	0	-	ns
Setup Time C0-15 to WR#	T_{CWS}	10	-	ns
Hold Time C0-15 from WR#	T_{CWH}	0	-	ns
Setup Time WR# to CLK	T_{WC}	10	-	ns, Note 3
Setup Time MOD0-1 to CLK	T_{MCS}	10	-	ns
Hold Time MOD0-1 from CLK	T_{MCH}	0	-	ns
Setup Time PACI# to CLK	T_{PCS}	10	-	ns
Hold Time PACI# from CLK	T_{PCH}	0	-	ns
Setup Time ENPHREG#, ENCFREG#, ENOFREG#, ENPHAC#, ENTIREG#, CL-ROFR#, PMSEL, LOAD#, ENI#, ACC, BINFMT#, PEAK#, MODPI/2PI#, SH0-1, RBYTILD# to CLK	T_{ECS}	10	-	ns
Hold Time ENPHREG#, ENCFREG#, ENOFREG#, ENPHAC#, ENTIREG#, CL-ROFR#, PMSEL, LOAD#, ENI#, ACC, BINFMT#, PEAK#, MODPI/2PI#, SH0-1, RBYTILD# from CLK	T_{ECH}	0	-	ns
Setup Time RIN0-18,IMIN0-18 to CLK	T_{DS}	10	-	ns
Hold Time RIN0-18, IMIN0-18 from CLK	T_{DH}	0	-	ns
CLK to Output Delay RO0-19, IO0-19	T_{DO}	-	12	ns
CLK to Output Delay DET0-1	T_{DEO}	-	12	ns
CLK to Output Delay PACO#	T_{PO}	-	12	ns
CLK to Output Delay TICO#	T_{TO}	-	12	ns
Output Enable Time OER#, OEI#, OER-EXT#, OEIEXT#	T_{OE}	-	8	ns
Output Enable Time OUTMUX0-1	T_{MD}	-	14	ns
Output Disable Time	T_{OD}	-	8	ns, Note 2
Output Rise, Fall Time	T_{RF}	-	6	ns, Note 2

NOTES:

1. AC tests performed with C_L = 40pF, I_{OL} = TBDmA, and I_{OH} = -TBDmA. Input reference level for CLK = 2.0V, all other inputs 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V; V_{OH} = TBDV, V_{OL} = TBDV.
2. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.
3. Applicable only when outputs are being monitored and ENCFREG#, ENPHREG# or ENTIREG# is active.

Absolute Maximum Ratings

Supply Voltage ....+8.0V
Input or Output Voltage Applied ....GND -0.5V to V_{CC} +0.5V
Storage Temperature Range ....-65°C to +150°C
Junction Temperature ....+175°C
Lead Temperature (Soldering 10s)......................300°C
ESD Classification ....Class 1

Reliability Information

Device Count............................103,000 Transistors

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range......................+4.5V to +5.5V
Operating Temperature Range ....-55°C to +125°C

DC Electrical Specifications T_A = -55°C to +125°C

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.2	-	V	V_{CC} = 5.5V
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = 4.5V
Logical One Input Voltage Clock	V_{IHC}	3.0	-	V	V_{CC} = 5.5V
Logical Zero Input Voltage Clock	V_{ILC}	-	0.8	V	V_{CC} = 4.5V
Output HIGH Voltage	V_{OH}	2.6	-	V	I_{OH} = -400µA, V_{CC} = 4.5V (Note 1)
Output LOW Voltage	V_{OL}	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.5V (Note 1)
Input Leakage Current	I_I	-10	+10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V
Output or I/O Leakage Current	I_O	-10	+10	µA	V_{OUT} = V_{CC} or GND, V_{CC} = 5.5V
Standby Power Supply Current	I_{CCSB}	-	500	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, (Note 4)
Operating Power Supply Current	I_{CCOP}	-	150	mA	f = 15MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.5V (Notes 2, 4)
Functional Test	FT	-	-		(Note 3)

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 10mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH} (clock inputs) = 3.4V, V_{IH} (all other inputs) = 2.6V, V_{IL} = 0.4V, $V_{OH} \geq$ 1.5V, and $V_{OL} \leq$ 1.5V.
4. Output per test load circuit with switch open and C_L = 40pF.

AC Electrical Specifications T_A = -55°C to +125°C

PARAMETER	SYMBOL	-15 (15MHz)		-25 (25.6MHz)		UNITS	(NOTE 1) CONDITIONS
		MIN	MAX	MIN	MAX		
CLK Period	T_{CP}	66	-	39	-	ns	
CLK High	T_{CH}	26	-	15	-	ns	
CLK Low	T_{CL}	26	-	15	-	ns	
WR# Low	T_{WL}	26	-	15	-	ns	
WR# High	T_{WH}	26	-	15	-	ns	
Set-up Time; AD0-1, CS# to WR# Going High	T_{AWS}	20	-	18	-	ns	
Hold Time; AD0, AD1, CS# from WR# Going High	T_{AWH}	0	-	0	-	ns	
Set-up Time C0-15 from WR# Going High	T_{CWS}	20	-	18	-	ns	

AC Electrical Specifications T_A = -55°C to +125°C (Continued)

PARAMETER	SYMBOL	-15 (15MHz) MIN	-15 (15MHz) MAX	-25 (25.6MHz) MIN	-25 (25.6MHz) MAX	UNITS	(NOTE 1) CONDITIONS
Hold Time C0-15 from WR# Going High	T_{CWH}	0	-	0	-	ns	
Set-up Time WR# to CLK High	T_{WC}	20	-	16	-	ns	(Note 2)
Set-up Time MOD0-1 to CLK Going High	T_{MCS}	20	-	18	-	ns	
Hold Time MOD0-1 from CLK Going High	T_{MCH}	0	-	0	-	ns	
Set-up Time PACI# to CLK Going High	T_{PCS}	25	-	18	-	ns	
Hold Time PACI# from CLK Going High	T_{PCH}	0	-	0	-	ns	
Set-up Time ENPHREG#, ENCFRCTL#, ENPHAC#, ENTICTL#, CLROFR#, PMSEL#, LOAD#, ENI#, ACC, BINFMT#, PEAK#, MODPI/2PI#, SH0-1, RBYTILD# from CLK Going High	T_{ECS}	20	-	15	-	ns	
Hold Time ENPHREG#, ENCFRCTL#, ENPHAC#, ENTICTL#, CLROFR#, PMSEL#, LOAD#, ENI#, ACC, BINFMT#, PEAK#, MODPI/2PI#, SH0-1, RBYTILD# from CLK Going High	T_{ECH}	0	-	0	-	ns	
Set-up Time RIN0-18, IMIN0-18 to CLK Going High	T_{DS}	20	-	15	-	ns	
Hold Time RIN0-18, IMIN0-18, to CLK Going High	T_{DH}	0	-	0	-	ns	
CLK to Output Delay, RO0-19, IO0-19	T_{DO}	-	40	-	25	ns	
CLK to Output Delay, DET0-1	T_{DEO}	-	40	-	27	ns	
CLK to Output Delay, PACO#	T_{PO}	-	30	-	20	ns	
CLK to Output Delay, TICO#	T_{TO}	-	30	-	20	ns	
Output Enable Time, OER#, OEI#, OEREXT#, OEIEXT#	T_{OE}	-	25	-	20	ns	(Note 3)
OUTMUX0-1 to Output Delay	T_{MD}	-	40	-	28	ns	

NOTES:

1. AC testing is performed as follows: V_{CC} = 4.5V and 5.5V. Input levels (CLK Input) 4.0V and 0V; Input levels (all other inputs) 3.0V and 0V; Timing reference levels (CLK) 2.0V; All others 1.5V. Output load per test load circuit with switch closed and C_L = 40pF. Output transition is measured at $V_{OH} \geq 1.5V$ and $V_{OL} \leq 1.5V$.
2. Applicable only when outputs are being monitored and ENCFREG#, ENPHREG#, or ENTIREG# is active.
3. Transition is measured at ±200mV from steady state voltage. Output loading per test load circuit, with switch closed and C_L = 40pF.

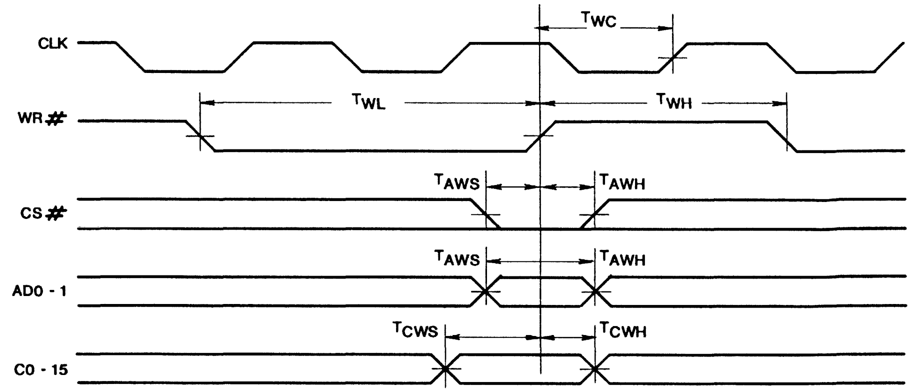
Electrical Specifications

PARAMETER	SYMBOL	NOTES	-15 MIN	-15 MAX	-25 MIN	-25 MAX	UNITS	CONDITIONS
Output Disable Time	T_{OD}	1, 2	-	20	-	15	ns	
Output Rise Time	T_R	1, 2	-	8	-	8	ns	From 0.8V to 2.0V
Output Fall Time	T_F	1, 2	-	8	-	8	ns	From 2.0V to 0.8V

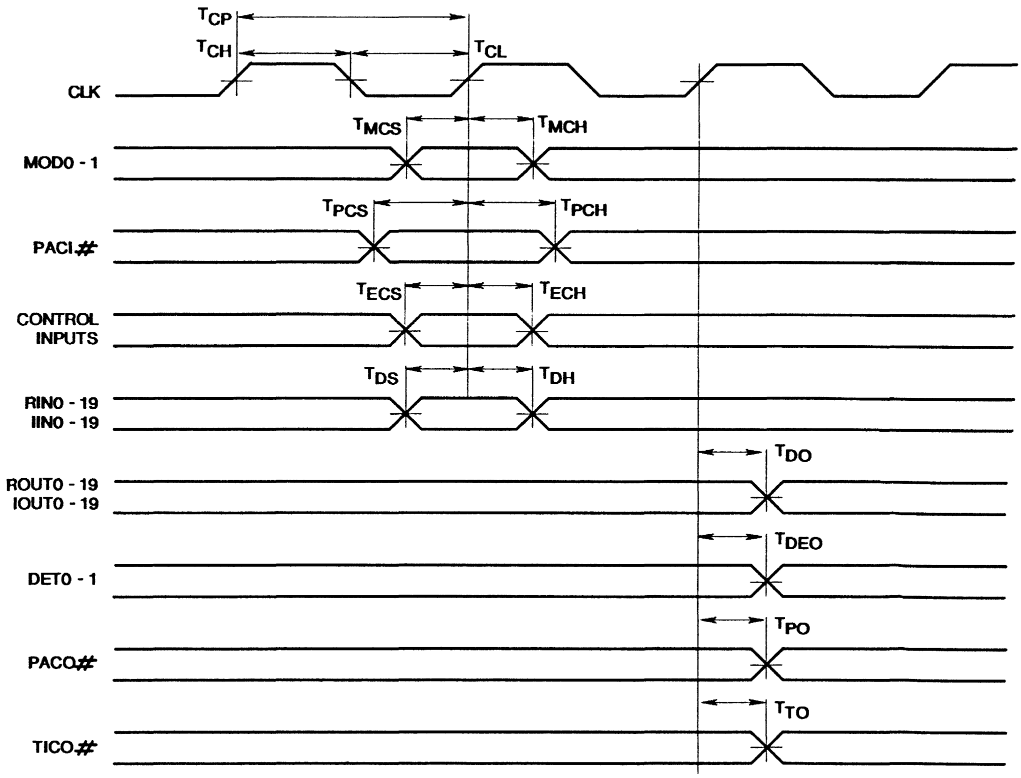
NOTES:

1. The parameters in this table are controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
2. Loading is as specified in the test load circuit with C_L = 40pF.

Waveforms

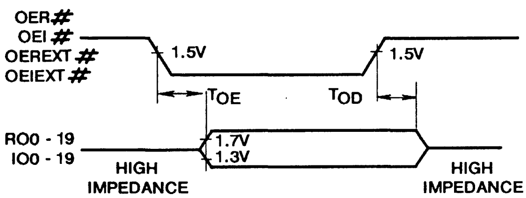


CONTROL BUS TIMING

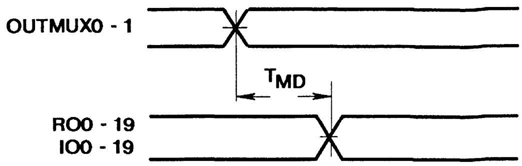


INPUT AND OUTPUT TIMING

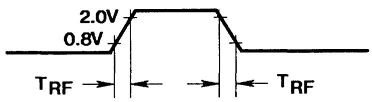
Waveforms (Continued)



OUTPUT ENABLE, DISABLE TIMING

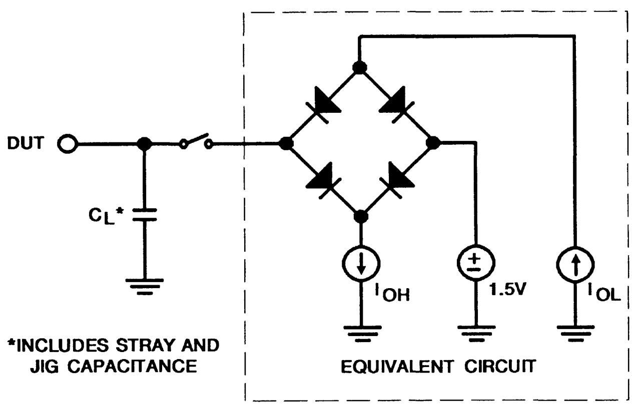


MULTIPLEXER TIMING



OUTPUT RISE AND FALL TIMES

Test Load Circuit



Switch S1 open for I_{CCSB} and I_{CCOP} tests

EQUIVALENT CIRCUIT

HARRIS SEMICONDUCTOR

HSP45116/883

Numerically Controlled Oscillator/Modulator

January 1994

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- NCO and CMAC on One Chip
- 15MHz and 25.6MHz Versions
- 32-Bit Frequency Control
- 16-Bit Phase Modulation
- 16-Bit CMAC
- 0.006Hz Tuning Resolution at 25.6MHz
- Spurious Frequency Components < -90dBc
- Fully Static CMOS

Applications

- Frequency Synthesis
- Modulation - AM, FM, PSK, FSK, QAM
- Demodulation, PLL
- Phase Shifter
- Polar to Cartesian Conversions

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP45116GM-15/883	-55°C to +125°C	145 Lead PGA
HSP45116GM-25/883	-55°C to +125°C	145 Lead PGA

Description

The Harris HSP45116/883 combines a high performance quadrature numerically controlled oscillator (NCO) and a high speed 16-bit Complex Multiplier/Accumulator (CMAC) on a single IC. This combination of functions allows a complex vector to be multiplied by the internally generated (cos, sin) vector for quadrature modulation and demodulation. As shown in the block diagram, the HSP45116/883 is divided into three main sections. The Phase/Frequency Control Section (PFCS) and the Sine/Cosine Section together form a complex NCO. The CMAC multiplies the output of the Sine/Cosine Section with an external complex vector.

The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The phase resolution of the PFCS is 32-bits, which results in frequency resolution better than 0.006Hz at 25.6MHz. The output of the PFCS is the argument of the sine and cosine. The spurious free dynamic range of the complex sinusoid is greater than 90dBc.

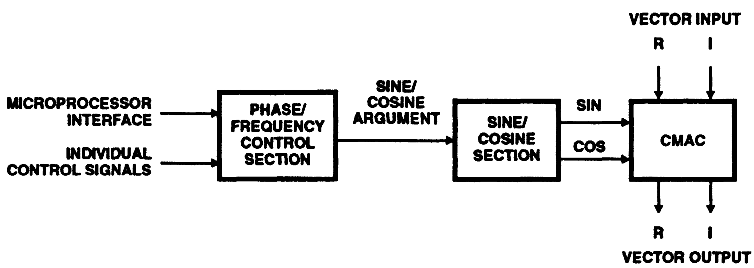
The output vector from the Sine/Cosine Section is one of the inputs to the Complex Multiplier/Accumulator. The CMAC multiplies this (cos, sin) vector by an external complex vector and can accumulate the result. The resulting complex vectors are available through two 20-bit output ports which maintain the 90dB spectral purity. This result can be accumulated internally to implement an accumulate and dump filter.

A quadrature down converter can be implemented by loading a center frequency into the Phase/Frequency Control Section. The signal to be downconverted is the Vector Input of the CMAC, which multiplies the data by the rotating vector from the Sine/Cosine Section. The resulting complex output is the down converted signal.

5

SIGNAL SYNTHESIZERS

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2813.2

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input or Output Voltage Applied .... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering 10 sec) .... 300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
Ceramic PGA Package .... 23.1°C/W 8.3°C/W
Maximum Package Power Dissipation at +125°C
Ceramic PGA Package .... 2.16 Watt
Device Count .... 103,000 Transistors

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range .... -55°C to +125°C

TABLE 1. HSP45116/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
Logical One Input Voltage Clock	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	3.0	-	V
Logical Zero Input Voltage Clock	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400μA V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	+10	μA
Output or I/O Leakage Current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	+10	μA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, (Note 4)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	500	μA
Operating Power Supply Current	I_{CCOP}	f = 15MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.5V (Notes 2, 4)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	150	mA
Functional Test	FT	(Note 3)	7, 8	-55°C ≤ T_A ≤ +125°C	-	-	

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 10mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH} (clock inputs) = 3.4V, V_{IH} (all other inputs) = 2.6V, V_{IL} = 0.4V, V_{OH} ≥ 1.5V, and V_{OL} ≤ 1.5V.
4. Output per test load circuit with switch open and C_L = 40pF.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. HSP45116/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	-15 (15MHz) MIN	-15 (15MHz) MAX	-25 (25.6MHz) MIN	-25 (25.6MHz) MAX	UNITS
CLK Period	T_{CP}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	66	-	39	-	ns
CLK High	T_{CH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	26	-	15	-	ns
CLK Low	T_{CL}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	26	-	15	-	ns
WR# Low	T_{WL}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	26	-	15	-	ns
WR# High	T_{WH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	26	-	15	-	ns
Set-up Time; AD0-1, CS# to WR# Going High	T_{AWS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	18	-	ns
Hold Time; AD0, AD1, CS# from WR# Going High	T_{AWH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
Set-up Time C0-15 from WR# Going High	T_{CWS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	18	-	ns
Hold Time C0-15 from WR# Going High	T_{CWH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
Set-up Time WR# to CLK High	T_{WC}	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	16	-	ns
Set-up Time MOD0-1 to CLK Going High	T_{MCS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	18	-	ns
Hold Time MOD0-1 from CLK Going High	T_{MCH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
Set-up Time PACI# to CLK Going High	T_{PCS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	25	-	18	-	ns
Hold Time PACI# from CLK Going High	T_{PCH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
Set-up Time ENPHREG# ENCFRCTL#, ENPHAC#, ENTICTL# CLROFR#, PMSEL#, LOAD#, ENI#, ACC, BINFMT#, PEAK#, MODPI/2PI#, SH0-1, RBYTILD# from CLK Going High	T_{ECS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	15	-	ns
Hold Time ENPHREG#, ENCFRCTL#, ENPHAC#, ENTICTL# CLROFR#, PMSEL#, LOAD#, ENI#, ACC, BINFMT#, PEAK#, MODPI/2PI#, SH0-1, RBYTILD# from CLK Going High	T_{ECH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
Set-up Time RIN0-18, IMIN0-18 to CLK Going High	T_{DS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	15	-	ns
Hold Time RIN0-18, IMIN0-18, to CLK Going High	T_{DH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns

TABLE 2. HSP45116/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	-15		-25		UNITS
					MIN	MAX	MIN	MAX	
CLK to Output Delay RO0-19, IO0-19	T_{DO}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	-	25	ns
CLK to Output Delay DET0-1	T_{DEO}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	-	27	ns
CLK to Output Delay PACO#	T_{PO}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	30	-	20	ns
CLK to Output Delay TICO#	T_{TO}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	30	-	20	ns
Output Enable Time OER#, OEI#, OEREXT#, OEIEXT#	T_{OE}	(Note 3)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	25	-	20	ns
OUTMUX0-1 to Output Delay	T_{MD}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	-	28	ns

NOTES:

1. A.C. testing is performed as follows: V_{CC} = 4.5V and 5.5V. Input levels (CLK Input) 4.0V and 0V; Input levels (all other inputs) 3.0V and 0V; Timing reference levels (CLK) 2.0V; All others 1.5V. Output load per test load circuit with switch closed and C_L = 40pF. Output transition is measured at $V_{OH} \geq$ 1.5V and $V_{OL} \leq$ 1.5V.
2. Applicable only when outputs are being monitored and ENCFREG#, ENPHREG#, or ENTIREG# is active.
3. Transition is measured at ±200mV from steady state voltage, Output loading per test load circuit, with switch closed and C_L = 40pF.

TABLE 3. HSP45116/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	-15		-25		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	VCC = Open, f = 1 MHz All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	15	-	15	pF
Output Capacitance	C_{OUT}		1	$T_A = +25^oC$	-	15	-	15	pF
Output Disable Time	T_{OD}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	20	-	15	ns
Output Rise Time	T_R	From 0.8V to 2.0V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	8	-	8	ns
Output Fall Time	T_F	From 2.0V to 0.8V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	8	-	8	ns

NOTES:

1. The parameters in Table 3 are controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
2. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	—	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Burn-In Circuit

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	V_{CC}	IMIN 4	IMIN 8	IMIN 9	IMIN 11	IMIN 15	IMIN 16	GND	V_{CC}	IO 18	IO 15	IO 12	IO 10	GND	V_{CC}	A
B	GND	IMIN 1	IMIN 5	IMIN 7	IMIN 10	IMIN 13	IMIN 14	IO 19	IO 16	IO 14	IO 11	IO 8	IO 7	IO 5	IO 2	B
C	RIN 15	RIN 18	IMIN 2	IMIN 3	IMIN 6	IMIN 12	IMIN 17	IMIN 18	IO 17	IO 13	IO 9	IO 6	IO 4	IO 1	RO 18	C
D	RIN 13	RIN 17	IMIN 0	INDEX									IO 3	RO 19	RO 17	D
E	RIN 10	RIN 14	RIN 16										IO 0	RO 16	RO 15	E
F	RIN 7	RIN 11	RIN 12										RO 14	RO 13	RO 11	F
G	V_{CC}	RIN 9	RIN 8										RO 9	RO 12	RO 10	G
H	GND	RIN 6	RIN 5										RO 8	RO 7	GND	H
J	RIN 3	RIN 1	RIN 4										RO 5	RO 4	V_{CC}	J
K	RIN 2	RIN 0	SH 1										RO 1	RO 2	RO 6	K
L	SH 0	ACC	RBYTILD #										PACO #	DET 1	RO 3	L
M	ENPH REG #	PEAK #	MOD 1										OEREXT #	OEI #	RO 0	M
N	ENOF REG #	BINFMT #	MOD 0	LOAD #	ENCF REG #	MODPI /2PI #	AD 0	C 14	C 13	C 8	C 2	OUT-MUX 1	OUT-MUX 0	OEIEXT #	DET 0	N
P	TICO #	PACI #	PMSEL	CLROFR #	ENTIREG #	CS #	AD 1	C 15	C 10	C 9	C 6	C 3	C 1	OER #	GND	P
Q	V_{CC}	GND	ENPHAC #	ENI #	CLK	WR #	V_{CC}	GND	C 12	C 11	C 7	C 5	C 4	C 0	V_{CC}	Q
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

145 LEAD
PIN GRID ARRAY
TOP VIEW

5

SIGNAL SYNTHESIZERS

Burn-In Circuit (Continued)

PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
D3	IMIN(0)	F4	Q3	ENPHAC#	F1	K14	RO(2)	$V_{CC}/2$	A10	IO(18)	$V_{CC}/2$
C2	RIN(18)	F9	P5	ENTIREG#	F4	L15	RO(3)	$V_{CC}/2$	B8	IO(19)	$V_{CC}/2$
D2	RIN(17)	F8	Q4	ENI#	F1	J14	RO(4)	$V_{CC}/2$	C8	IMIN(18)	F9
E3	RIN(16)	F7	N6	MODPI/2PI#	F16	J13	RO(5)	$V_{CC}/2$	C7	IMIN(17)	F8
C1	RIN(15)	F6	P6	CS#	F2	K15	RO(6)	$V_{CC}/2$	A7	IMIN(16)	F7
E2	RIN(14)	F5	Q5	CLK	F0	H14	RO(7)	$V_{CC}/2$	A6	IMIN(15)	F6
D1	RIN(13)	F4	P7	AD(1)	F4	H13	RO(8)	$V_{CC}/2$	B7	IMIN(14)	F5
F3	RIN(12)	F16	N7	AD(0)	F3	G13	RO(9)	$V_{CC}/2$	B6	IMIN(13)	F4
F2	RIN(11)	F15	Q6	WR#	F1	G15	RO(10)	$V_{CC}/2$	C6	IMIN(12	F16
E1	RIN(10)	F14	P8	C(15)	GND	F15	RO(11)	$V_{CC}/2$	A5	IMIN(11)	F15
G2	RIN(9)	F13	N8	C(14)	GND	G14	RO(12)	$V_{CC}/2$	B5	IMIN(10)	F14
G3	RIN(8)	F12	N9	C(13)	GND	F14	RO(13)	$V_{CC}/2$	A4	IMIN(9)	F13
F1	RIN(7)	F11	Q9	C(12)	GND	F13	RO(14)	$V_{CC}/2$	A3	IMIN(8)	F12
H2	RIN(6)	F10	Q10	C(11)	GND	E15	RO(15)	$V_{CC}/2$	B4	IMIN(7)	F11
H3	RIN(5)	F9	P9	C(10)	GND	E14	RO(16)	$V_{CC}/2$	C5	IMIN(6)	F10
J3	RIN(4)	F8	P10	C(9)	GND	D15	RO(17)	$V_{CC}/2$	B3	IMIN(5)	F9
J1	RIN(3)	F7	N10	C(8)	GND	C15	RO(18)	$V_{CC}/2$	A2	IMIN(4)	F8
K1	RIN(2)	F6	Q11	C(7)	GND	D14	RO(19)	$V_{CC}/2$	C4	IMIN(3)	F7
J2	RIN(1)	F5	P11	C(6)	GND	E13	IO(0)	$V_{CC}/2$	C3	IMIN(2)	F6
K2	RIN(0)	F4	Q12	C(5)	GND	C14	IO(1)	$V_{CC}/2$	B2	IMIN(1)	F5
K3	SH(1)	F3	Q13	C(4)	GND	B15	IO(2)	$V_{CC}/2$	A1	V_{CC}	None
L1	SH(0)	F2	P12	C(3)	GND	D13	IO(3)	$V_{CC}/2$	A9	V_{CC}	V_{CC}
L2	ACC	F4	N11	C(2)	GND	C13	IO(4)	$V_{CC}/2$	A15	V_{CC}	None
M1	ENPHREG#	F16	P13	C(1)	GND	B14	IO(5)	$V_{CC}/2$	G1	V_{CC}	V_{CC}
N1	ENOFREG#	F4	Q14	C(0)	V_{CC}	C12	IO(6)	$V_{CC}/2$	J15	V_{CC}	V_{CC}
M2	PEAK#	F8	N12	OUTMUX(1)	F11	B13	IO(7)	$V_{CC}/2$	Q1	V_{CC}	None
L3	RBYTILD#	F16	N13	OUTMUX(0)	F10	B12	IO(8)	$V_{CC}/2$	Q7	V_{CC}	V_{CC}
N2	BINFMT#	F4	P14	OER#	F0	C11	IO(9)	$V_{CC}/2$	Q15	V_{CC}	None
P1	TICO#	$V_{CC}/2$	M13	OEREXT#	F0	A13	IO(10)	$V_{CC}/2$	A8	GND	GND
M3	MOD(1)	GND	N14	OEIEXT#	F0	B11	IO(11)	$V_{CC}/2$	A14	GND	None
N3	MOD(0)	GND	M14	OEI#	F0	A12	IO(12)	$V_{CC}/2$	B1	GND	None
P2	PACI#	F4	L13	PACO#	$V_{CC}/2$	C10	IO(13)	$V_{CC}/2$	H1	GND	GND
N4	LOAD#	F15	N15	DET0	$V_{CC}/2$	B10	IO(14)	$V_{CC}/2$	H15	GND	GND
P3	PMSEL	F1	L14	DET1	$V_{CC}/2$	A11	IO(15)	$V_{CC}/2$	P15	GND	None
P4	CLROFR#	F4	M15	RO(0)	$V_{CC}/2$	B9	IO(16)	$V_{CC}/2$	Q2	GND	None
N5	ENCFREG#	F4	K13	RO(1)	$V_{CC}/2$	C9	IO(17)	$V_{CC}/2$	Q8	GND	GND

NOTES:

1. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND
2. V_{CC} = 5.5V ± 0.5V with 0.1μF (min) capacitor between V_{CC} and GND per position
3. F0 = 100kHz ± 10%, F1 = F0/2, F2 = F1/2 . . . . . , F11 = F10/2, 40% to 60% duty cycle
4. Input Voltage limits: V_{IL} = 0.8V max, V_{IH} = 4.5V ±10%

Die Characteristics

DIE DIMENSIONS:
350 x 353 x 19 ±1 mils

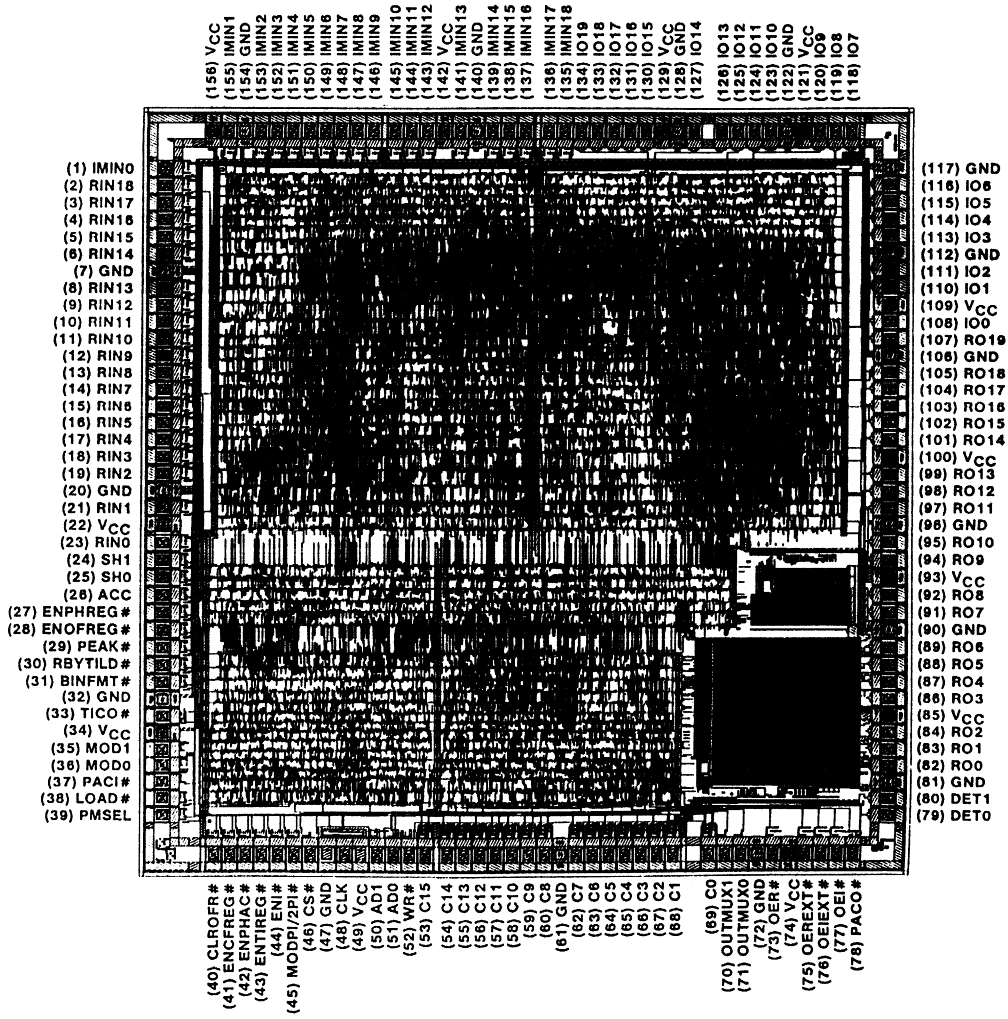
METALLIZATION:
Type: Si-Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY: 1.6 x 10^5A/cm^2

Metallization Mask Layout

HSP45116/883



SIGNAL SYNTHESIZERS 5

DSP 6

DOWN CONVERSION AND DEMODULATION

NOTE: Bold Type Designates a New Product from Harris.

6 DOWN CONV. AND DEMODULATION

HARRIS SEMICONDUCTOR

HSP50016

JC-52 292,- — 15a 16wk
GC-52 476,-
JC-75 367,-

January 1994

Digital Down Converter

Features

- 52 MSPS Input Data Rate
- 16-Bit Data Input
- Spurious Free Dynamic Range Through Modulator >102dB
- Frequency Selectivity: <0.006Hz
- Identical Lowpass Filters for I and Q
- Passband Ripple: <0.04dB
- Stopband Attenuation: >104dB
- Filter -3dB to -102dB Shape Factor: <1.5
- Decimation from 64 to 131,072
- IEEE 1149.1 Test Access Port

Applications

- Digital Radio Receivers
- Channelized Receivers
- Spectrum Analysis

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP50016JC-52	0°C to +70°C	44 Lead PLCC
HSP50016GC-52	0°C to +70°C	48 Lead PGA

HSP50016JC-75 75MHz clk.

Description

The Digital Down Converter (DDC) is a single chip synthesizer, quadrature mixer and lowpass filter. Its input data is a sampled data stream of up to 16-bits in width and up to a 52 MSPS data rate. The DDC performs down conversion, narrowband low pass filtering and decimation to produce a baseband signal.

The internal synthesizer can produce a variety of signal formats. They are: CW, frequency hopped, linear FM up chirp, and linear FM down chirp. The complex result of the modulation process is lowpass filtered and decimated with identical real filters in the in phase (I) and quadrature (Q) processing chains.

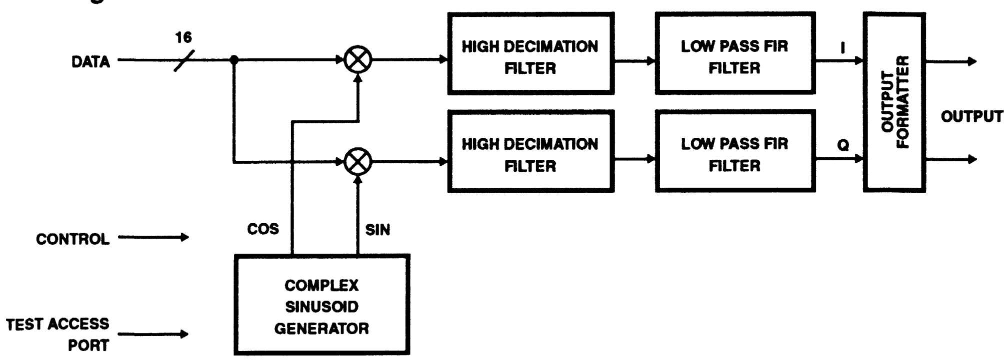
Lowpass filtering is accomplished via a high decimation filter (HDF) followed by a fixed finite impulse response (FIR) filter. The combined response of the two stage filter results in a -3dB to -102dB shape factor of better than 1.5. The stopband attenuation is greater than 106dB. The composite passband ripple is less than 0.04dB. The synthesizer and mixer can be bypassed so that the chip operates as a single narrow band low pass filter.

The chip receives forty bit serial commands as a control input. This interface is compatible with the serial I/O port available on most microprocessors.

The output data can be configured in fixed point or single precision floating point. The fixed point formats are 16, 24, 32, or 38 bit, two's complement, signed magnitude, or offset binary.

The circuit provides an IEEE 1149.1 Test Access Port.

Block Diagram

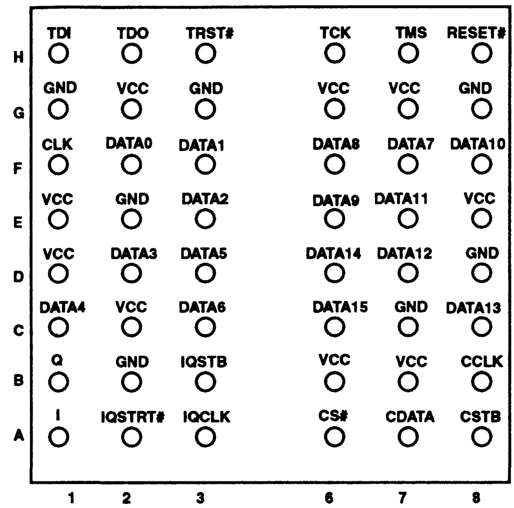


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3288.3

Pinouts

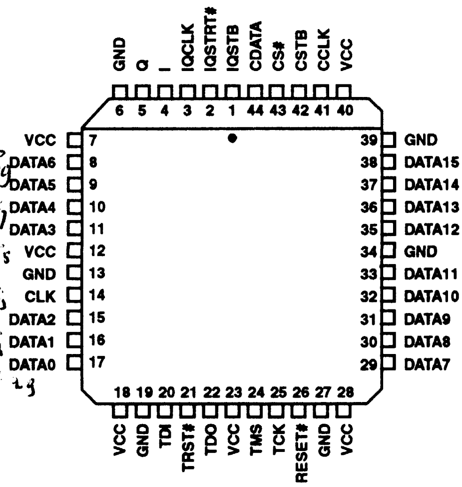
48 PIN PGA
BOTTOM VIEW



48 PIN PGA
TOP VIEW

	1	2	3		6	7	8
A	I	IQSTRT#	IQCLK		CS#	CDATA	CSTB
B	Q	GND	IQSTB		VCC	VCC	CCLK
C	DATA4	VCC	DATA6		DATA15	GND	DATA13
D	VCC	DATA3	DATA5		DATA14	DATA12	GND
E	VCC	GND	DATA2		DATA9	DATA11	VCC
F	CLK	DATA0	DATA1		DATA8	DATA7	DATA10
G	GND	VCC	GND		VCC	VCC	GND
H	TDI	TDO	TRST#		TCK	TMS	RESET#

44 LEAD PLCC
TOP VIEW



Pin Description

NAME	PLCC PIN	TYPE	DESCRIPTION
VCC	7, 12, 18, 23, 28, 40	-	+5V Power
GND	6, 13, 19, 27, 34, 39	-	Ground
DATA0-15	8-11, 15-17, 29-33, 35-38	I	Input data bus. Selectable between two's complement and offset binary. DATA0 is the LSB.
CLK	14	I	Clock for input data bus.
RESET#	26	I	RESET# initializes the internal state of the DDC. During RESET#, all internal processing stops. RESET# facilitates the synchronization of multiple chips for Auto Three-State operation. If the Force bits in control word 7 are inactive and the IEEE Test Access Port is in an Idle state, RESET# causes the IQCLK, IQSTB, I and Q outputs to go to a high impedance state. All control registers are updated from their respective control buffer registers on the third rising edge of CLK after the deassertion of RESET#. If RESET# is deasserted T_{RR} nanoseconds prior to the rising edge of CLK, the internal reset will deassert synchronously. If T_{RR} is violated, then the circuit contains a synchronizer which will cause reset to be deasserted internally one or more clocks later. An initial reset is required to guarantee proper operation of the DDC. Active low.
I	4	O	The I output has three modes: I data; I data followed by Q data; real data.
Q	5	O	The Q output has two modes: Q data and the carry out of the Phase Adder.
IQCLK	3	O	IQCLK: bit or word clock for the I and Q outputs.
IQSTB	1	O	IQSTB: beginning or end of word indicator for I and Q.
IQSTRT#	2	I	Initiates output data sequence. Active low.
CDATA	44	I	Port for control data input.
CCLK	41	I	Control data input bit clock.
CSTB	42	I	Beginning of word indicator for control data.
CS#	43	I	Enables control data loading of DDC. Active low.
TCK	25	I	Bit clock for IEEE 1149.1 data.
TMS	24	I	Test port mode select.
TDI	20	I	Input data IEEE test port.
TDO	22	O	Output data for IEEE test port.
TRST#	21	I	Test port reset. Active low.

DDC Functional Block Diagram

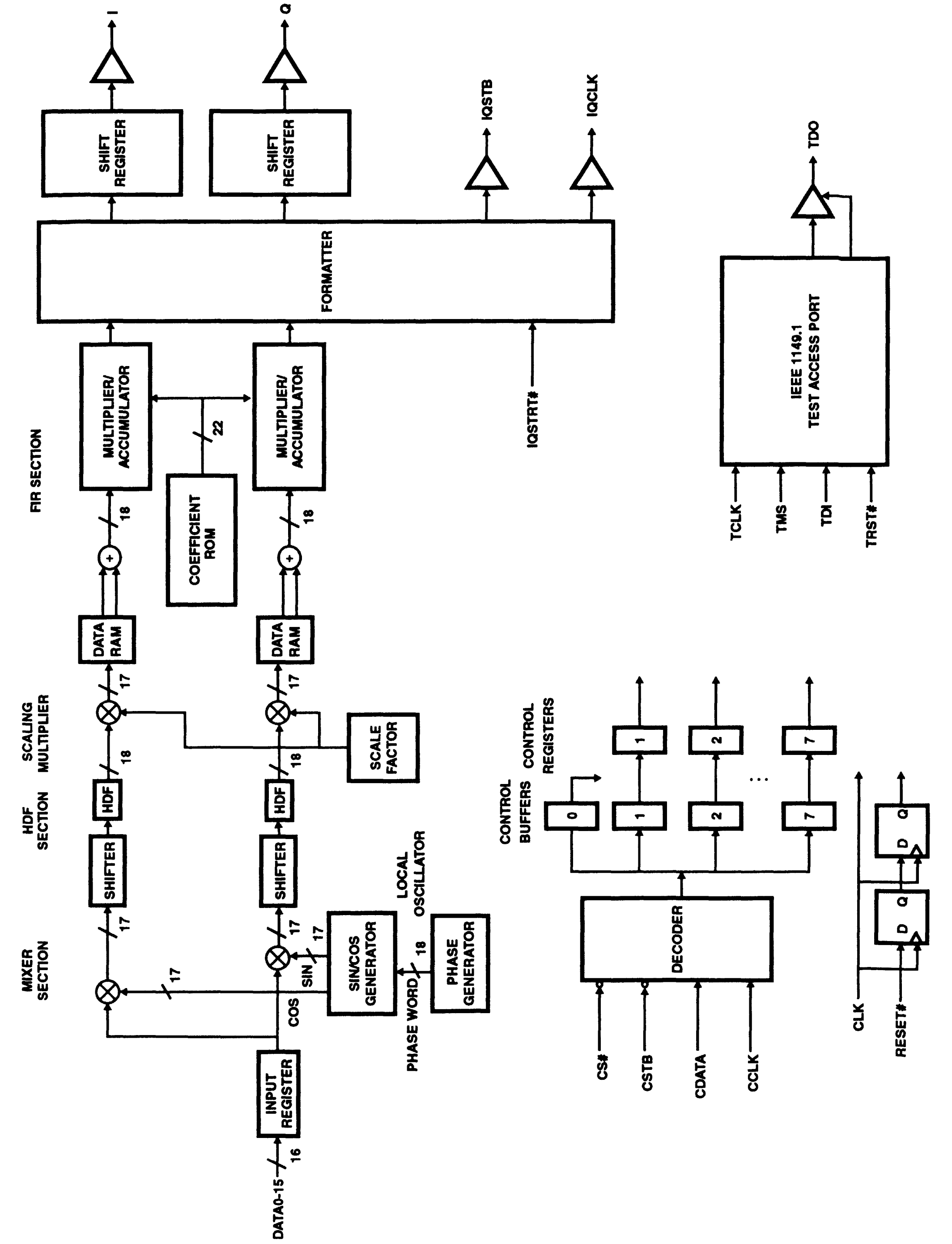


FIGURE 1

Phase Generator Block Diagram

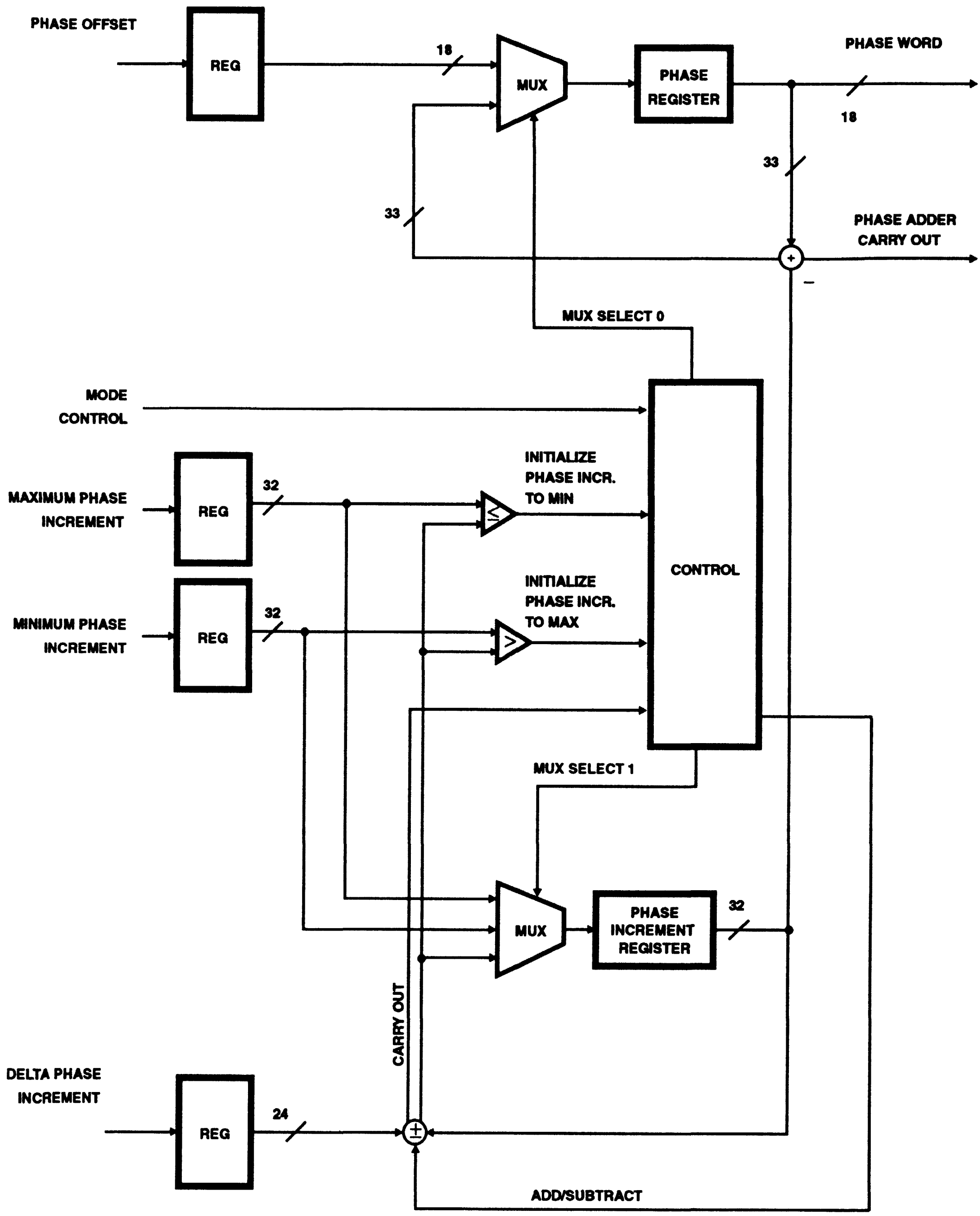


FIGURE 2

Functional Description

The primary function of the DDC is to extract a narrow band of interest from a wideband input, convert that band to baseband and output it in either a quadrature or real form. This is accomplished by centering the band of interest at DC by multiplying the input data times a quadrature sinusoid. A quadrature lowpass filter (identical real lowpass filters in the in phase (I) and quadrature phase (Q) processing branches) is applied to the result. Each filtering chain consists of a cascaded HDF and FIR filter, which extract the band of interest. During filtering, the signal is decimated by a rate which is proportional to the output bandwidth. The bandwidth of the resulting signal is the double sided passband width of the lowpass filters. An Output Formatter manipulates the filter output to provide the data in a variety of formats.

Local Oscillator

Signal data clocked into the DATA0-15 input of the DDC is multiplied by a quadrature sinusoid in the Mixer section. (See Figure 1). The data input to the DDC is a 16 bit real data stream which is sampled on the rising edges of CLK. It can be in two's complement or offset binary format.

The input data is passed to a mixer, which is composed of two real multipliers. One of these multiplies the input data samples by the in phase (cosine) component of the quadrature sinusoid and the other multiplies the input data samples by the quadrature (sine) component. The in phase and quadrature data paths are designated I and Q respectively. The sine and cosine are generated in the local oscillator as shown in Figure 1.

The local oscillator is programmed to produce a quadrature sinusoid with programmable frequency and phase. The frequency can be constant (Continuous Wave - CW), linearly increasing (up chirp), linearly decreasing (down chirp), or linear up/down chirp. The initial phase of the waveform is set by the phase offset.

The phase, frequency and chirp limits of the quadrature sinusoid are controlled by the Phase Generator (Figure 2). The output of the Phase Generator is an 18 bit phase word that represents the current phase angle of the complex sinusoid. The Phase Generator automatically increments the phase angle by a preprogrammed amount on every rising edge of CLK. Stepping the output phase from 0 through full scale (2^{18} - 1) steps the phase angle of the quadrature sinusoid from 0 to $(-2+2^{-17})\pi$ radians.The frequency of the complex sinusoid is determined by the number of clocks needed for the phase to step though its full range of 2π radians. The required phase increment for a given local oscillator frequency is calculated by:

$$\text{Phase Increment} = 2^{33} f_C / f_S \qquad (1)$$

where:

f_C is the desired local oscillator frequency

f_S is the input sampling frequency

There are five parameters which control the Phase Generator. They are: phase offset, minimum phase increment, maximum phase increment, delta phase increment and mode control. Mode control is used to select the function of the other parameters.

The phase offset is the initial setting of the phase word going to the SIN/COS Generator. Subsequent phases of the sinusoid are calculated relative to this offset. The minimum phase increment has two mode dependent functions: when the SIN/COS Generator is forming a CW waveform, the minimum phase increment is the phase step taken on every clock. When the SIN/COS Generator is producing a chirped sinusoid, the minimum phase increment is the smallest phase step taken. Maximum phase increment is only used during chirped modes; it is the largest allowable phase increment. During chirp modes, the delta phase increment is the difference between successive phase increments.

The four phase parameters are stored in their respective registers in the Phase Generator. The Phase Register stores the current phase angle. On the first clock following the deassertion of RESET#, the 18 MSBs of the Phase Register are loaded from the Phase Offset Register. On every rising edge of CLK thereafter, the output of the Phase Increment Register is subtracted from the 32 LSBs of the current phase. The 33 bit difference is stored back in the Phase Register on the next CLK. The 18 most significant bits of the Phase Register form the phase word, which is the input to the SIN/COS Generator.

Figure 3 gives a graphic representation of the four phase parameters. To understand their interrelationships, the phase should be visualized as the angle of a rotating vector. When the local oscillator in the DDC is programmed to generate a CW waveform, the multiplexers are configured so that the Minimum Phase Increment is stored in the Phase Increment Register; this value is subtracted from the output of the Phase Register on every CLK and the difference becomes the new Phase Register value. The Delta Phase Increment and Maximum Phase Increment are ignored.

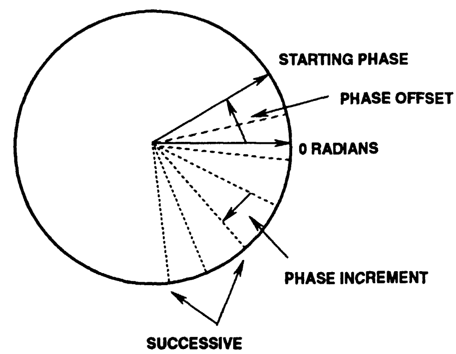


FIGURE 3. PHASE WORD PARAMETERS FOR CW CASE

In up chirp mode the local oscillator generates a signal with a linearly increasing frequency (Figure 4A). The Phase Increment Register is initially loaded with the Minimum Phase Increment value; on every clock, the contents of the

Phase Increment Register is subtracted from the current output of the Phase Register. Simultaneously, the Delta Phase Increment Register is added to the 24 LSBs of the output of the Phase Increment Register. On the next CLK, that sum is stored back in the Phase Increment Register, the new phase is stored in the Phase Register and the process is repeated. The phase increment is allowed to grow until the next phase increment would exceed the maximum phase increment value. When this happens, the Phase Increment Register is reset to the minimum phase increment and the cycle starts over again. Note that the phase increment is never equal to the maximum phase increment. From the time the Phase Generator starts at the minimum phase increment until it reaches the maximum phase increment, the phase word on clock n is given by:

Phase Word = Phase Offset - [Minimum Phase Increment + n(Delta Phase Increment)]

An example of the outputs of the Phase Increment Register, Phase Register, and the I output of the SIN/COS Generator are shown in Figure 4B.

In down chirp mode the local oscillator generates a signal with a linearly decreasing frequency (Figure 5A). The maximum phase increment is loaded into the Phase Increment Register and the phase offset value goes into the Phase Register. The delta phase increment is subtracted from the 24 LSBs of the phase increment to form a new phase increment at each clock. The phase increment is allowed to diminish until it reaches the minimum phase increment value, then it is reset to the maximum phase increment value and the cycle is repeated. Note that the value of the phase increment can be equal to, but never less than the minimum phase increment, since the Phase Increment Register is reloaded if the next phase increment value would be less than the minimum phase increment. This feature protects the DDC from exceeding the Nyquist frequency. In this case, from the time the Phase Generator starts at the maximum phase increment until it reaches the minimum phase increment, the phase word on clock n is given by:

Phase Word = Phase Offset - [Maximum Phase Increment - n(Delta Phase Increment)]

See Figure 5B for a graphical representation of this process.

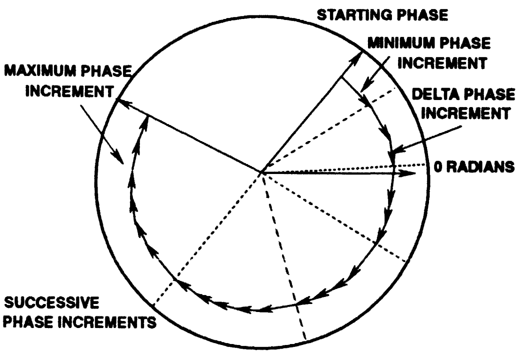


FIGURE 4A. PHASE WORD DURING UP CHIRP.

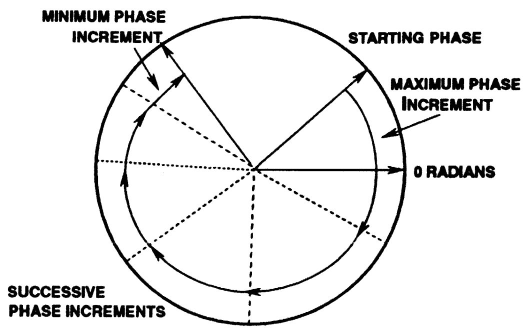


FIGURE 5A. PHASE WORD DURING DOWN CHIRP

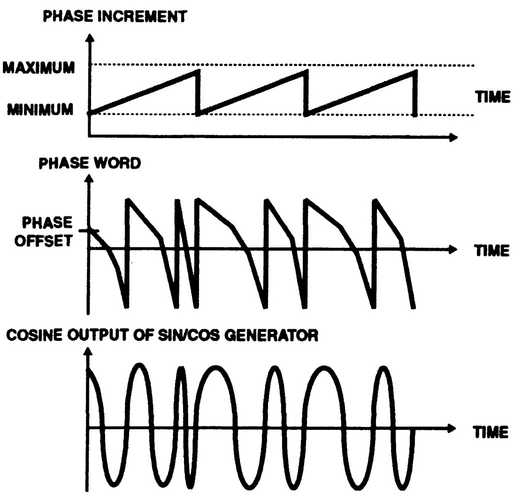


FIGURE 4B. UP CHIRP

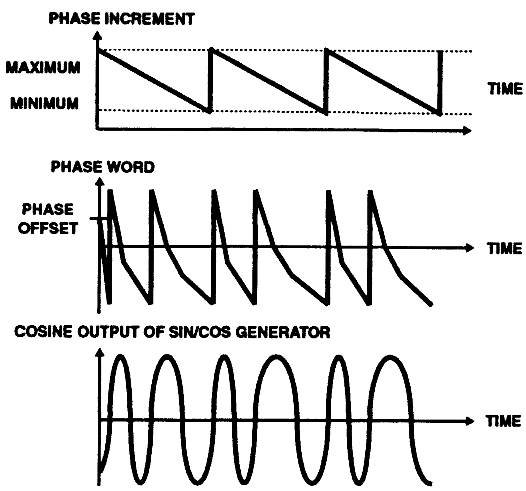


FIGURE 5B. DOWN CHIRP

In up/down chirp mode, the phase accumulator is set to the phase offset value and the minimum phase increment is loaded into the Phase Increment Register. The delta phase increment is added to the 24 LSBs of the Phase Increment Register to form a new phase increment at each clock. The phase increment is allowed to grow until it nears the maxmum phase increment value (as defined in the up chirp description). The delta phase increment value is then subtracted from the least significant bits of the Phase Increment Register to form a new phase increment at each clock. The phase increment is allowed to diminish until it reaches the minimum phase increment value (as defined in the down chirp description). The Phase Increment Register is then reloaded with the minimum phase increment, and the up/down cycle begins again. See Figure 6 for a graphical representation of this process.

The minimum and maximum phase increments have allowable values from 0 to 2^{32}-1. This corresponds to the phase increment:

$$0 < \text{Phase Increment} < \pi(1 - 2^{-32}) \text{ radians}$$

The Delta Phase Increment parameter can take on values from 0 to 2^{24} - 1 which corresponds to the Delta Phase Increment:

$$0 < \text{Delta Phase Increment} < \pi(2^{-8} - 2^{-32}) \text{ radians}$$

The output of the phase accumulator forms the input to the SIN/COS Generator which in turn produces a quadrature vector which rotates clockwise: the outputs are cos(ωn) and -sin(ωn). The outputs of the SIN/COS Generator are two's complement values which are scaled to prevent overflow in subsequent operations in the DDC under normal operation. The scale factor has a negligible effect on the end to end DDC gain.

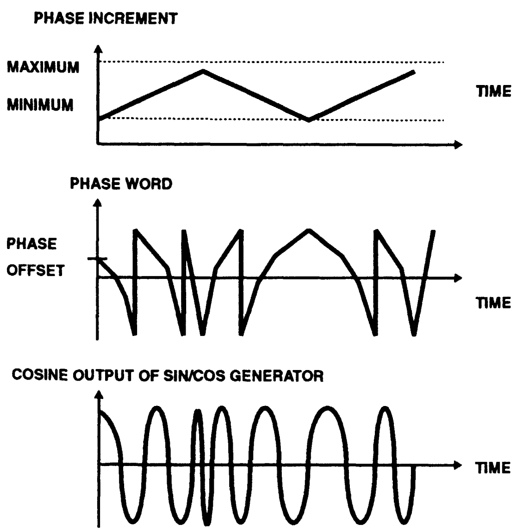


FIGURE 6. UP/DOWN CHIRP

The frequency resolution of the DDC = (frequency of CLK) / (Number of Phase Register bits). At the maximum clock rate, this results in a frequency selectivity of 52MHz/2^{33} = 0.006Hz. The 18 bit phase word yields a phase noise Figure of greater than 102dB.

Mixer

The Mixer performs quadrature modulation by multiplying the output of the SIN/COS Generator by the input data. The outputs of the I and Q multipliers are symmetrically rounded to 17 bits to preserve the 102 dB spurious free dynamic range (SFDR). The result of the quadrature modulation process is passed to the High Decimating Filter (HDF) section.

High Decimation Filter

The High Decimation Filter (HDF) section is comprised of two real HDF filters, one processing the I data branch and one processing the Q data branch. Each branch has the lowpass response shown in Figure 7. The undecimated frequency impulse response is given by the equation:

$$H(f) = (\mathrm{Sin}(\pi f)/\mathrm{Sin}(\pi f/R))^5$$

In Figure 7, f' = f_S/R, the input sample rate divided by the HDF decimation factor. Figure 7 shows this curve from DC to the first null. Note that the HDF is a true FIR filter; i.e., the phase is linear.

The data path through the HDF was designed to ensure a true 16 bit noise floor (approximately 98dB) at the output of the DDC. The structure of the HDF filter used in the DDC is a five stage decimation filter. The width of each successive stage decreases such that the LSBs are lost due to truncation [1]. As a result, the data must be processed in the MSBs of the filter so that the noise due to truncation is below the required noise floor. This means that the input data of the HDF must be shifted so that its output data fills the HDF output word. The shift is a function of the desired HDF decimation rate R and the number of stages, which is fixed at 5. The shift is performed by the Data Shifter, which positions the input data to the HDF for the maximum dynamic range while avoiding overflow errors. The shift factor is programmed into the Shift field of Control Word 4. The value in this field is calculated by the equation:

$$\text{Shift} = 75 - \text{Ceiling}(5 \log_2(R)) \qquad (2)$$

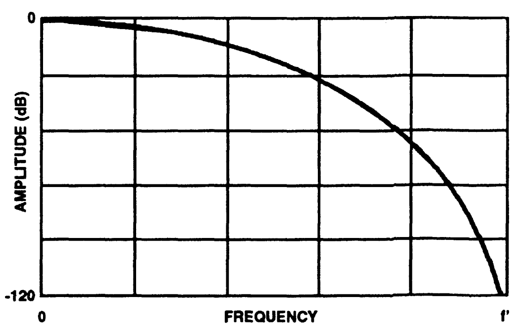


FIGURE 7. FREQUENCY RESPONSE OF HIGH DECIMATION FILTER FROM DC TO FIRST NULL

where R is the HDF decimation rate and Ceiling(X) denotes the ceiling function of X; i.e., the result is X if X is an integer, otherwise the result is the next higher integer.

The output data rate of the HDF is CLK divided by the HDF decimation rate (programmed into the HDF Decimation field in Control Word 5).

During RESET#, the HDF is initialized and will not output any information until it is filled with new data.

Scaling Multipliers

The output of each HDF is passed to a Scaling Multiplier. The Scaling Multipliers are used to compensate for the HDF gain, which is between 1 (inclusive) and 0.5 (noninclusive), or (0.5, 1.0]. The gain through the HDF is dependent on the decimation factor: when the decimation is a power of two, the HDF gain is equal to 1; otherwise, the gain must be compensated for in the Scaling Multiplier. The HDF gain is given by the equation:

$$\text{HDF Gain} = R^5 / 2^{\text{Ceiling}(5\log_2(R))} \quad (3)$$

where R is the HDF decimation rate. The compensating Scale Factor, which is input to both Scaling Multipliers, is given by the equation:

$$\text{Scale Factor} = 2^{\text{Ceiling}(5\log_2(R))}/R^5 \quad (4)$$

Note that the Scale Factor falls in the interval [1,2). The output of the scaling multiplier is symmetrically rounded to 17 bits.

The binary formats of the inputs and outputs of the scaling multiplier are as follows:

Input from HDF: $a_0(-2^0).\ a_1(2^{-1})\ a_2(2^{-2}) \ldots a_{17}(2^{-17})$

Scale factor: $a_0(2^0).\ a_1(2^{-1})\ a_2(2^{-2}) \ldots a_{15}(2^{-15})$

Output: $a_0(-2^0).\ a_1(2^{-1})\ a_2(2^{-2}) \ldots a_{16}(2^{-16})$

FIR Filter

The Scaling Multiplier output is passed to the FIR Filter, which performs aliasing attenuation, passband roll off compensation and transition band shaping. The FIR Filter Section is functionally two identical 121 tap lowpass FIR filters, one each for the I and Q channel. The two filters are each implemented as sum of products, each with a single multiplier, with the coefficients stored in ROM. The filters' passbands are precompensated to be the inverse of the response of the HDF. The frequency response of the FIR filters is shown in Figure 8. The composite HDF and FIR filter frequency response is shown in Figure 9. The FIR coefficients are scaled so that the maximum gain of the composite filter is less than or equal to 0dB. The composite passband ripple is less than 0.04dB.

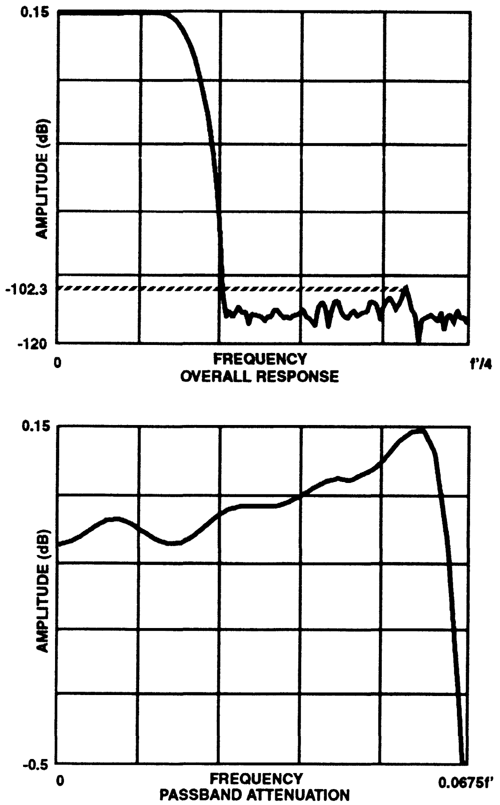


FIGURE 8. FREQUENCY RESPONSE OF FIR FILTER

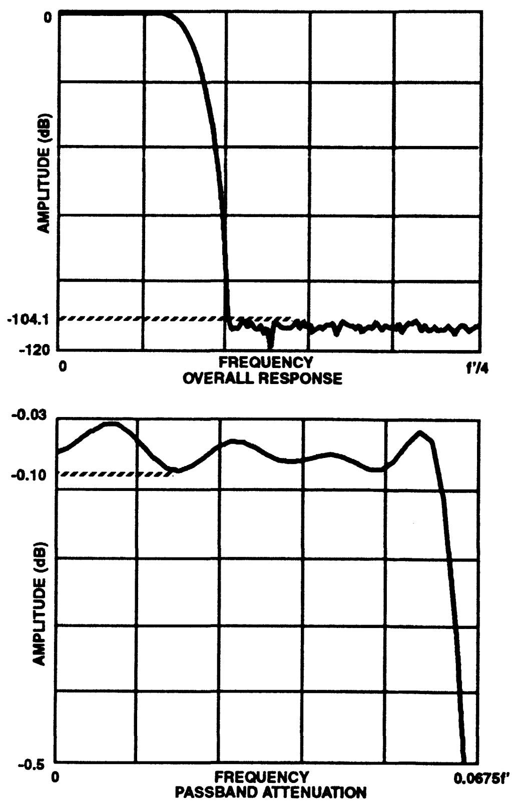


FIGURE 9. END TO END FREQUENCY RESPONSE OF DDC

The coefficients of the filter are quantized to 22 bits to preserve greater than 106dB of stopband attenuation. The sum of products of each filter output calculation is a 38 bit number with 37 fractional bits.

When a quadrature output is selected, the outputs of the FIR filters are decimated by a factor of four. When real output is selected, only the I output is active. The output is decimated by two in this case. When Filter Only mode is selected, only the I filter path is active and its output is decimated by four.

The composite filter bandwidths are a function of the HDF decimation rate and the FIR Filter shape. The double sided bandwidths are specified by the following equations.

$$-3\text{dB BW} = 0.13957 \times f' \qquad (5)$$

$$-102\text{dB BW} = 0.19903 \times f' \qquad (6)$$

Output Control

The circuit has two serial data outputs, I and Q. The timing of the output bits is referenced to IQCLK and IQSTB. There are several modes of operation for the data and control lines, all of which were designed to be compatible with common microprocessors. These modes are programmed by loading the appropriate control words (see Table 1 through Table 8).

The I output has three modes: I data out; I data followed by Q data; and real data out. The Q pin can output either Q data or the carry out of the Phase Adder. Both outputs can be programmed to set the number of significant bits transmitted; the arithmetic representation; the order of the bits, LSB or MSB first; and the polarity of the data bits, high or low true. The spectral sense of the output data is selectable between normal and reversed. The spectral orientation of the data is selectable between baseband centered quadrature, baseband offset quadrature, and baseband real. In addition, the output drivers for I, Q, IQCLK and IQSTB can be individually enabled or placed in a high impedance state using Control Word 6. These options are explained below.

Quadrature data output can occur in one of two ways: simultaneously or sequentially. The simultaneous method clocks out the I and Q data on their respective output pins. The I followed by Q method clocks I and Q out sequentially on the I output pin: the entire I word is serially clocked out first, then the entire Q word. In real data output mode, the Formatter converts the quadrature data to real and clocks it out serially on the I output pin. In all modes, the I and Q outputs return to the zero state after the last bit is transmitted.

TABLE 1. FORMAT FOR CONTROL WORD (0) - CONTROL REGISTER UPDATE

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	000 = Control Word 0
36	Update	0 = No Control Register Update Update
35-32	Reserved	All zeroes

TABLE 2. FORMAT FOR CONTROL WORD 1 - PHASE GENERATOR / TEST ENABLE / OUTPUT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	001 = Control Word 1
36	Update	0 = No Control Register Update 1 = Control Register Update
35-4	Minimum Phase Increment	Bits 35-4 = $2^{31}...2^0$
3	Test Enable	0 = Test Features Disabled 1 = Test Features Enabled
2-0	Phase Generator Mode	000 = Filter Only 001 = Normal Mode (CW) 010 = Reserved 011 = Up Chirp 100 = Reserved 101 = Down Chirp 110 = Reserved 111 = Up/Down Chirp

TABLE 3. FORMAT FOR CONTROL WORD 2 - PHASE GENERATOR

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	010 = Control Word 2
36	Update	0 = No Control Register Update 1 = Control Register Update
35-32	Reserved	All zeroes
31-0	Maximum Phase Increment	Bits 31-0 = $2^{31}...2^0$.

TABLE 4. FORMAT FOR CONTROL WORD 3 - PHASE GENERATOR / OUTPUT TIME SLOT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	011 = Control Word 3
36	Update	0 = No Control Register Update 1 = Control Register Update
35-32	Reserved	All zeroes
31-18	Time Slot Length	Time Slot length in IQCLK periods; length = number of bits + 2. Bits 31-18 = $2^{13}...2^0$.
17-0	Phase Offset	Starting phase angle of phase accumulator; range = 0 to 2π. Bits 17-0 = $2^{33}...2^{16}$

TABLE 5. FORMAT FOR CONTROL WORD 4 - PHASE GENERATOR / HDF / OUTPUT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	100 = Control Word 4
36	Update	0 = No Control Register Update 1 = Control Register Update
35-33	Reserved	All zeroes
32-31	Output Spectrum	00 = No Up Conversion, Complex Output 01 = Up Convert by f*/4, Real Output 10 = Up Convert by f*/2, Complex Output 11 = Reserved Mode
30-7	Delta Phase Increment	24 Bit Delta Phase Increment. Bits 30-7 = $2^{23}...2^0$.
6-1	HDF Data Shift	HDF input data shift (towards LSB). Bits 6-1 = $2^5...2^0$. Shift =75 - Ceiling(5 $\log_2$(R))
0	Spectral Reverse	0 = Normal output 1 = Spectrally Reversed output

TABLE 6. FORMAT FOR CONTROL WORD 5 - HDF / OUTPUT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	101 = Control Word 5
36	Update	0 = No Control Register Update 1 = Control Register Update
35-21	HDF Decimation Rate	HDF Decimation Factor Minus 1. Minimum Allowable Value = 15. Bits 35-21 = $2^{14}...2^0$. Decimate by 32,768: Bits 35-21 = All Ones
20-5	Scaling Multiplier Gain	16 Bit Gain Compensation Number With Values Between 0 and 2, 2 Non Inclusive. Bits 20-5 = $2^0.2^{-1}...2^{-15}$.
4-3	Output Format	00 = Two's Complement 01 = Offset Binary 10 = Sign Magnitude 11 = Single Precision Floating Point Format
2-1	Number Of Output Bits	00 = 16 Bits 01 = 24 Bits 10 = 32 Bits 11 = 38 Bits
0	Output Sense	0 = LSB First 1 = MSB First

TABLE 7. FORMAT FOR CONTROL WORD 6 - INPUT, OUPUT FORMATS

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	110 = Control Word 6
36	Update	0 = No Control Register Update 1 = Control Register Update
35	I followed by Q	0 = I and Q output separately 1 = I and Q data output on I pin
34-29	Time Slot Number	Bits 34-29 = $2^5...2^0$.
28	IQCLK Polarity	0 = Output Data Stable On Rising Edge Of IQCLK; IQCLK high between I or Q bit periods when IQCLK Duration = 0. 1 = Output Data Stable On Falling Edge Of IQCLK; IQCLK low between I or Q bit periods when IQCLK Duration = 0.
27	IQCLK Duty Cycle	0 = IQCLK Active Time = CLK period. 1 = 50% Duty Cycle
26	IQCLK Duration	0 = Active During I or Q bit periods only 1 = Active continuously
25-24	IQCLK Three State Control	00 = Three State IQCLK 01 = Enable IQCLK 1x = Auto-Three State Enable IQCLK
23	IQSTB Polarity	0 = Active High 1 = Active Low
22	IQSTB Location	0 = IQSTB prior to the beginning of the data word. 1 = IQSTB during the data word.
21-20	IQSTB Three State Control	00 = Three State IQSTB 01 = Enable IQSTB 1x = Auto Three State Enable IQSTB
19	I Polarity	0 = True data 1 = Inverted Data
18-17	I Three State Control	00 = Three State I 01 = Enable I 1x = Auto Three State Enable I
16	Q Polarity	0 = True data 1 = Inverted data
15-14	Q Three State Control	00 = Three State Q 01 = Enable Q 1x = Auto Three State Enable Q
13	Input Format	0 = Offset Binary 1 = Two's Complement
12-0	IQCLK Rate	I/QCLK Rate, Bits 12-0 = $2^{12}...2^0$.

TABLE 8. FORMAT FOR CONTROL WORD 7 - TEST FEATURES

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	111 = Control Word 7
36	Update	0 = No Control Register Update 1 = Control Register Update
35-14	Reserved	All zeroes
13	Data	0 = Normal Data Input 1 = Force Input Data to 8000 Hex.
12-11	FIR Accumulator Control	00 = Normal Accumulation 01 = No Accumulation 10 = Continuous Accumulation 11 = Reserved
10	Q Strobe on Roll Over	0 = Q carries normal data 1 = Q Strobes When Phase Generator Rolls Over
9	Force Outputs	0 = Normal Output Response 1 = Force Outputs
8	IQCLK Forced Data	If Bit 9 = 1, Force IQCLK = Bit 8; Else Normal
7	IQSTB Forced Data	If Bit 9 = 1, Force IQSTB = Bit 7; Else Normal.
6	I Forced Data	If Bit 9 = 1, Force I = Bit 6; Else Normal.
5	Q Forced Data	If Bit 9 = 1, Force Q = Bit 5; Else Normal.
4-3	Bypass	If Bit 4 = 0 Sin Cos Generator Normal, if Bit 4 = 1 bypass. If Bit 3 = 0 Scaling Multiplier Normal, if Bit 3 = 1, then scale factor = 1.
2	Reserved	Must be zero for proper operation while Test Features are enabled.
1	Wait For RAM Full	If Bit = 0, DDC will output data normally after a reset, which will include unpredictable data in data RAMs. If bit = 1, no chip output will occur until sufficient data RAM locations are written.
0	Disable Overflow Protection	0 = Normal Operation 1 = Disable Overflow Protection

When set for fixed point output, the output data can be in two's complement, offset binary or signed magnitude form. Data is converted to offset binary by complementing the most significant bit of a two's complement number. The length of the output data word can be 16, 24, 32 or 38 bits. The first three options are symmetrically rounded to the LSB of the output data; the fourth option represents the full 38 bit width of the accumulator and so represents exact arithmetic.

The output has a saturation option to prevent possible overflow due to a step input at power up.When Overflow Protection is enabled the output is forced to be either the most positive or most negative number. Saturation is available in all four fixed point output options.

Data can also be output in single precision floating point format. (See Table 9.) For all output data formats, the internal calculations are performed in exact two's complement integer arithmetic and the resulting data is converted in the Output Formatter.

TABLE 9. FLOATING POINT FORMAT

SIGN	EXPONENT	MANTISSA	
-2^0	2^7 to 2^0	Implied 1	0.2^{-1} to 2^{-23}

The I and Q pins can be programmed for either simultaneous or I followed by Q output. In simultaneous mode, the I and Q data appear on the I and Q pins, respectively. Each data sample is preceded by a leading zero bit, followed by the output data, followed by a trailing zero bit. In I followed by Q mode, the output data appears on the I pin, and consists of a leading zero bit, then the I data, a trailing zero, a leading zero, the Q data, and finally a trailing zero bit. In Figure 10 and Figure 11, the leading and trailing zero bits occur before bit 0 and after bit N, respectively.

IQCLK is used to delineate the bit or word timing of the I and Q outputs. There are several options on the configuration of IQCLK, which are controlled with Control Word 6 (See Table 7). The frequency of IQCLK is programmed to be a fraction of the CLK frequency, from (CLK rate)/2 to (CLK rate)/8192 (See equation 7). If IQCLK Rate = 0, then IQCLK remains in its inactive state and the output bits change on the rising edges of CLK.

$$\text{IQCLK Rate} = \frac{\text{CLK}}{\text{IQCLK Frequency}} - 1 \qquad (7)$$

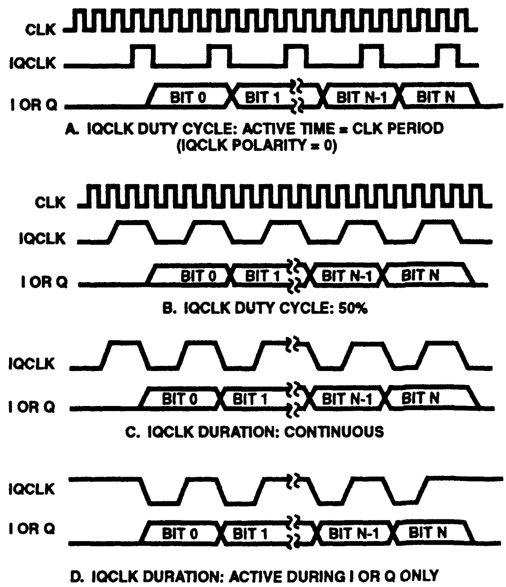
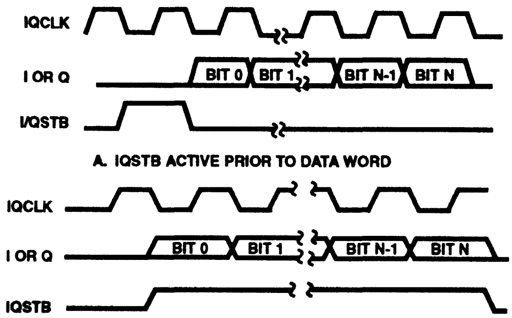


FIGURE 10. TIMING FOR CLK, IQCLK, IQSTB, I AND Q

IQCLK can be programmed to be active only during I or Q output or it can be active continuously with the IQCLK Duration bit. Using the IQCLK Duty Cycle bit, IQCLK is selectable as either 50% duty cycle or to be high for one period of CLK. In addition, the Formatter can be set so that the data bits are clocked on either the positive or negative edges of IQCLK with the IQCLK Polarity bit. Figure 10 shows the various modes of operation with IQCLK Polarity programmed for active high operation.

Control word 6 also configures IQSTB, as shown in Figure 11. When programmed for Active Prior to Data Word, IQSTB is high for one period of IQCLK and terminates simultaneously with the beginning of the first data bit; otherwise it goes active with the beginning of the first bit and inactive with the end of the last bit. IQSTB can be programmed to be either active high or low.



A. IQSTB ACTIVE PRIOR TO DATA WORD

B. IQSTB ACTIVE DURING DATA WORD

FIGURE 11. IQSTB TIMING

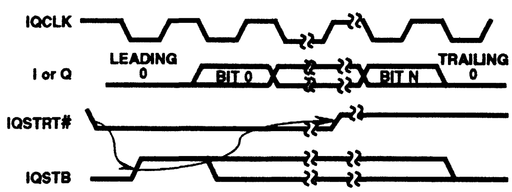


FIGURE 12. REQUESTED DATA OUTPUT TIMING

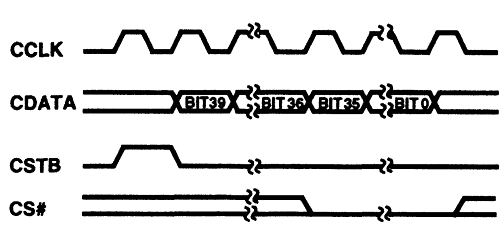


FIGURE 13. CONTROL WORD TIMING DIAGRAM

Data can be read out of the DDC on request through the use of the IQSTRT# pin. After passing through the Formatter, the I and Q data are stored in output buffers, which are updated at the end of the FIR Filter processing cycle. The IQSTRT# and IQSTB lines form a two line handshake as shown in Figure 12. IQSTRT# initiates the request. If the buffer has data in it, the DDC will begin an output data sequence on the next edge of IQCLK. The DDC will then put out one bit per IQCLK until the output cycle is complete. In I followed by Q mode, one IQSTRT# will initiate an I output word followed by a Q output word. In real data output mode, one IQSTRT# will initiate two samples of real data on the I pin.

To avoid the generation of multiple read cycles, IQSTRT# must go inactive within 10 cycles of IQCLK after the initiation of IQSTB. The DDC will not update the output buffer again until the current output cycle has completed. When IQSTRT# is used in this handshake mode, it must consist of pulses that satisfy the set up and hold requirements listed in the AC Timing Specifications and the pulses must occur at a rate of CLK/(HDF Decimation x 4 -1). This mode of operation requires the Time Slot Number in control word 6 to be 0.

When handshake mode is not used, IQSTRT# should be at a logic low.

Auto Three State mode for IQCLK, IQSTB, I and Q allows multiple chips to operate using common data and output control lines. Each chip is assigned a Time Slot Number on the bus to use for outputting its data. All outputs programmed for Auto Three State Mode are active during their time slot and are in a high impedance state at all other times. A time slot starts one CLK period prior to the beginning of the first bit of I or Q and ends (Time Slot Length) CLK periods afterwards. Assignment of a time slot is with reference to the deassertion of RESET#. The minimum possible Time Slot Length for a given application is:

$$\text{Length}_{min} = [(\text{Number of Output Bits} + 2) \times \text{Mode}] + 1 \qquad (8)$$

Where Mode = 2 if the DDC is in either Real Output or I Followed By Q mode; else Mode = 1.

Note that equation 8 is useful in all modes for calculating the number of IQCLKs necessary to complete one output data cycle. For a given decimation rate and output word length, the maximum value in the IQCLK Rate field is:

$$\text{IQCLK Rate}_{max} = \text{Floor}\left[\frac{(\text{HDF Decimation}) \times 4}{\text{Length}_{min}}\right] - 1 \qquad (9)$$

Where Floor(X) represents the integer part of X.

Control Word Input

The DDC has eight 40 bit control words which are loaded through the four pin control interface. The format and timing of this interface is compatible with the serial interface timing of most common DSP microprocessors (See Figure 13). The words are shifted MSB first, where bit 39 of the control word is the MSB. Bits 39 through 37 are the control word address, i.e. the target control buffer. CS# must go low before bit 35 is clocked in. All 40 bits of the control word must be loaded. The formats of the control words are shown in Tables 1 through 8.

The control words are double buffered: each control word is initially loaded into one of eight control buffers for subsequent down loading into the corresponding control register. The internal circuitry of the DDC uses the control registers to regulate its operation. Control buffers can be downloaded in one of two ways. Loading a buffer register with bit 36 = 1 causes all control registers to be updated from their respective control buffers when the current word is finished loading. If bit 36 = 0, then only that control buffer is updated and the operation of the DDC is not affected. All control registers are updated from their respective buffers on the third rising edge of CLK following the deassertion of RESET#. Note that Control Word 0 is unique in that it is only used to update the seven control registers, and it is recognized by the DDC regardless of the state of CS#. In systems with multiple DDCs, this allows the user to update the configuration of all chips simultaneously without using RESET#.

To ensure that the control information is properly loaded, the frequency of CLK must be greater than the frequency of CCLK. In addition, RESET# must remain inactive during the loading of a control word.

Test

The HSP50016 supports two types of testing. Control Word 7 can be used to verify the operation of the circuit through the divide and conquer method. Setting the Enable Test Bit (Control Word 1, bit 3) equal to a 1 enables the test features controlled by Control Word 7. (This bit is in Control Word 1 so that Word 7 does not have to be loaded if the test features are not being used.) The functions allowed by Control Word 7 are shown in table 8.

The DDC also has a Test Access Port (TAP). This port is full conformant to IEEE Std. 1149.1 - 1990 - IEEE Standard Test Access Port and Boundary-Scan. [2] The TAP supports the following instructions: BYPASS, SAMPLE/PRELOAD, INTEST, EXTEST, RUNBIST and IDCODE. In addition, there are seven instructions called RDCNTLWD1-7, which read the contents of the control words over the TAP. The address bits and bit 36 are only used to determine the destination of data during loading; they are not stored, so they are not read out with this instruction.

The full description of the operation fo the DDC while under the control of the TAP will be published in a separate document.

Applications

Down Conversion

The primary spectral operation in the DDC is down conversion of an input signal to base band. See Figure 14. This process is done in two steps: multiplication of the input waveform by an internally generated quadrature sinusoid, i.e., modulation and lowpass filtering to attenuate the unwanted spectral components. The unwanted spectral components have two sources, the input signal and an artifact of the modulation process.

The modulation process can be written as:

$$u(n) = x(n)e^{-j\omega_c} = x(n)[\cos(\omega_c) - j\sin(\omega_c)]$$

Where x(n) is the real input data sequence, $\omega = 2\pi f$, and ω_c is the frequency of the signal generated by the SIN/COS Generator.

For demonstration purposes let $x(n) = \cos(\omega_k n)$. The multiplication then becomes:

$$\begin{aligned} u(n) &= \cos(\omega_k n)[\cos(\omega_c n) - j\sin(\omega_c n)] \\ &= 1/2[\cos((\omega_k - \omega_c)n) + \cos((\omega_k + \omega_c)n) \\ &\quad - j(\sin((\omega_k + \omega_c)n) - \sin((\omega_k - \omega_c)n))] \end{aligned}$$

The signal u(n) is passed through a low pass filter; assuming that the filter passes the low frequency terms with no degradation and attenuates the high frequency terms completely, the filtering operation produces the output:

$$\begin{aligned} v(n) &= 1/2(\cos((\omega_k - \omega_c)n) + j\sin((\omega_k - \omega_c)n)) \\ &= 1/2e^{j(\omega_k - \omega_c)n} \end{aligned}$$

When the magnitude of the input signal x(n) is one, the magnitude of v(n) is 1/2. Both the I and Q channels are multiplied by a factor of two to yield:

$$\begin{aligned} w(n) &= \cos((\omega_k - \omega_c)n) + j\sin((\omega_k - \omega_c)n) \\ &= e^{j(\omega_k - \omega_c)n}. \end{aligned}$$

Figure 15 shows an HSP50016 in a single channel down conversion circuit. Notice that the input data is only 12 bits, so it is justified to the MSB of the DDC's input data. If a smaller sample width is used, it is recommended that the MSB of the data is input into DATA15, and the unused bits are connected to ground. This alignment makes it easier to locate the position of the MSB in the output data. Note that the input is configured for offset binary arithmetic and the output is set up for I followed by Q, which enables the use of only one serial connection to the output processor. The serial data clock of the processor and the Control Clock of the DDC are driven by a TTL compatible oscillator. (IQCLK cannot be used for this purpose since its frequency is indeterminate until the DDC has been configured.) Note that many processors provide a bit clock which eliminates the need for the external oscillator.

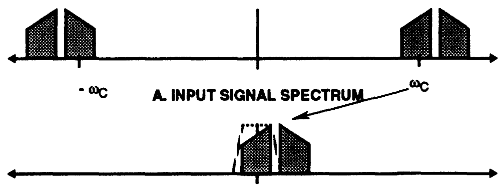


FIGURE 14. DOWN CONVERSION

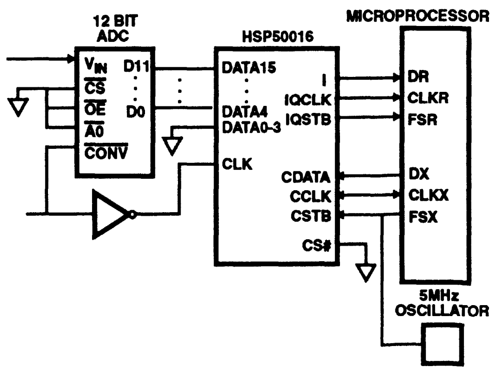


FIGURE 15. CIRCUIT FOR SINGLE CHANNEL OPERATION

An example of the control word contents for this mode of operation is given in Tables 10-15. In this setup, the DDC has been configured for a constant down conversion frequency, decimation by 64 and Test Features disabled. Bit fields of three bits or less are in binary notation; longer fields are in hexadecimal. Control words zero and seven are not used.

TABLE 10. SAMPLE FORMAT FOR CONTROL WORD 1 - PHASE GENERATOR / TEST ENABLE

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	001 = Control Word 1
36	Update	1 = Control Register Update
35-4	Minimum Phase Increment	Minimum Phase Increment Computed according to Equation 1.
3	Test Enable	0 = Test Features Disabled
2-0	Phase Generator Mode	001 = Normal Mode

TABLE 11. SAMPLE FORMAT FOR CONTROL WORD 2 - PHASE GENERATOR

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	010 = Control Word 2
36	Update	0 = No Control Register Update 1 = Control Register Update
35-32	Reserved	All zeroes
31-0	Maximum Phase Increment	All zeroes

TABLE 12. SAMPLE FORMAT FOR CONTROL WORD 3 - PHASE GENERATOR / OUTPUT TIME SLOT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	011 = Control Word 3
36	Update	1 = Control Register Update
35-32	Reserved	All zeroes
31-18	Time Slot Length	All zeroes
17-0	Phase Offset	All zeroes

TABLE 13. SAMPLE FORMAT FOR CONTROL WORD 4 - PHASE GENERATOR / HDF / OUTPUT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	100 = Control Word 4
36	Update	1 = Control Register Update
35-33	Reserved	All zeroes
32	Up Convert	0 = Do not up convert
31	Real Mode	0 = Complex Mode
30-7	Delta Phase Increment	All zeroes
6-1	Shift	37 = Decimal 55, the shift corresponding to HDF decimation by 16
0	Spectral Reverse	0 = No spectral reversal

TABLE 14. SAMPLE FORMAT FOR CONTROL WORD 5 - HDF / OUPUT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	101 = Control Word 5
36	Update	1 = Control Register Update
35-21	HDF Decimation	F = Decimation by 16 in HDF
20-5	Scaling Multiplier Gain	8000 = Scaling Multiplier Gain of 1.
4-3	Output Format	00 = Two's Complement
2-1	Number of Output Bits	00 =16 Bits
0	Output Sense	1 = MSB First

TABLE 15. SAMPLE FORMAT FOR CONTROL WORD 6 - OUTPUT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	110 = Control Word 6
36	Update	1 = Control Register update
35	I followed by Q	1 = I and Q data output on I pin
34-29	Time Slot	Time Slot number = 0
28	IQCLK Polarity	0 = Data stable on rising edge of IQCLK
27	IQCLK Duty Cycle	1 = IQCLK duty cycle is 50%
26	IQCLK Duration	1 = Active continuously
25-24	IQCLK Three State Control	01 = Enable IQCLK
23	IQSTB Polarity	0 = IQSTB active high
22	IQSTB Location	0 = IQSTB active prior to the beginning of the data word.
21-20	IQSTB Three State	01 = Enable IQSTB
19	I Polarity	0 = I output active high
18-17	I Three State Control	01 = Enable I
16	Q Polarity	0 = Q output active high
15-14	Q Three State Control	00 = Disable Q
13	Input Format	1 = Two's complement
12-0	IQCLK Rate	All zeroes = CLK used to clock output bits

Quadrature To Real Conversion

After the input data has been processed by the DDC, the output can be converted into a real signal if desired. In that case, the baseband centered quadrature signal is upconverted so that the bottom of the spectrum is at baseband. The real part of the upconverted signal is taken as the output. To satisfy the Nyquist criteria, the sample rate of the resulting signal must be at least twice the minimum sample rate of the I and Q components of the quadrature signal. This prevents one sideband from aliasing onto the other sideband when the real part of the output signal is taken.

The spectrum of a quadrature signal which has been over sampled by 2 is shown in Figure 16a. This represents the output of the filters. As described in the previous paragraph, the oversampling is a necessary feature of this process, since the final signal will occupy twice the bandwidth of the filter output. To prevent aliasing upon taking the real part of the signal, it is necessary to perform an up conversion by f"/4, where f" is the decimated sample frequency. (Note that f_s is defined as the input sampling frequency, f' is the input sampling frequency divided by the HDF decimation rate R, and f" is f' divided by the FIR decimation rate. f" is the output sampling rate.) The up conversion function is:

$$e^{j2\pi nf"/4f"} = e^{j\pi n/2}$$

For n = 0, 1, 2, 3, 4,... the output values of the local oscillator in rectangular representation are: 1 + 0j, 0 + j, -1 + 0j, 0 - j, 1 + 0j,.... Since the real half of the complex multiplication of the local oscillator values by the filtered signal values (the desired output is the real part of the product) require only trivial operations, this up conversion is done in the Formatter. Figure 16b shows the signal spectrum after up conversion. Figure 16c shows the spectrum of the real output signal.

Continuing with the single tone example from the previous section, the quadrature signal output from the FIR filters is:

$$\begin{aligned} w(n) &= \cos((\omega_K - \omega_c)n) + j\sin((\omega_K - \omega_c)n) \\ &= e^{j(\omega_K - \omega_c)n} \end{aligned}$$

Multiplying w(n) by the up convert function and summing the result is equivalent to the output sequence:

$$\begin{aligned} &y(n) = 1 \times \cos((\omega_K - \omega_c)n), \\ &y(n+1) = j \times j\sin((\omega_K - \omega_c)(n+1)), \\ &y(n+2) = -1 \times \cos((\omega_K - \omega_c)(n+2)), \\ &y(n+3) = -j \times j\sin((\omega_K - \omega_c)(n+3)), \\ &y(n+4) = 1 \times \cos((\omega_K - \omega_c)(n+4)),... \end{aligned}$$

$$\begin{aligned} y = {} & \cos((\omega_K - \omega_c)n), -\sin((\omega_K - \omega_c)(n+1)), \\ & -\cos((\omega_K - \omega_c)(n+2)), \sin((\omega_K - \omega_c)(n+3)), \\ & \cos((\omega_K - \omega_c)(n+4)),... \end{aligned}$$

Or:

$$\begin{aligned} y = {} & RE(w(n)), - IM(w(n+1)), - RE(w(n+2)), IM(w(n+3)), \\ & RE(w(n+4)),... \end{aligned}$$

Since $|e^{j\pi n/2}| = 1$ and $|w(n)| = 1$, no further magnitude corrections are required.

The setup for this application is similar to that of the down conversion circuit given above, except the Output Formatter is set for Real Mode (bit 31 in Control Word 4). This bit configures the part for up conversion by f"/4 and summing of the real and imaginary parts of the filter output.

Up Conversion by f"/2

This operation allows the user to exchange the positions of the upper and lower halves of a down converted signal while leaving each half unchanged. Quadrature up conversion by f"/2 is performed by multiplying the output signal by $e^{j2\pi nf"/2} = \cos(2\pi nf"/2) + j\sin(2\pi nf"/2)$. When sampled at a rate of f", $\cos(2\pi nf"/2)$ takes on the values 1, -1, 1, -1,... and $\sin(2\pi nf"/2)$ always = 0. Thus, the up convert LO sequence is:

$$e^{j\pi n} = 1 + j0, -1 + j0, 1 + j0, \ldots$$

This sequence is multiplied by the output of the I and Q branches of the filter:

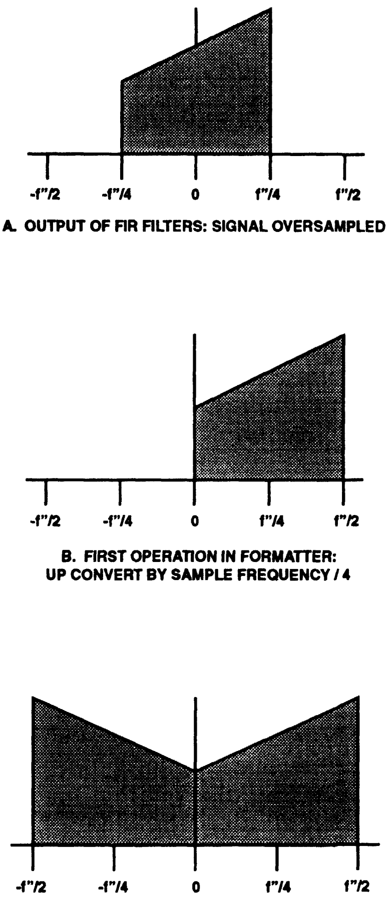
$$\begin{aligned} w(n) &= \cos((\omega_K - \omega_c)n) + j\sin((\omega_K - \omega_c)n) \\ &= e^{j(\omega_K - \omega_c)n}, \end{aligned}$$

yielding an output sequence:

$$\begin{aligned} y = {} & (RE(w(n)), IM(w(n))), \\ & -RE(w(n+1)), - IM(w(n+1))), \\ & RE(w(n+2)), IM(w(n+2))), \ldots \end{aligned}$$

The Formatter contains the circuitry to shift the quadrature output spectrum up by one half of the output sample frequency f". This operation is independent of the function of the Phase Generator and Mixer. The spectra of the outputs of the Filter and Formatter are shown in Figure 17.

The setup is identical to the down conversion configuration, except that the Up Convert bit is set in Control Word 4.



C. SECOND OPERATION IN FORMATTER: I OUTPUT = I + Q

FIGURE 16. QUADRATURE TO REAL CONVERSION OF AN OUTPUT SIGNAL

Quadrature Spectral Reversal

Spectral reversal is often used to negate a spectral reversal which has occurred due to a previous operation in the processing chain. Examples of this are spectral reversal in an analog down conversion or in a constructive aliasing operation. The DDC gives the user the ability to convert the signal to baseband in either forward or reverse fashion. Quadrature spectral reversal is achieved by translating the lower sideband of the input to baseband rather than the upper sideband. This is implemented in the DDC by mixing the input signal with $e^{j2\pi f_c n}$ - that is, up converting the input rather than down converting it. The resulting signal is:

$$u(n) = x(n)e^{j2\pi f_c n} = x(n)[\cos(\omega_c n) + j\sin(\omega_c n)]$$

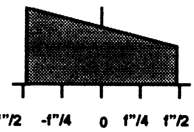
Assuming $x(n) = \cos(\omega_k n)$,

$$\begin{aligned} u(n) &= \cos(\omega_k n)[\cos(\omega_c n) + j\sin(\omega_c n)] \\ &= [\cos((\omega_k - \omega_c)n) + \cos((\omega_k + \omega_c)n) \\ &\quad + j(\sin((\omega_k + \omega_c)n) - \sin((\omega_k - \omega_c)n))] \end{aligned}$$

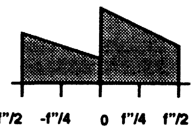
After quadrature filtering and correcting for the gain of 1/2, we have:

$$\begin{aligned} w(n) &= \cos((\omega_k - \omega_c)n) - j\sin((\omega_k - \omega_c)n) \\ &= \cos(-(\omega_k - \omega_c)n) + j\sin(-(\omega_k - \omega_c)n) \\ &= \cos((\omega_c - \omega_k)n) + j\sin((\omega_c - \omega_k)n) \end{aligned}$$

$$= e^{j(\omega_c - \omega_k)n}$$



A. OUTPUT OF FIR FILTERS



B. FILTER OUTPUT UP CONVERTED BY OUTPUT SAMPLE FREQUENCY / 2

FIGURE 17. UP CONVERSION BY F" / 2

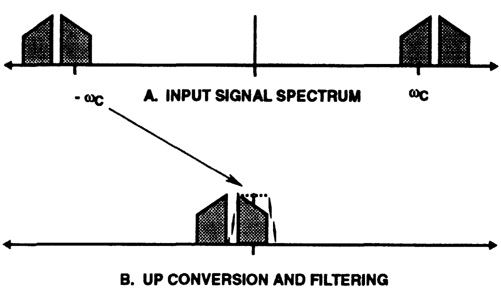


FIGURE 18. UP CONVERSION OF FILTER OUPUT SIGNAL

The appropriate spectral plots are shown in Figure 18. In up conversion, the sine output of the SIN/COS Generator is negated so that the vector output of the Local Oscillator rotates counter clockwise. This is implemented by setting the Spectral Reverse bit in Control Word 4 to a one. Otherwise, the setup for this mode is the same as the one for down conversion.

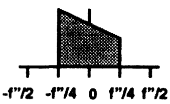
Real Spectral Reversal

Real spectral reversal is simply quadrature spectral reversal with quadrature to real conversion in the Formatter. The up converted and filtered signal w(n) is upconverted again by f"/ 4 in the Formatter.Each sideband of the result is spectrally reversed from the sidebands that would have been produced by down conversion with quadrature to real conversion. The output spectrum is shown in Figure 19.

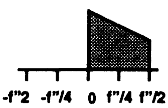
The setup for this application is similar to that of down conversion, except in control word 4, where the Spectral Reverse and Real Output bits are set to one.

High Decimation Filter Only

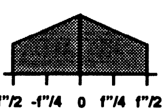
The DDC can be operated as a single high decimation filter. This is done by setting the Phase Generator to Filter Only and the Minimum Phase Increment and Phase Offset to 0. This multiplies the incoming data stream by a constant hexadecimal 3FFFF in the I channel and 0 in the Q channel. The HDF section of the circuit requires a minimum decimation rate of 16 to allow sufficient time for the FIR to compute its response. This mode of operation implements a filter which has a decimation rate from 64 to 131,072. The frequency response is shown in Figures 7, 8 and 9. Only the I output has valid data in this mode; the Q output should be set to high impedance state to reduce circuit noise.



A. OUTPUT OF FILTERS: SIGNAL OVERSAMPLED BY 2



B. FIRST OPERATION IN FORMATTER: UP CONVERT BY SAMPLE FREQUENCY / 4



C. SECOND OPERATION IN FORMATTER: I OUTPUT = I + Q

FIGURE 19. QUADRATURE TO REAL CONVERSION OF AN OUTPUT SIGNAL

6

DOWN CONV. AND DEMODULATION

Multichannel Operation

Several DDCs can be placed in parallel with each one operating on a different frequency band. To minimize wiring, their outputs can be configured so that they are connected over a common serial bus. Each DDC is assigned a time slot number (Control Word 6) and a time slot length (Control Word 3). Each DDC in turn controls the bus for long enough to output its data, then relinquishes the bus. The time slot assignment and length are programmed at configuration time. Up to 64 chips can be multiplexed in this manner.

Figure 20 shows a block diagram of this configuration. The DDCs are configured by the microprocessor by first writing a logical 0 to its Chip Select line. The control words are written to that part in any order. When the part has been configured, CS# is written high again, and the next part is configured in the same manner. Collisions are prevented by programming each DDC with a unique Time Slot number, which holds its output from 0 to 63 output word times before transmission. Each part also has a Time Slot Length, whose minimum value is given in equation 8. Note that a value greater than the minimum can be used to give the processor time to operate on the data

The corresponding configuration register setup is similar to that of single channel down conversion, except for the Auto Three State fields. In this example, the first DDC in the chain is set to drive IQCLK; the others have this output set for high impedance. (It makes no difference which DDC is chosen to be the one to drive IQCLK, but it must be active continuously.) The unused outputs are put in their high impedance condition on the other DDCs to minimize power consumption. Note also that this example shows all DDCs in I followed by Q mode so that only one data line to the microprocessor is necessary. Figure 21 gives the timing of the output data.

Alternatively, the processor can request data from each of the DDCs asynchronously. In this setup, Requested Output Mode is used. The Data Concentrator polls each channel individually and is responsible for insuring that each channel is polled before the output data is lost. The Data Concentrator is a custom circuit designed by the user. A block diagram of such a system is shown in Figure 22. The interface between the controller and the DDCs has been omitted for the sake of clarity.

References

[1] Hogenauer, Eugene V., An Economical Class of Digital Filters for Decimation and Interpolation, IEEE Transactions on Acoustics, Speech and Signal Processing, April 1981

[2] IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1 - 1990

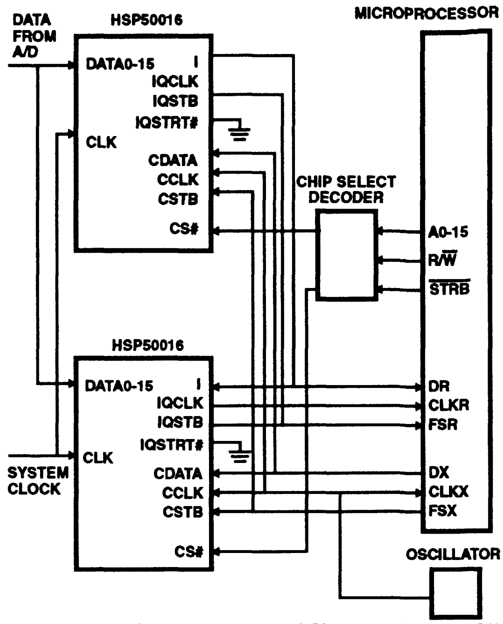


FIGURE 20. CIRCUIT FOR MULTIPLE CHANNEL OPERATION (AUTO THREE STATE)

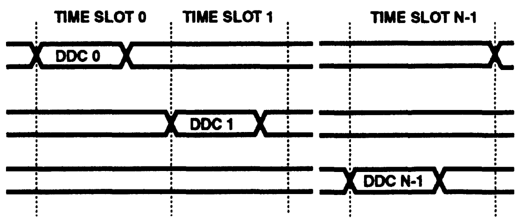


FIGURE 21. TIMING FOR MULTIPLE CHANNEL OPERATION (AUTO THREE STATE)

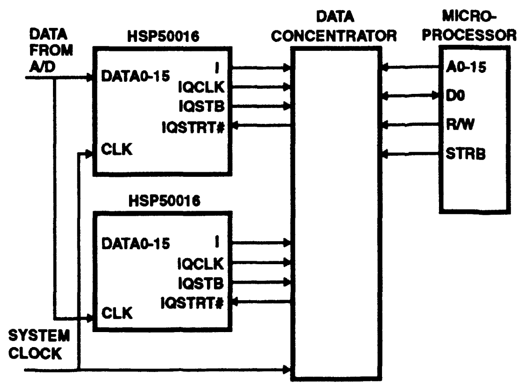


FIGURE 22. CIRCUIT FOR MULTIPLE CHANNEL OPERATION (REQUESTED OUTPUT)

Absolute Maximum Ratings

Supply Voltage .... +7.0V
Input, Output or I/O Voltage .... GND-0.5V to VCC+0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature............ +175°C (PGA), +150°C(PLCC)
Lead Temperature (Soldering 10s).................... +300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
PGA Package	41°C/W	5°C/W
PLCC Package	35°C/W	13°C/W

Maximum Package Power Dissipation at 70°C
PGA Package 1.95W
PLCC Package 2.28W
Gate Count .... 65,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range................... +4.75V to +5.25V
Operating Temperature Range .... 0°C to +70°C

DC Electrical Specifications V_{CC} = 5.0V 5%, T_A = 0° to +70°C

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Power Supply Current	I_{CCOP}	-	394	mA	V_{CC} = Max,CLK Frequency 52.6MHz Notes 1,2
Standby Power Supply Current	I_{CCSB}	-	500	µA	V_{CC} = Max, Outputs Not Loaded
Input Leakage Current	I_I	-500	10	µA	V_{CC} = Max, Input = 0V or V_{CC} TMS, TDI, TRST#
		-10	10	µA	V_{CC} = Max, Input = 0V or V_{CC} All other inputs
Output Leakage Current	I_O	-10	10	V	V_{CC}= Max, Input = 0V or V_{CC}
Logical One Input Voltage	V_{IH}	2.0	-	V	V_{CC} = Max
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = Min
Logical One Input Voltage: CLK, TRST#	V_{IHC}	3.0	-	V	V_{CC} = Max
Logical One Output Voltage	V_{OH}	2.6	-	V	I_{OH} = -5mA, V_{CC} = Min
Logical Zero Output Voltage	V_{OL}	-	0.4	V	I_{OL} = 5mA, V_{CC} = Min
Input Capacitance	C_{IN}	-	10	pF	CLK Frequency 1MHz All measurements referenced to GND. T_A = +25°C, Note 3
Output Capacitance	C_{OUT}	-	10	pF	

NOTES:

1. Power supply current is proportional to frequency. Typical rating is 7.5mA/MHz. Note that operation at maximum clock frequency will exceed maximum junction temperature of device. Use of a heat sink and/or air flow is required under these conditions: recommended heat sink is EG&G Wakefield D10650-40.
2. Output load per test circuit and CL= 40pF.
3. Not tested, but characterized at initial design and at major process/design changes.

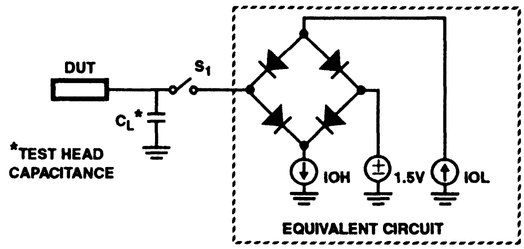
AC Electrical Specifications V_{CC} = 5.0V ±5%, T_A = 0° to +70°C, (Note 1)

PARAMETER	SYMBOL	-52(52.6)MHz MIN	-52(52.6)MHz MAX	PRELIMINARY -75(76.9)MHz MIN	PRELIMINARY -75(76.9)MHz MAX	TEST CONDITIONS
CLK Period	T_{CP}	19	-	13	-	ns
CLK High	T_{CH}	7	-	5	-	ns
CLK Low	T_{CL}	7	-	5	-	ns
Setup Time DATA0-15 to CLK	T_{DS}	10	-	7	-	ns
Hold Time DATA0-15 from CLK	T_{DH}	1	-	1	-	ns
RESET# Pulse Width	T_{RL}	T_{CP}+11	-	T_{CP}+8	-	ns
RESET#, IQSTRT# Setup Time from CLK	T_{RS}	10	-	7	-	ns, Note 2
RESET#, IQSTRT# Hold Time to CLK	T_{RH}	1	-	1	-	ns, Note 2
CLK to I, Q, IQSTB, IQCLK Delay	T_{DO}	-	15	-	12	ns
CCLK Period	T_{CCP}	100	-	100	-	ns
CCLK High	T_{CCH}	40	-	40	-	ns
CCLK Low	T_{CCL}	40	-	40	-	ns
CDATA, CSTB, CS# Setup to CCLK	T_{CDS}	30	-	30	-	ns
CDATA, CSTB, CS# Hold from CCLK	T_{CDH}	30	-	30	-	ns
CCLK Low Setup to CLK	T_{CLS}	30	-	30	-	ns, Notes 2, 3
CCLK High Hold from CLK	T_{CHH}	30	-	30	-	ns, Notes 2, 3, 6
TCK Period	T_{TP}	100	-	100	-	ns, Note 4
TCK High	T_{TH}	40	-	40	-	ns
TCK Low	T_{TL}	40	-	40	-	ns
TRST# Pulse Width	T_{TRL}	100	-	100	-	ns
TCK to TDO, Data delay	T_{TDO}	-	30	-	30	ns
Setup Time On All Inputs to TCK	T_{ATS}	30	-	30	-	ns, Note 5
Hold Time On All Inputs from TCK	T_{ATH}	30	-	30	-	ns, Note 5
TCK Setup Time to CLK	T_{TCS}	30	-	30	-	ns, Note 4
TCK Hold Time from CLK	T_{TCH}	30	-	30	-	ns, Note 4
Output Enable Time from CLK	T_{OE}	-	18	-	12	ns, Note 6
Output Disable Time from CLK	T_{OD}	-	18	-	12	ns, Note 6
Output Enable time from TCK	T_{TOE}	-	32	-	32	ns, Note 6
Output Disable time from TCK	T_{TOD}	-	32	-	32	ns, Note 6
Output rise, fall time	T_{RF}	-	5	-	5	ns, Note 6

NOTES:

1. AC tests performed with C_L= 40 pF, I_{OL} = 5mA, and I_{OH} = -5mA. Input reference level for CLK, TRST# is 2.0V, all other inputs 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V; V_{OH} = V_{OL} = 2.5V.
2. These are asynchronous inputs; setup and hold times must only be maintained in order to predict which clock cycle they take effect internally.
3. Timing must only be maintained when Update bit is active in control word data being loaded.
4. Special Timing relationship between TCK and CLK is required for Test Instructions RUNBIST, EXTEST and INTEST.
5. All inputs except TRST#, and only when TCK is driving internal clock.
6. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

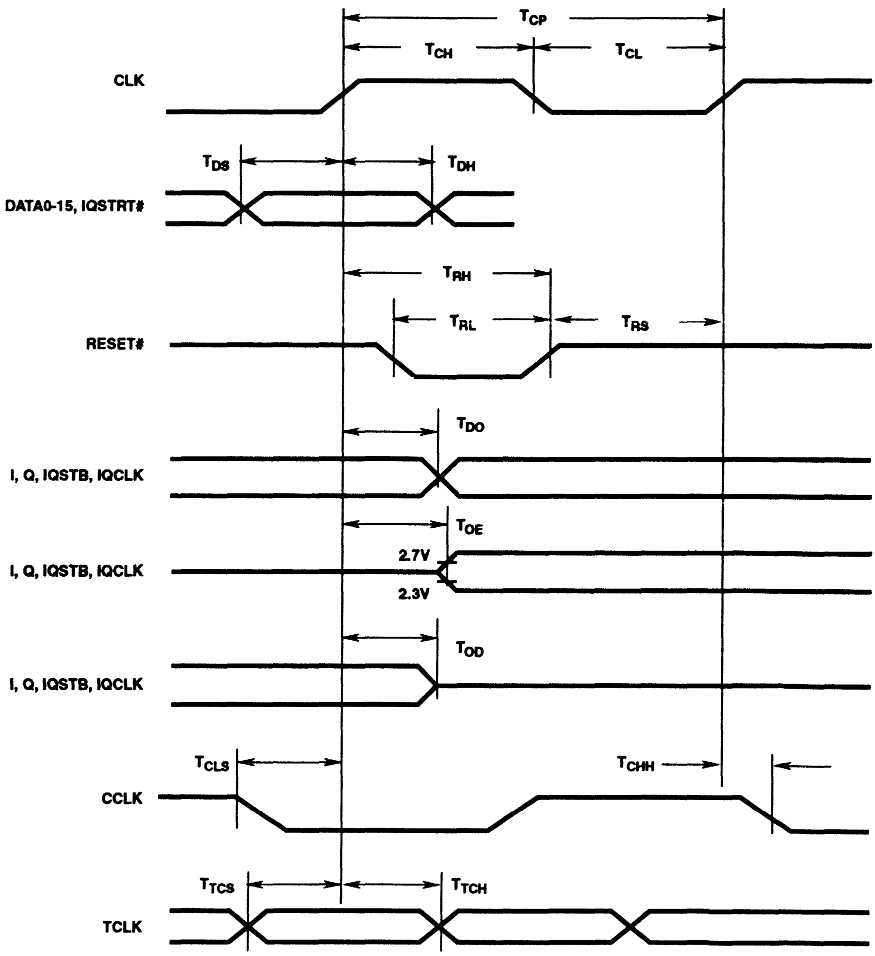
AC Test Load Circuit



SWITCH S1 OPEN FOR I_{CCSB} AND I_{CCOP}

Waveforms

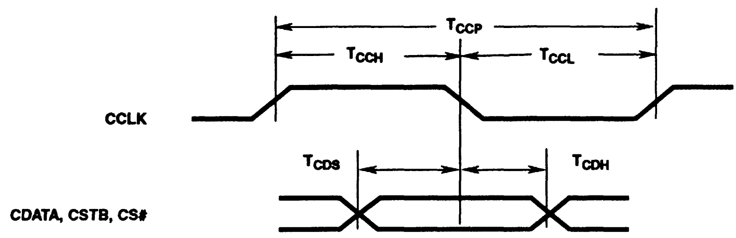
TIMING RELATIVE TO CLK



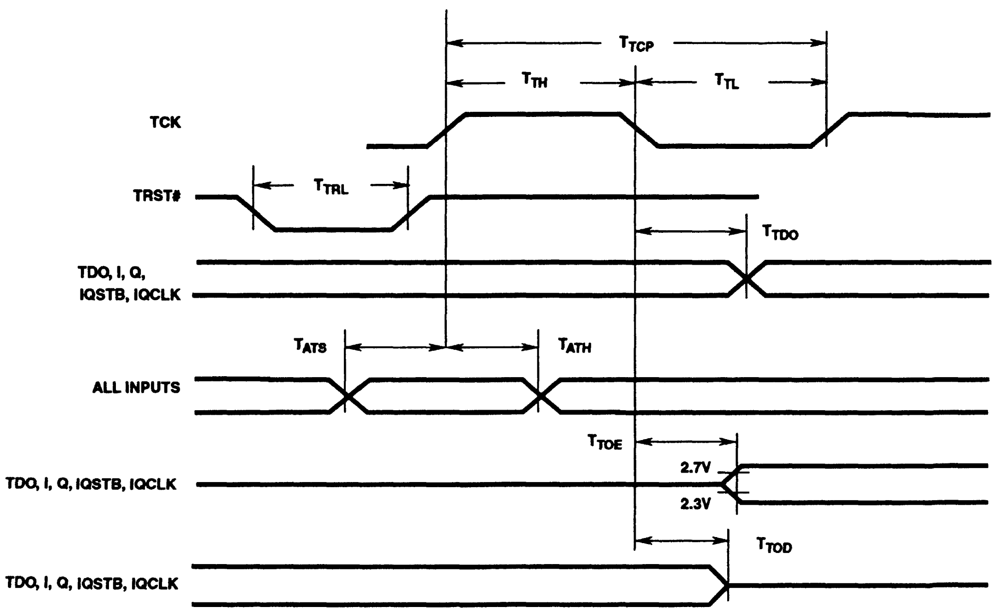
6 DOWN CONV. AND DEMODULATION

Waveforms (Continued)

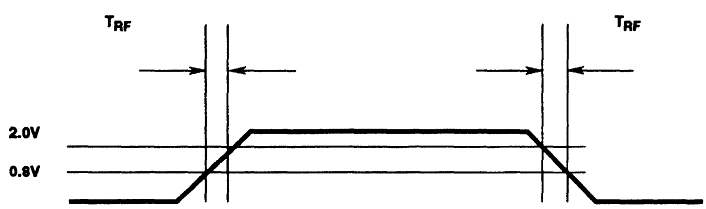
TIMING RELATIVE TO CCLK



TIMING RELATIVE TO TCK



OUTPUT RISE AND FALL TIMES



HARRIS SEMICONDUCTOR

HSP50110

ADVANCE INFORMATION

February 1994

Digital Quadrature Tuner

Features

- **10 bit Real or Complex Inputs**
- **Frequency Selectivity <0.014Hz**
- **Data Rates to 60MSPS**
- **Third Order Cascaded-Integrator-Comb (CIC) Filter configurable as Integrate and Dump Filter (First Order CIC) or Bypassable**
- **Decimation from 1-4096, or Set by Resampling NCO used for Bit Synchronization**
- **Error Detection for External IF AGC Loop**
- **Internal AGC Loop for Output Level Stability**
- **Bi-Directional 8-Bit Microprocessor Interface**
- **Parallel or Serial Output Data Formats**

Applications

- **Phase and Frequency Modulation**
- **VSAT, INMARSAT Systems**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP50110JC-60	0°C to +70°C	84 Lead PLCC

Description

The Digital Quadrature Tuner (DQT) provides many of the functions needed for digital demodulation. These functions include carrier L.O. generation, symbol clock generation, preselection filtering, baseband AGC, and IF AGC error detection. The DQT facilitates many different digital implementations of demodulator tracking loops, which allows this chip to handle multiple modes and/or data rates simply by loading a new set of control words.

The DQT accepts digitized signals in either a real or complex representation. The digitized band of interest is shifted to DC through a complex multiplication by an internally generated L.O. The quadrature LO is generated by a numerically controlled oscillator (NCO) with a tuning resolution of approximately 14MHz at a clock rate of 60MHz and a spurious free dynamic range of 60dB. For added flexibility, a control interface is provided for real time phase and frequency updates.

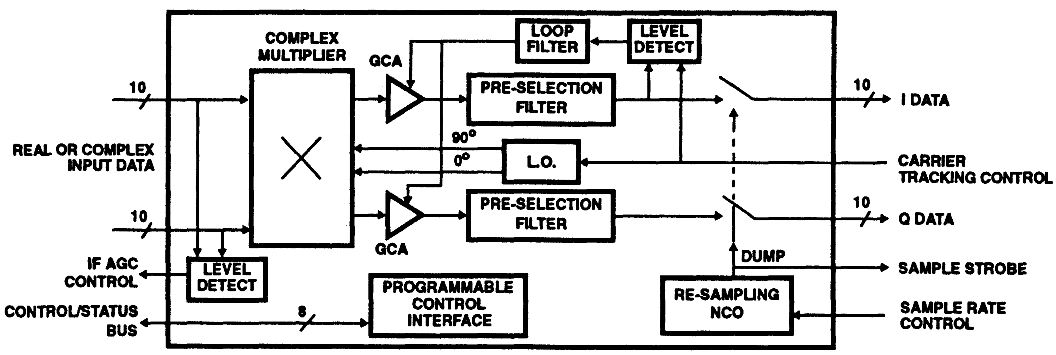
The output of the complex multiplier is gain corrected and feed into identical preselection filters on both the real and imaginary processing legs. Each preselection filter is comprised of a decimating low pass filter followed by a compensation filter. The decimating low pass filter is a 3 stage cascade-integrator-comb (CIC) filter. The CIC filter can be bypassed, configured as an integrate and dump filter with a sin(X)/X response, or a third order filter with a $(\sin(X)/X)^3$ response. The decimation of the CIC filter stage may be fixed from 1-4096, or it may be controlled by a re-sampling NCO used for bit synchronization. The compensation filter is user selectable for flattening the $(\sin(X)/X)^N$ response of the CIC. These onboard filters may be bypassed if custom external filtering is required.

Level detectors are provided to generate error signals for external/internal AGC loops. The DQT output is provided in either serial or parallel formats to support interfacing with a variety DSP processors or digital filter components. This device is configurable over a general purpose 8-bit parallel bidirectional microprocessor control bus.

6

DOWN CONV. AND DEMODULATION

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3651

DSP 7

SPECIAL FUNCTION

PAGE

SPECIAL FUNCTION DATA SHEETS

HARRIS SEMICONDUCTOR

HSP45240

February 1994

Address Sequencer

Features

- Block Oriented 24-Bit Sequencer
- Configurable as Two Independent 12-Bit Sequencers
- 24 x 24 Crosspoint Switch
- Programmable Delay on 12 Outputs
- Multi-Chip Synchronization Signals
- Standard µP Interface
- 100pF Drive on Outputs
- DC to 50MHz Clock Rate

Applications

- 1-D, 2-D Filtering
- Pan/Zoom Addressing
- FFT Processing
- Matrix Math Operations

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP45240JC-33	0°C to +70°C	68 Lead PLCC
HSP45240JC-40	0°C to +70°C	68 Lead PLCC
HSP45240JC-50	0°C to +70°C	68 Lead PLCC
HSP45240GC-33	0°C to +70°C	68 Lead PGA
HSP45240GC-40	0°C to +70°C	68 Lead PGA
HSP45240GC-50	0°C to +70°C	68 Lead PGA

Description

The Harris HSP45240 is a high speed Address Sequencer which provides specialized addressing for functions like FFTs,1-D and 2-D filtering, matrix operations, and image manipulation. The sequencer supports block oriented addressing of large data sets up to 24-bits at clock speeds up to 50MHz.

Specialized addressing requirements are met by using the onboard 24 x 24 crosspoint switch. This feature allows the mapping of the 24 address bits at the output of the address generator to the 24 address outputs of the chip. As a result, bit reverse addressing, such as that used in FFTs, is made possible.

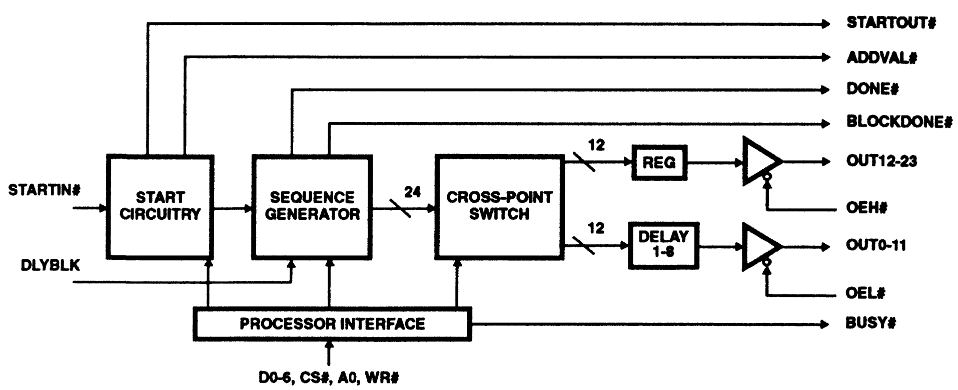
A single chip solution to read/write addressing is also made possible by configuring the HSP45240 as two 12-bit sequencers. To compensate for system pipeline delay, a programmable delay is provided on 12 of the address outputs.

The HSP45240 is manufactured using an advanced CMOS process, and is a low power fully static design. The configuration of the device is controlled through a standard microprocessor interface and all inputs/outputs, with the exception of clock, are TTL compatible.

7

SPECIAL FUNCTION

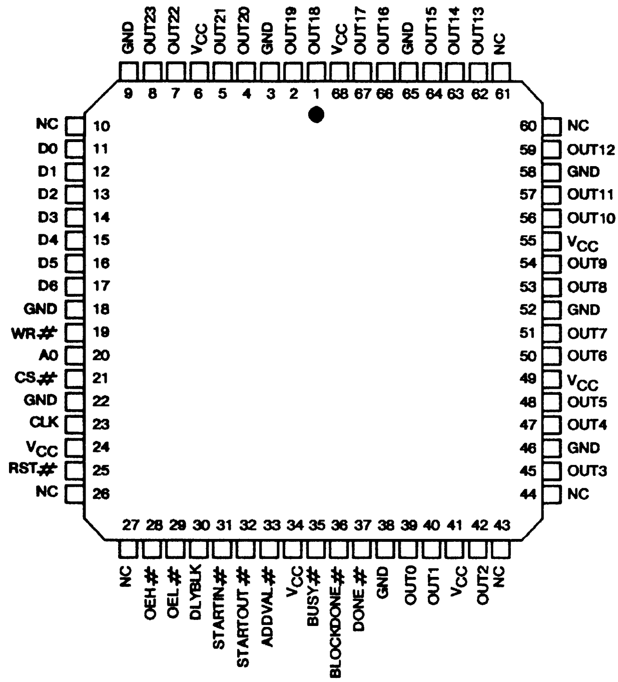
Block Diagram



File Number **2489.3**

Package Pinouts

ADDRESS SEQUENCER HSP45240
68 PIN PLASTIC LEADED CHIP CARRIER (PLCC)



68 PIN GRID ARRAY (PGA)
(BOTTOM VIEW)

	1	2	3	4	5	6	7	8	9	10	11
L		OEH#	DLYBLK	START OUT#	VCC	BLOCK DONE#	GND	OUT1	OUT2	NC	
K	NC	NC	OEL#	START IN#	ADD VAL#	BUSY#	DONE#	OUT0	VCC	NC	OUT3
J	RST#	VCC								GND	OUT4
H	CLK	GND								OUT5	VCC
G	CS#	A0								OUT6	OUT7
F	WR#	GND								GND	OUT8
E	D6	D5								OUT9	VCC
D	D4	D3								OUT10	OUT11
C	D2	D1								GND	OUT12
B	D0	NC	OUT22	OUT21	GND	OUT18	OUT17	GND	OUT14	NC	NC
A		GND	OUT23	VCC	OUT20	OUT19	VCC	OUT16	OUT15	OUT13	

Pin Descriptions

NAME	TYPE	PLCC PIN NUMBER	DESCRIPTION
V_{CC}	I	6,24,34,41 49,55,68	+5V power supply pin.
GND	I	3,9,18,22 38,46,52 58,65	GROUND
RST#	I	25	RESET: This active low input causes a chip reset which lasts for 26 clocks after RST# has been de-asserted. The reset initializes the Crosspoint Switch and some of the configuration registers as described in the Processor Interface section. The chip must be clocked for reset to complete.
CLK	I	23	CLOCK: The "CLK" signal is a CMOS input which provides the basic timing for address generation.
WR#	I	19	WRITE: The rising edge of this input latches the data/address on D0-6 to be latched into the Processor Interface.
CS#	I	21	CHIP SELECT: This active "low" input enables the configuration data/address on D0-6 to be latched into the Processor Interface.
A0	I	20	ADDRESS 0: This input defines D0-6 as a configuration register address if "high", and configuration data if "low", (see Processor Interface text).
D0-6	I	11-17	DATA BUS: Data bus for Processor Interface.
OEH#	I	28	OUTPUT ENABLE HIGH: This asynchronous input is used to enable the output buffers for OUT12-23.
OEL#	I	29	OUTPUT ENABLE LOW: This asynchronous input is used to enable the output buffers for OUT0-11.
STARTIN#	I	31	START-IN: This active low input initiates an addressing sequence. May be tied to STARTOUT# of another HSP45240 for multi-chip synchronization. STARTIN# should only be asserted for one CLK because address sequencing begins after STARTIN# is de-asserted.
DLYBLK	I	30	DELAY BLOCK: This active "high" input may be used to halt address generation on address block boundaries (see Sequence Generator text). The required timing relationship of this signal to the end of an address block is shown in Application Note 9205.
OUT0-23	O	39,40,42,45, 47,48,50,51, 53,54,56,57, 59,62-64,66, 67,1,2,4,5, 7,8	OUTPUT BUS: TTL compatible 24-bit Address Sequencer output.
BLOCKDONE#	O	36	BLOCK DONE: This active low output signals when the last address in an address block is on OUT0-23.
DONE#	O	37	DONE: This active low output signals when the last address of an address sequence is on OUT0-23.
ADDVAL#	O	33	ADDRESS VALID: This active low output signals when the first address of an address sequence is on OUT0-23.
STARTOUT#	O	32	START-OUT: This active low output is generated when an address sequence is initiated by a mechanism other than STARTIN#. May be tied to the STARTIN# of other HSP45240's for multichip synchronization.
BUSY#	O	35	BUSY: This active low output is asserted one CLK after RST# is de-asserted and will remain asserted for 25 CLK's. While BUSY# is asserted all writes to the Processor Interface are disabled.

# Denotes active low.

Functional Description

The Address Sequencer is a 24-bit programmable address generator. As shown in the Block Diagram, the sequencer consists of 4 functional blocks: the start circuitry, the sequence generator, the crosspoint switch, and the processor interface. The addresses produced by the sequence generator are input into the crosspoint switch. The crosspoint switch maps 24 bits of address input to a 24 bit output. This allows for addressing schemes like "bit-reverse" addressing for FFT's. A programmable delay block is provided to allow the MSW of the output to be skewed from the LSW. This feature may be used to compensate for processor pipeline delay when the sequence generator is configured as two independent 12 bit sequencers. Address Sequencer operation is controlled by values loaded into configuration registers associated with the sequence generator, crosspoint switch, and start circuitry. The configuration registers are loaded through the processor interface.

Start Circuitry

The Start Circuitry generates the internal START signal which causes the Sequence Generator to initiate an addressing sequence. The START signal is produced by writing the Processor Interface's "Sequencer Start" address (see Processor Interface text), by asserting the STARTIN# input, or by the terminal address of a sequence generated under "One-Shot Mode with Restart" (see Sequence Generator section). Care should be taken to assert STARTIN# for only one clock cycle to insure proper operation. A programmable delay from 1 to 31 clocks is provided to delay the initiation of an addressing sequence by delaying the internal START signal (see Processor Interface text).

The Start Circuitry generates the output signal ADDVAL# which is asserted when the first valid output address is at the pads. In addition, the Start Circuitry generates the "STARTOUT#" signal for multichip syncronization. Note: STARTOUT# is only generated when an addressing sequence is started by writing the "Sequencer Start" address of the Processor Interface, or an internal START is generated by reaching the end of an addressing sequence produced by "One-Shot Mode with Restart".

Sequence Generator

The Sequence Generator is a block oriented address generator. This means that the desired address sequence is subdivided into one or more address blocks each containing a user defined number of addresses. User supplied configuration data determines the number of address blocks and the characteristics of the address sequence to be generated.

As shown in Figure 1, the Sequence Generator is subdivided into the an address generation and control section. The address generation section performs an accumlation based on the output of MUX1 and MUX2. The control section governs the operation of the multiplexers, enables loading of the Block Start Address register, and signals completion of an address sequence.

An address sequence is started when the control section of the Sequence Generator receives the internal START signal from the Start Circuitry. When the START signal is received, the control section multiplexes the contents of the Start Address Register and a "0" to the adder. The result of this summation is the first address in the first block of the address sequence. This value is stored in the Block Start Address register by an enable generated from the control section, and the multiplexers are switched to feed the output of the Holding and Address Increment registers to the adder. Address generation will continue with the Address Increment added to the contents of the Holding Register until the first address block has been completed.

An address block is completed when the number of addresses generated since the beginning of the address block equals the value stored in the Block Size register. When the last address of the block is generated, BLOCKDONE# is asserted to signal the end of the address block (see Application Note 9205). On the following CLK, the multiplexers are configured to pass the contents of the Block Start Address and Block Increment registers to the adder which generates the first address of the next address block. An enable from the control section allows this value to update the Block Start Address register, and the multiplexers are switched to feed the Holding and Address Increment registers to the adder for generation of the remaining addresses in the block.

The address sequence is completed when the number of address blocks generated equals the value loaded into the Number of Blocks register. When the final address in the last address block has been generated, DONE# and BLOCKDONE# are asserted to signal the completion of the address sequence.

The parameters governing address generation are loaded into five 24-bit configuration registers via the Processor Interface. These parameters include the Start Address, the beginning address of the sequence; the Block Size, the number of addresses in the address block; the Address Increment, the increment between addresses in a block; the Number of Blocks, the number of address blocks in a sequence (minimum 1); the Block Increment, the increment between starting addresses of each block. The loading and structure of these registers is detailed in the Processor Interface text.

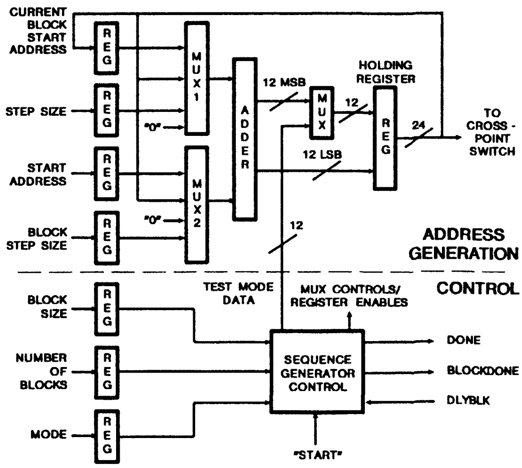


FIGURE 1. SEQUENCE GENERATOR BLOCK

Three modes of operation may be selected by loading the 6-bit Mode Control register (see Processor Interface). The three modes of operation are:

1. One-Shot Mode without Restart Address generation halts after completion of the user specified address sequence. Address generation will not resume until the internal START signal is generated by the Start Circuitry. When the final address in the final block of the address sequence is generated, both DONE# and BLOCKDONE# are asserted and the last address is held on OUT0-23 (See Application Note 9205). 2.
2. One-Shot Mode with Restart: This mode is identical to One-Shot Mode without Restart with the exception that the Start Circuitry automatically generates an internal START at the end of the user specified sequence to restart address generation. The end of the address sequence is signaled by the assertion of DONE#, BLOCKDONE#, and STARTOUT# as shown in Application Note 9205. In this mode, the first address of the next sequence immediately follows the last address of the current sequence if start delay is disabled.
3. Continuous Mode: Address generation never terminates. Address generation proceeds based on the Start Address, Address Increment, Block Size, and Block Increment Parameters. The Number of Blocks parameter is ignored, and the DONE# signal is never asserted.

The Mode Control register is also used to configure the Sequence Generator for operation as two independent 12-bit address sequencers. In dual sequencer mode, the adder in the sequence generator suppresses the carry from the 12 LSBs to the 12 MSBs. With the carry suppressed, two independent sequences may be produced. These 12-bit address sequences may be delayed relative to each other by programming the Mode Control register for a delay up to 7 clocks. This feature is useful to compensate for pipeline delay when using dual sequencer mode to generate read/write addressing.

The DLYBLK input can be used to halt address generation at the end of any address block within a sequence. In addition, DLYBLK can be used to delay an address sequence from restarting if asserted at the end of the final address block generated under "One-Shot Mode with Restart". See Application Note 9205 for the timing relationship of DLYBLK to the end of the address block required to halt address sequencing.

Crosspoint Switch

The crosspoint switch is responsible for reordering the address bits output by the sequence generator. The switch allows any of its 24 inputs to be independently connected to any of its 24 outputs. The crosspoint switch outputs can be driven by only one input, however, one input can drive any number of switch outputs. If none of the inputs are mapped to a particular output bit, that output will be "low".

The input to output map is configured through the processor interface. The I/O map is stored in a bank of 24 configuration registers. Each register corresponds to one output bit. The output bit is mapped to the input via a value, 0 to 23, stored in the register. After power-up, the user has the option of configuring the switch in 1:1 mode by using the reset input, "RST#". In 1:1 mode the cross-point switch outputs are in the same order as the input. More details on configuring the switch registers are contained in the Processor Interface text.

Processor Interface

The Processor Interface consists of a 10 pin microprocessor interface and a register bank which holds configuration data. The data is loaded into the register bank by first writing the register address to the processor Interface and then writing the data. An auto address increment mode is provided so that a base address may be written followed by a number of data writes.

The microprocessor interface consists of a 7 bit data bus (D0-6), a one bit address select (A0) to specify D0-6 as either address or data, a write input (WR#) to latch data into the Processor Interface, and a chip select input (CS#) to enable writing to the interface. The Processor Interface input is decoded as either data or address as shown by the bit map in Table 1.

TABLE 1.

	A0	D6	D5	D4	D3	D2	D1	D0
REGISTER ADDRESSES								
Switch Output Registers	1	x	0	n	n	n	n	n
Sequencer Starting Address	1	x	1	0	0	0	n	n
Sequencer Block Size	1	x	1	0	0	1	n	n
Sequencer Number of Blocks	1	x	1	0	1	0	n	n
Sequencer Block	1	x	1	0	1	1	n	n
Address Increment								
Sequencer Address	1	x	1	1	0	0	n	n
Increment								
Mode Control	1	x	1	1	0	1	0	0
Test Control	1	x	1	1	0	1	0	1
Start Delay Control	1	x	1	1	0	1	1	0
Address Sequencer "START"	1	x	1	1	1	1	1	1
DATA WORDS								
Current Address Data	0	0	n	n	n	n	n	n
(no address increment)								
Current Address Data (address increment)	0	1	n	n	n	n	n	n

NOTES:

1. Table 1 "x" means "don't care", and "n" denotes bits which are decoded as an address in address registers and data in data registers.
2. When WR# transitions "high" to write the Sequencer "Start" address (1x111111), it must remain high until after a rising edge of clock. Otherwise, the sequencer "start" signal will not be generated.

The register bank consists of a series of 6 bit registers which may be addressed individually as shown in Table 1. The data in these registers is down loaded into configuration registers in the Start Circuitry, Sequence Generator, and Crosspoint Switch when an address sequence is initiated by the internal START signal (see Start Circuitry). This double buffered architecture allows new configuration data to be down loaded to the Processor Interface while an address sequence is being completed using previous configuration data.

The register bank has five sets of four registers which contain address generation parameters. These parameters include: Address Start, Block Size, Number of Blocks, Block Increment, and Address Increment. Each register set maps to one of five 24-bit configuration registers in the Sequence Generator block (see Sequence Generator). The mapping of the 6-bit registers in the register bank to the 24-bit configuration registers is determined by the 2 LSB's of the register address. The higher the value of the 2 LSB's the higher the relative mapping of the 6-bit register to the 24-bit register. For example, if the 2 LSB's of the register address are both 0, the register contents will map to the 6 LSB's of the configuration register.

The register bank has 24 registers which contain the data for Crosspoint Switch I/O mapping. These registers are accessed via the 5 LSB's of the address for the Crosspoint Mapping registers in Table 1. A value from 0 to 23 accesses the mapping registers for OUT0-23 repectively. A value greater than 23 is ignored. The output bit represented by a particular register is mapped to the input by the 6-bit value loaded into the register. If the value loaded into the register exceeds 23, the correponding output bit will be "0". For example, if the 5 LSB's of the Crosspoint Mapping address are equal to 3, and the valued loaded into the register accessed by this address is equal to 23, OUT3 would be mapped to the MSB of the sequence generator output.

After a reset, the Mode Control, Test Control, and Start Delay registers are reset as described in the section describing each register's bit map; the Crosspoint Mapping registers are reset to a 1:1 crosspoint switch mapping; the registers which hold the five address generation parameters are not affected.

To save the user the expense of alternating between address and data writes, an auto address increment mode is provided. The address increment mode is invoked by performing data writes with a "1" in the D6 location of the data word as shown in Table 1. For example, the crosspoint switch could be configured by 25 writes to the Processor Interface (one write for the starting address of the crosspoint mapping registers followed by 24 data writes to those registers).

Mode Control Register

The Mode Control Register is used to control the operation of the sequence generator. In addition, it also controls the output delay between the MSW and the LSW of OUT0-23. The following tables illustrate the structure of the mode control register.

TABLE 2. MODE CONTROL REGISTER FORMAT

ADDRESS LOCATION: 1x110100					
D5	D4	D3	D2	D1	D0
OD2	OD1	OD0	DS	M1	M0

ODx - Output Delay: Delays OUT0-11 from OUT12-23 by the following number of clocks.

OD2	OD1	OD0	
0	0	0	Output Delay of 0
0	0	1	Output Delay of 1
0	1	0	Output Delay of 2
0	1	1	Output Delay of 3
1	0	0	Output Delay of 4
1	0	1	Output Delay of 5
1	1	0	Output Delay of 6
1	1	1	Output Delay of 7

DS - Dual Sequencer Enable: Allows two independent 12- bit sequences to be generated.

0	A 24-bit sequence is generated.
1	Two 12-bit sequences are generated.

Mx - Mode: Sequencer Mode.

M1	M0	
0	0	One-Shot Mode without Restart
0	1	One-Shot Mode with Restart
1	x	Continuous Mode (x = don't care)

During reset, this register will be reset to all zeroes. This will configure the chip as a 24-bit sequencer with zero delays on the outputs. The chip will also be in one-shot mode without restart.

Start Delay Control Register

The Start Delay Control Register is used to configure the start circuitry for delayed starts from 1 to 31 clock cycles. Internal "START", external "START", and restarts will be delay by the programmed amount. The structure of the Start Delay Control Register is shown in Table 3.

TABLE 3. START DELAY CONTROL REGISTER FORMAT

ADDRESS LOCATION: 1x110110					
D5	D4	D3	D2	D1	D0
SDE	SD4	SD3	SD2	SD1	SD0

SDE - Start Delay Enable: Enables "START" to be delayed by the programmed amount. When Start Delay is enabled, a minimum of "1" is required for the programmed delay.

0	Start Delay is Disabled.
1	Start Delay is Enabled.

SDx - Start Delay: Delays the "START" by the decoded number of clocks.

SD4	SD3	SD2	SD1	SD0	
0	0	0	0	1	Start Delay of 1
0	0	0	1	0	Start Delay of 2
0	0	0	1	1	Start Delay of 3
1	1	1	1	1	Start Delay of 31

During reset, this register will be reset to all zeros. This will bring the chip up in a mode with Start Delay disabled.

Test Control Register

A Test Control Register is provided to configure the sequence generator to produce test sequences. In this mode, the sequence generator can be configured to multiplex out the contents of the down counters in the sequence generator control circuitry, Figure 2. These counters are used to determine when a block or sequence is complete. As shown in Figures 1 and 2, the MSW or LSW in the down counters is multiplexed to the MSW of the address generator output. In addition, a test mode is provided in which the sequence generator performs a shifting operation on the contents of the start address register. The structure of the Test Control Register is shown in Table 4.

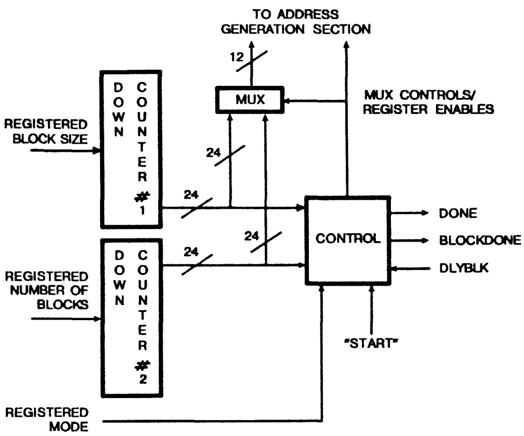


FIGURE 2. SEQUENCE GENERATOR CONTROL

TABLE 4. TEST CONTROL REGISTER FORMAT

ADDRESS LOCATION: 1x110101					
D5	D4	D3	D2	D1	D0
xx	xx	SE	COE	CS1	CS0

Bits "D5" and "D6" are currently not used.

SE - Shifter Enable: Input to crosspoint switch is generated by shifting Start Address Register one bit per clock.

0	Sequence Generator Functions Normally
1	Sequence Generator Functions as Shift Register

COE - Counter Output Enable: Enable contents of down counters in the sequence generator control circuitry to be muxed to the 12 MSB's of the address generator output.

0	Disable Muxing of down counters
1	Enable Muxing of down counters

CS - Counter Select: Selects which 12-bit word of the down counters is muxed to the MSW of the address generator output.

CS1	CS0	
0	0	Select Counter #1, bits 0-11
0	1	Select Counter #1, bits 12-23
1	0	Select Counter #2, bits 0-11
1	1	Select Counter #2, bits 12-23

During reset, this register will be reset to all zeroes. This will bring the chip up in the mode with all of the test features disabled.

Applications

Image Processing

The application shown in Figure 3 uses the HSP45240 Address Sequencer to satisfy the addressing requirements for a simple image processing system. In this example the controller configures the sequencers to generate specialized addressing sequences for reading and writing the frame buffers. A typical mode of operation for this system might be to perform edge detection on a sub-section of an image stored in the frame buffer. In this application, data is fed to the 2-D Convolver by the address sequence driving the input frame buffer.

A graphical interpretation of sub-image addressing is shown in Figure 4. Each dot in the figure corresponds to an image pixel stored in memory. It is assumed that the pixel values are stored by row. For example, the first 16 memory locations would contain the first row of pixel values. The 17th memory location would contain the first pixel of the second row.

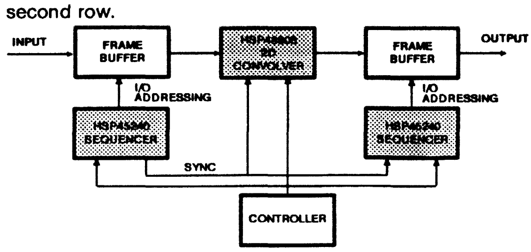


FIGURE 3. IMAGE PROCESSING SYSTEM

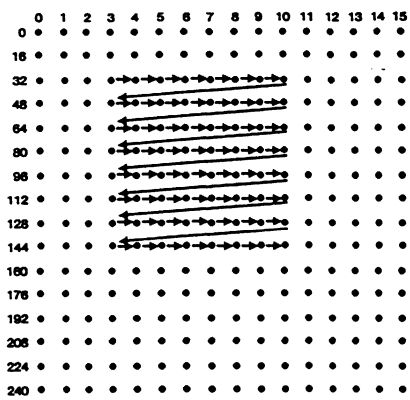


FIGURE 4. SEQUENCER SUB-IMAGE ADDRESSING

The sub-image address sequence shown in Figure 3 is generated by configuring the sequence generator with the following:

1. Start Address = 35
2. Block Size = 8
3. Number of Blocks = 8
4. Step Size = 1
5. Block Step Size = 16

In this example the start address corresponds to the address of the first pixel of the first row. The row length corresponds to the Block Size which is programmed to 8. Within the block, consecutive addresses are generated by programming the Step Size to 1. At the completion of first block of addresses, the Block Step Size of 16 is added to the Start Address to generate the address of the first pixel of the second row. Finally, 8 rows of addressing are generated by setting the Number of Blocks to 8.

In this application, the sub-image is processed one time and then a new sub-image area is chosen. As a result, the Mode Control Register would be configured for One-Shot mode without Restart. Also, the Start Delay Control register of the Sequencer driving the output frame buffer would be configured with a start delay to compensate for the pipeline delay introduced by the 2-D Convolver. Finally, the crosspoint switch would be configured in 1:1 mode so that the sequence generator output has a 1 to 1 mapping to the chip output.

For applications requiring decimation of the original image, the Step Size could be increased to provide addressing which skips over pixels along a row. Similary, the Block Step Size could be increased such that pixel rows are skipped.

FFT Processing

The application shown in Figure 5 depicts the architecture of a simplified radix 2 FFT processor. In this application the Address Sequencer drives a memory bank which feeds the arithmetic processor with data. In a radix 2 implementation, the arithmetic processor takes two complex data inputs and produces two results. These results are then stored in the registers from which the data came. This type of implementation is referred to as an "in place" FFT algorithm.

The arithmetic processing unit performs an operation know as the radix 2 butterfly which is shown graphically in Figure 6. In this diagram the node in the center of the butterfly represents summing point while the arrow represents a multiplication point. The flow of an FFT computation is described by diagrams comprised of many butterflies as shown in Figure 7.

The FFT processing shown in Figure 7 consists of three stages of radix 2 butterfly computation. The read/write addressing, expressed in binary, for each stage is shown in Table 5. The specialized addressing required here is produced by using the crosspoint switch to map the address bits from the sequence generator to the chip output.

The mapping for the sequencer's crosspoint switch is determined, by inspecting the addressing for each stage. For example, the first stage of addressing is generated by configuring the crosspoint switch so that bit 0 of the switch input is mapped to bit 2 of the switch output, bit 1 of the switch input is mapped to bit 0 of the output, and bit 2 of the switch input is mapped to bit 1 of the switch output. The remainder of the switch I/O map is configured 1:1, i.e. bit 3 of the switch input is mapped to bit 3 of the switch output. Under this configuration, a sequence generator output of 0,1,2,3,4,5,6,7 will produce a crosspoint switch output of 0,4,1,5,2,6,3,7. The switch maps for the other stages as well as a map for the bit-reverse addressing of the FFT result is given in Table 5.

The serial count required as input for the crosspoint switch is generated by configuring the sequence generator with the following:

1. Start Address = 0
2. Block Size = 8
3. Number of Blocks = 1
4. Step Size = 1
5. Block Step Size = 0

Under this configuration the sequence generator will produce a count from 0 to 7 in increments of 1. The FFT length corresponds to the Block Size, in this case 8.

The serial count from the sequence generator is converted into the desired addressing sequence by applying the appropriate map to the crosspoint switch. In this application, the switch mapping changes for each stage of the FFT computation. Thus, while one address sequence is being completed, the crosspoint switch is being configured for the next stage of FFT addressing. When one stage of addressing is complete, the new switch configuration is loaded into the current state registers by an internal or externally generated start or restart.

The crosspoint switch is configured for the first stage of addressing by writing a 0 to switch output register 2, a 2 to switch output register 1, and a 0 to switch output register 2. These values are loaded by first writing the address of switch output register 0 and then loading data using auto-address increment mode (see Table 1). The remaining registers are assumed to be configured in 1:1 mode as a result of a prior "RESET". The second and third stages of addressing are generated by reconfiguring the above three registers.

The Address Sequencer can be configured in dual sequencer mode to provide both read and write addressing for each butterfly. Since 2 independent 12 bit sequences can be generated by the Address Sequencer, it can be used to provide read/write addressing for FFT's up to 4096 points. The programmable delay between the MSW and LSW of the Sequencer output is used to compensate for the pipeline delay associated with the arithmetic processor.

TABLE 5. FFT ADDRESSING BY COMPUTATIONAL STAGE

STAGE 1 R/W ADDR.	STAGE 2 R/W ADDR.	STAGE 3 R/W ADDR.	OUTPUT ADDRESSING
000	000	000	000
100	010	001	100
001	001	010	010
101	011	011	110
010	100	100	001
110	110	101	101
011	101	110	011
111	111	111	111
SWITCH MAPPING			
021	201	210	012

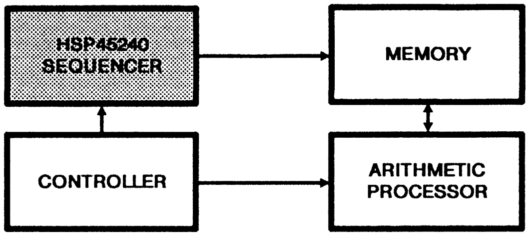


FIGURE 5. FFT PROCESSOR

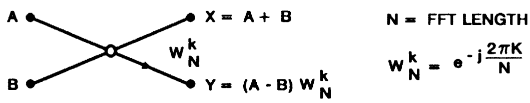


FIGURE 6. BUTTERFLY FOR DECIMATION-IN-FREQUENCY

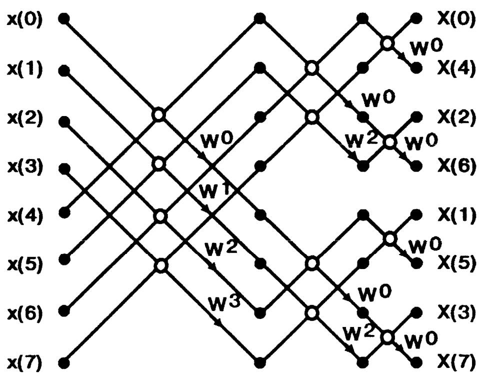


FIGURE 7. COMPLETE EIGHT-POINT IN-PLACE DECIMATION-IN-FREQUENCY FFT

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output or I/O Voltage Applied .... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation at +70°C .... 1.86W (PLCC), 2.84W (PGA)
θ_{jc} .... 15.1°C/W (PLCC), 10.1°C/W (PGA)
θ_{ja} .... 43.1°C/W (PLCC), 37.1°C/W (PGA)
Gate Count .... 8388 Gates
Junction Temperature .... +150°C (PLCC), +175°C (PGA)
Lead Temperature (Soldering, Ten Seconds) .... +300°C
ESD Classification .... Class 1

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +5.0V ± 5%
Operating Temperature Range .... 0°C to +70°C

D.C. Electrical Specifications (V_{CC} = 5.0V + 5%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.0	-	V	V_{CC} = 5.25V
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = 4.75V
High Level Clock Input	V_{IHC}	3.0	-	V	V_{CC} = 5.25V
Low Level Clock Input	V_{ILC}	-	0.8	V	V_{CC} = 4.75V
Output HIGH Voltage	V_{OH}	2.6	-	V	I_{OH} = -400μA, V_{CC} = 4.75V
Output LOW Voltage	V_{OL}	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.75V
Input Leakage Current	I_I	-10	10	μA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V
I/O Leakage Current	I_O	-10	10	μA	V_{OUT} = V_{CC} or GND, V_{CC} = 5.25V
Standby Power Supply Current	I_{CCSB}	-	500	μA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Outputs open
Operating Power Supply Current	I_{CCOP}	-	99	mA	f = 33MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Outputs Open, (Note 1)
Input Capacitance	C_{IN}	-	10	pF	f = 1MHz, V_{CC} = Open, all measurements are referenced to device GND. (Note 2).
Output Capacitance	C_O	-	10	pF	

NOTES:

1. Power supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 3mA/MHz.
2. Not tested, but characterized at initial design and at major process/design changes.

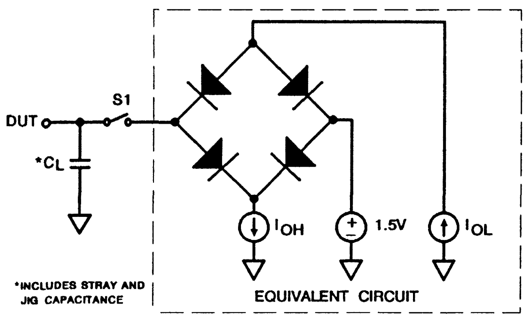
A.C. Electrical Specifications (V_{CC} = 5.0V + 5%, T_A = 0°C to +70°C) (Note 2)

PARAMETER	SYMBOL	-33 (33MHz) MIN	-33 (33MHz) MAX	-40 (40MHz) MIN	-40 (40MHz) MAX	-50 (50MHz) MIN	-50 (50MHz) MAX	UNIT	TEST CONDITIONS
Clock Period	T_{CP}	30	-	25	-	20	-	ns	
Clock Pulse Width High	T_{CH}	12	-	10	-	9	-	ns	
Clock Pulse Width Low	T_{CL}	12	-	10	-	9	-	ns	
Setup Time D0-6 to WR# High	T_{DS}	14	-	13	-	12	-	ns	
Hold Time D0-6 from WR# High	T_{DH}	0	-	0	-	0	-	ns	
Set-up Time A0, CS#, to WR# Low	T_{AS}	5	-	5	-	5	-	ns	
Hold Time A0, CS#, from WR# High	T_{AH}	0	-	0	-	0	-	ns	
Pulse Width for WR# Low	T_{WRL}	13	-	12	-	10	-	ns	
Pulse Width for WR# High	T_{WRH}	13	-	12	-	10	-	ns	
WR# Cycle Time	T_{WP}	30	-	25	-	20	-	ns	
Set-up Time STARTIN#, DLYBLK, to Clock High	T_{IS}	12	-	10	-	8	-	ns	
Hold Time STARTIN#, DLYBLK, to Clock High	T_{IH}	0	-	0	-	0	-	ns	
Clock to Output Prop. Delay on OUT0-23	T_{PDO}	-	15	-	13	-	12	ns	
Clock to Output Prop. Delay on STARTOUT#, BLKDONE#, DONE#, ADDVAL#, and BUSY#	T_{PDS}	-	15	-	13	-	12	ns	
Output Enable Time	T_{EN}	-	20	-	15	-	13	ns	
Output Disable Time	T_{OD}	-	20	-	15	-	13	ns	Note 1
Output Rise/Fall Time	T_{ORF}	-	5	-	3	-	3	ns	Note 1
RST# Low Time	T_{RST}	2 Clock Cycles						ns	

NOTES:

1. Controlled by design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
2. A.C. Testing is performed as follows: Input levels (CLK Input) = 4.0V and 0V; Input levels (All other inputs) = 0V and 3.0V; Input timing reference levels: (CLK) = 2.0V, (Others) = 1.5V; Output timing references: $V_{OH} \geq 1.5V$, $V_{OL} \leq 1.5V$.

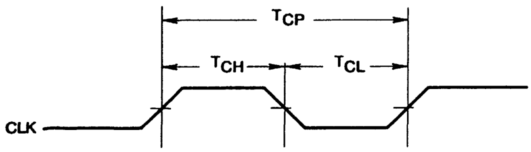
A.C. Test Load Circuit



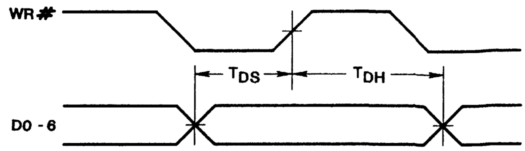
OUTPUT PIN	C_L
BLOCKDONE# DONE# ADDVAL# STARTOUT# BUSY#	40pF
OUT0-23	100pF

*Test Head Capacitance
Switch S1 Open for I_{CCSB} and I_{CCOP} Tests.

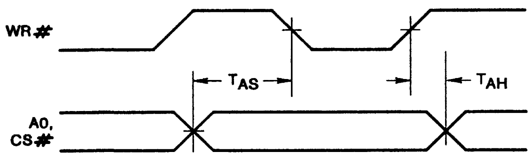
Timing Diagrams



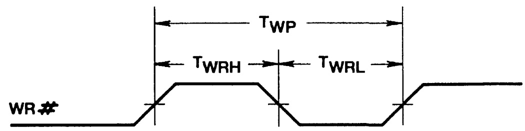
CLOCK AC PARAMETERS



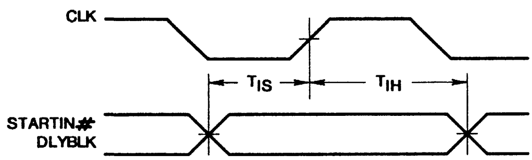
DATA SETUP AND HOLD



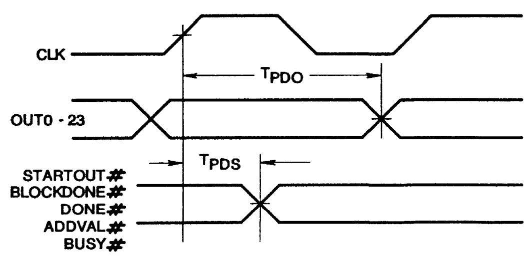
ADDRESS/CHIP SELECT SETUP AND HOLD



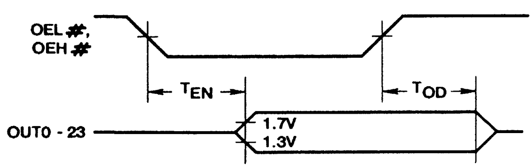
WR# AC PARAMETERS



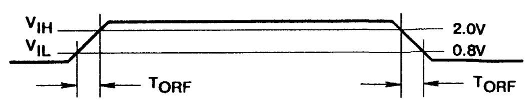
INPUT SETUP AND HOLD



OUTPUT PROPOGATION DELAY



OUTPUT ENABLE, DISABLE TIMING



OUTPUT RISE AND FALL TIMING

HSP45240/883

February 1994

Address Sequencer

Features

- **This Circuit Is Processed In Accordance to MIL-STD-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Block Oriented 24-Bit Sequencer**
- **Configurable as Two Independent 12-Bit Sequencers**
- **24 x 24 Crosspoint Switch**
- **Programmable Delay on 12 Outputs**
- **Multi-Chip Synchronization Signals**
- **Standard μP Interface**
- **100pF Drive on Outputs**
- **DC to 40MHz Clock Rate**

Applications

- **1-D, 2-D Filtering**
- **Pan/Zoom Addressing**
- **FFT Processing**
- **Matrix Math Operations**

Description

The Harris HSP45240 is a high speed Address Sequencer which provides specialized addressing for functions like FFTs, 1-D and 2-D filtering, matrix operations, and image manipulation. The sequencer supports block oriented addressing of large data sets up to 24 bits at clock speeds up to 40MHz.

Specialized addressing requirements are met by using the onboard 24 x 24 crosspoint switch. This feature allows the mapping of the 24 address bits at the output of the address generator to the 24 address outputs of the chip. As a result, bit reverse addressing, such as that used in FFTs, is made possible.

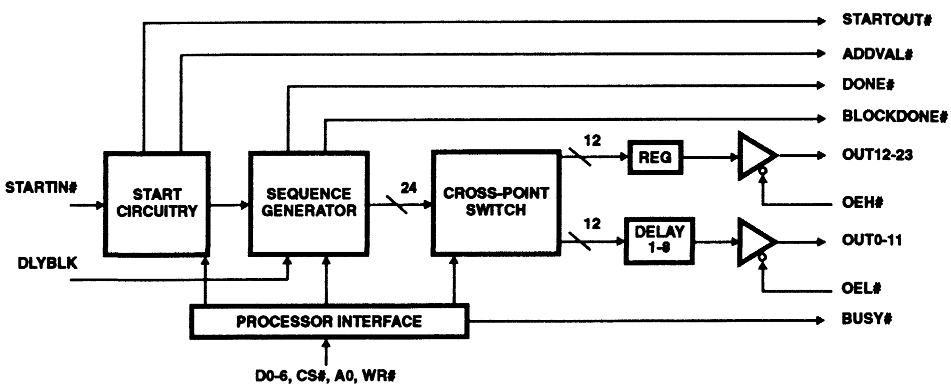
A single chip solution to read/write addressing is also made possible by configuring the HSP45240 as two 12-bit sequencers. To compensate for system pipeline delay, a programmable delay is provided on 12 of the address outputs.

The HSP45240 is manufactured using an advanced CMOS process, and is a low power fully static design. The configuration of the device is controlled through a standard microprocessor interface and all inputs/outputs, with the exception of clock, are TTL compatible.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP45240GM-25/883	-55°C to +125°C	68 Lead PGA
HSP45240GM-33/883	-55°C to +125°C	68 Lead PGA
HSP45240GM-40/883	-55°C to +125°C	68 Lead PGA

Block Diagram



File Number **2816.2**

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output Voltage Applied .... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering, Ten Seconds) .... +300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic PGA Package	37.1°C/W	10.1°C/W

Maximum Package Power Dissipation at +125°C
Ceramic PGA Package .... 1.35 Watt
Gate Count .... 8,388 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range .... -55°C to +125°C

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400μA V_{CC} = 4.5V (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC} = 4.5V (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-10	+10	μA
Output Leakage Current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-10	+10	μA
Clock Input High	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.8	V
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V, Outputs Open	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	500	μA
Operating Power Supply Current	I_{CCOP}	f = 33MHz V_{CC} = 5.5V (Note 2)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	99	mA
Functional Test	FT	(Note 3)	7, 8	$-55°C \leq T_A \leq +125°C$	-	-	

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 3mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, $V_{OH} \geq$ 1.5V, $V_{OL} \leq$ 1.5V, V_{IHC} = 3.4V, and V_{ILC} = 0.4V.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested (Note 1)

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS -25 (25MHz) MIN	MAX	-33 (33MHz) MIN	MAX	-40 (40MHz) MIN	MAX	UNITS
Clock Period	T_{CP}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	39	-	30	-	25	-	ns
Clock Pulse Width High	T_{CH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	12	-	10	-	ns
Clock Pulse Width Low	T_{CL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	12	-	10	-	ns
Setup Time D0-6 to WR# High	T_{DS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	17	-	16	-	14	-	ns
Hold Time D0-6 from WR# Low	T_{DH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Set-up Time A, CS#, to WR# Low	T_{AS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	5	-	5	-	5	-	ns
Hold Time A ,CS#, from WR# High	T_{AH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Pulse Width for WR# Low	T_{WRL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	18	-	14	-	12	-	ns
Pulse Width for WR# High	T_{WRH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	18	-	14	-	12	-	ns
WR# Cycle Time	T_{WP}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	39	-	30	-	25	-	ns
Set-up Time STARTIN#, DLYBLK, to to Clock High	T_{IS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	12	-	10	-	ns
Hold Time STARTIN#, DLYBLK, to Clock High	T_{IH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Clock to Output Prop. Delay on OUT0-23	T_{PDO}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	18	-	16	-	14	ns
Clock to Prop. Delay, on STARTOUT#, BLKDONE#, DONE#, ADVAL#, and BUSY#	T_{PDS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	18	-	16	-	14	ns
Output Enable Time	T_{EN}	Note 2	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	22	-	20	-	15	ns
RST# Low Time	T_{RST}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	2 Clock Cycles						ns

NOTES:

1. A.C. Testing: V_{CC} = 4.5V and 5.5V, Inputs are driven at 3.0V for Logic "1" and 0.0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a logic "1" and "0". CLK is driven at 4.0V and 0V and measured at 2.0V.
2. Transition is measured at ±200mV from steady state voltage with loading as specified by test load circuit and C_L = 40pF.

7 SPECIAL FUNCTION

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS -25 (25MHz) MIN	-25 (25MHz) MAX	-33 (33MHz) MIN	-33 (33MHz) MAX	-40 (40MHz) MIN	-40 (40MHz) MAX	UNITS
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	10	-	10	-	10	pF
Output Capacitance	C_{OUT}	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	10	-	10	-	10	pF
Output Disable Delay	T_{OEZ}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	22	-	20	-	15	ns
Output Rise Time	T_{OR}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	5	-	5	-	3	ns
Output Fall Time	T_{OF}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	5	-	5	-	3	ns

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Burn-In Circuit

	1	2	3	4	5	6	7	8	9	10	11
L		OEH#	DLYBLK	START OUT #	V_{CC}	BLOCK DONE#	GND	OUT1	OUT2	NC	
K	NC	NC	OEL#	START IN#	ADD VAL#	BUSY#	DONE#	OUT0	V_{CC}	NC	OUT3
J	RST#	V_{CC}								GND	OUT4
H	CLK	GND								OUT5	V_{CC}
G	CS#	AO								OUT6	OUT7
F	WR#	GND								GND	OUT8
E	D6	D5								OUT9	V_{CC}
D	D4	D3								OUT10	OUT11
C	D2	D1								GND	OUT12
B	D0	NC	OUT22	OUT21	GND	OUT18	OUT17	GND	OUT14	NC	NC
A		GND	OUT23	V_{CC}	OUT20	OUT19	V_{CC}	OUT16	OUT15	OUT13	

68 LEAD
PIN GRID ARRAY
BOTTON VIEW

PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
A2	GND	GND	B9	OUT14	$V_{CC}/2$	F11	OUT8	$V_{CC}/2$	K6	BUSYB	$V_{CC}/2$
A3	OUT23	$V_{CC}/2$	C1	D2	F10	G1	CSB	F5	K7	DONEB	$V_{CC}/2$
A4	V_{CC}	V_{CC}	C2	D1	F9	G2	A0	F6	K8	OUT0	$V_{CC}/2$
A5	OUT20	$V_{CC}/2$	C10	GND	GND	G10	OUT6	$V_{CC}/2$	K9	V_{CC}	V_{CC}
A6	OUT19	$V_{CC}/2$	C11	OUT12	$V_{CC}/2$	G11	OUT7	$V_{CC}/2$	K11	OUT3	$V_{CC}/2$
A7	V_{CC}	V_{CC}	D1	D4	F12	H1	CLK	F0	L2	OEHB	F13
A8	OUT16	$V_{CC}/2$	D2	D3	F11	H2	GND	GND	L3	DLYBLK	F11
A9	OUT15	$V_{CC}/2$	D10	OUT10	$V_{CC}/2$	H10	OUT5	$V_{CC}/2$	L4	STARTOUTB	$V_{CC}/2$
A10	OUT13	$V_{CC}/2$	D11	OUT11	$V_{CC}/2$	H11	V_{CC}	V_{CC}	L5	V_{CC}	V_{CC}
B1	D0	F8	E1	D6	F7	J1	RSTB	F14	L6	BLOCKDONEB	$V_{CC}/2$
B3	OUT22	$V_{CC}/2$	E2	D5	F13	J2	V_{CC}	V_{CC}	L7	GND	GND
B4	OUT21	$V_{CC}/2$	E10	OUT9	$V_{CC}/2$	J10	GND	GND	L8	OUT1	$V_{CC}/2$
B5	GND	GND	E11	V_{CC}	V_{CC}	J11	OUT4	$V_{CC}/2$	L9	OUT2	$V_{CC}/2$
B6	OUT18	$V_{CC}/2$	F1	WRB	F4	K3	OELB	F12			
B7	OUT17	$V_{CC}/2$	F2	GND	GND	K4	STARTINB	F6			
B8	GND	GND	F10	GND	GND	K5	ADVALB	$V_{CC}/2$			

NOTES:

1. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5 ±0.5V.
4. 0.1μF (min) capacitor between V_{CC} and GND per position.
5. F0 = 100KHz ±10%, F1 = F0/2, F2 = F1/2 . . . . . , F11 = F10/2, 40% - 60% Duty Cycle.
6. Input voltage limits: V_{IL} = 0.8V max., V_{IH} = 4.5V ±10%.

Metallization Topology

DIE DIMENSIONS:

186 x 222 x 19 ±1 mils

METALLIZATION:

Type: Si - Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:

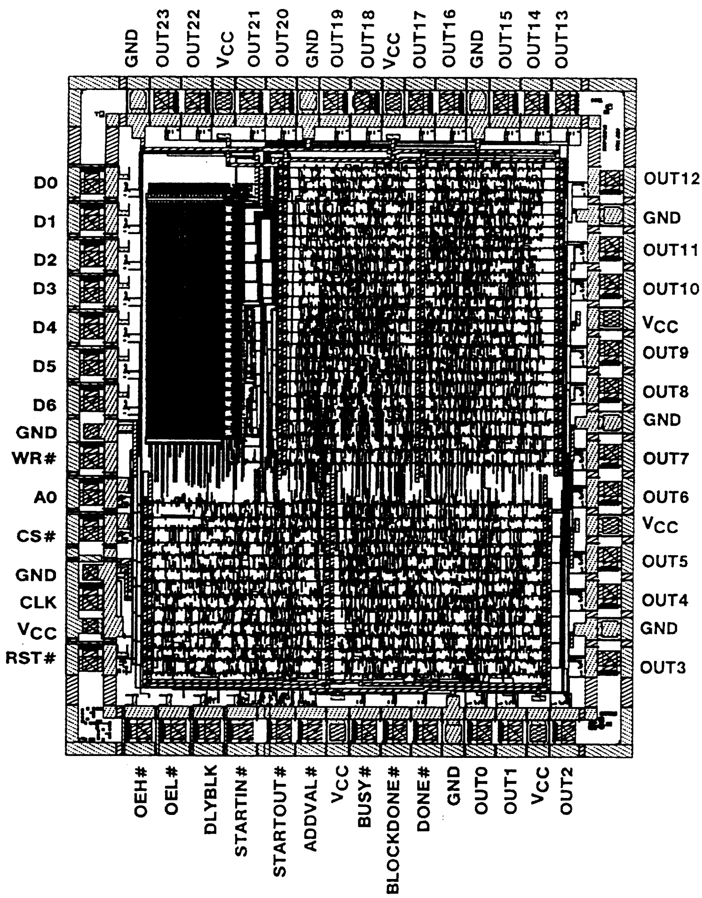
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:

$1.8 \times 10^5 A/cm^2$

Metallization Mask Layout

HSP45240/883



HARRIS SEMICONDUCTOR

HSP45256

January 1994

Binary Correlator

Features

- Reconfigurable 256 Stage Binary Correlator
- 1-Bit Reference x 1, 2, 4, or 8-Bit Data
- Separate Control and Reference Interfaces
- 25.6, 33MHz Versions
- Configurable for 1-D and 2-D Operation
- Double Buffered Mask and Reference
- Programmable Output Delay
- Cascadable
- Standard Microprocessor Interface

Applications

- Radar/Sonar
- Spread Spectrum Communications
- Pattern/Character Recognition
- Error Correction Coding

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP45256JC-25	0°C to +70°C	84 Lead PLCC
HSP45256JC-33	0°C to +70°C	84 Lead PLCC
HSP45256GC-25	0°C to +70°C	85 Lead PGA
HSP45256GC-33	0°C to +70°C	85 Lead PGA

Description

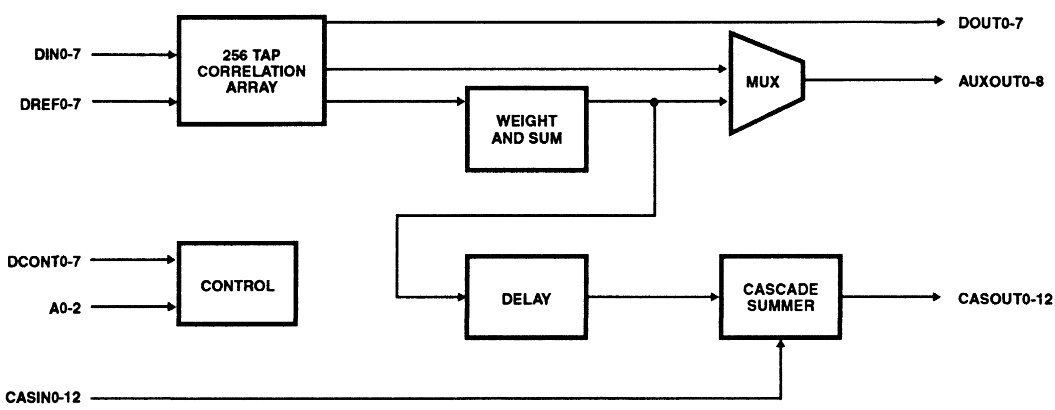
The Harris HSP45256 is a high-speed, 256 tap binary correlator. It can be configured to perform one- or two-dimensional correlations of selectable data precision and length. Multiple HSP45256's can be cascaded for increased correlation length. Unused taps can be masked out for reduced correlation length.

The correlation array consists of eight 32-tap stages. These may be cascaded internally to compare 1, 2, 4 or 8-bit input data with a 1-bit reference. Depending on the number of bits in the input data, the length of the correlation can be up to 256, 128, 64, or 32 taps. The HSP45256 can also be configured as two separate correlators with window sizes from 4 by 32 to 1 by 128 each. The mask register can be used to prevent any subset of the 256 bits from contributing to the correlation score.

The output of the correlation array (correlation score) feeds the weight and sum logic, which gives added flexibility to the data format. In addition, an offset register is provided so that a preprogrammed value can be added to the correlation score. This result is then passed through a user programmable delay stage to the cascade summer. The delay stage simplifies the cascading of multiple correlators by compensating for the latency of previous correlators.

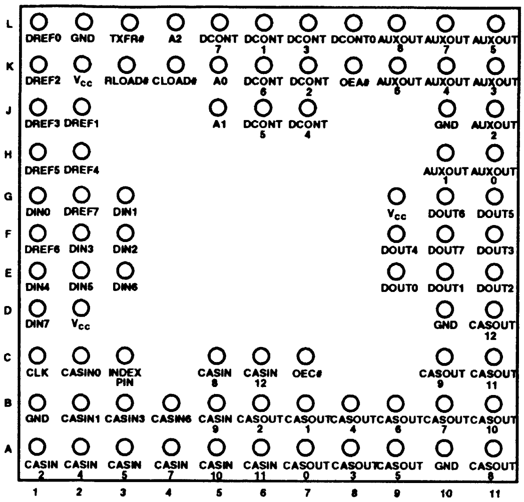
The Binary Correlator is configured by writing a set of control registers via a standard microprocessor interface. To simplify operation, both the control and reference registers are double buffered. This allows the user to load new mask and reference data while the current correlation is in progress.

Block Diagram

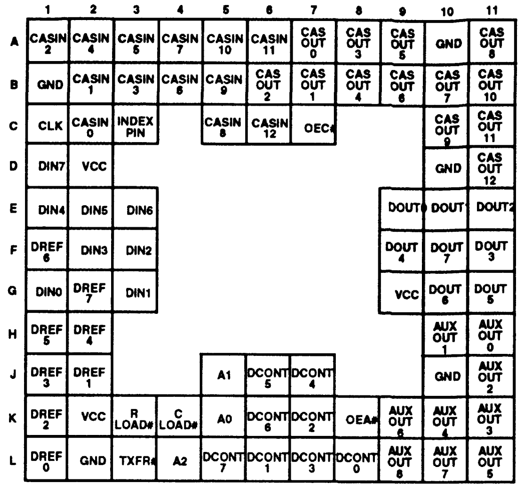


Pinouts

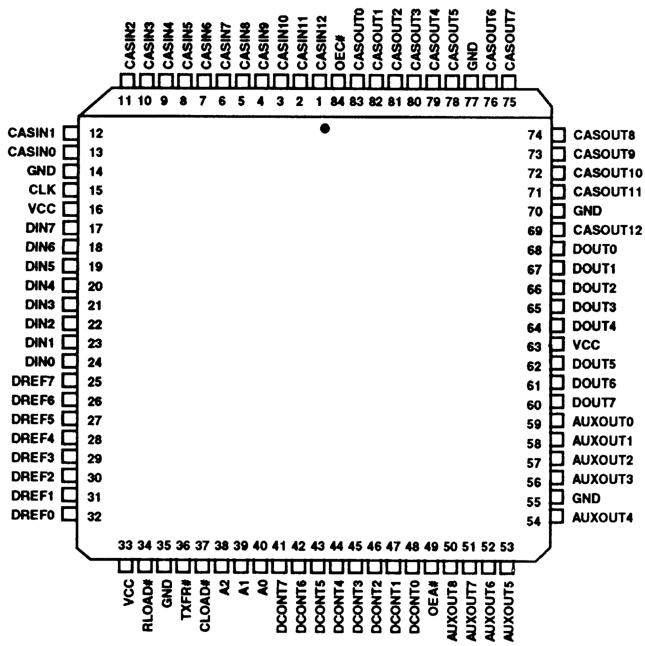
85 PIN PGA
BOTTOM VIEW



85 PIN PGA
TOP VIEW



84 PIN PLCC
TOP VIEW



Pin Description

SYMBOL	PLCC PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	16, 33, 63		The +5V power supply pin.
GND	14, 35, 55, 70, 77		Ground.
DIN0-7	17-24	I	The DIN0-7 bus consists of eight single data input pins. The assignment of the active pins is determined by the configuration. Data is loaded synchronous to the rising edge of CLK. DIN0 is the LSB.
DOUT0-7	60-62, 64-68	O	The DOUT0-7 bus is the data output of the correlation array. The format of the output is dependent on the window configuration and bit weighting. DOUT0 is the LSB.
CLK	15	I	System clock. Positive edge triggered.
CASIN0-12	1-13	I	CASIN0-12 allows multiple correlators to be cascaded by connecting CASOUT0-12 of one correlator to CASIN0-12 of another. The CASIN bus is added internally to the correlation score to form CASOUT. CASIN0 is the LSB.
CASOUT0-12	69, 71-76, 78-83	O	CASOUT0-12 is the output correlation score. This value is the delayed sum of all the 256 taps of one chip and CASIN0-12. When the part is configured to act as two independent correlators, CASOUT0-8 represents the correlation score for the first correlator while the second correlation score is available on the AUXOUT0-8 bus. In this configuration, the cascading feature is no longer an option. CASOUT0 is the LSB.
OEC#	84	I	OEC# is the output enable for CASOUT0-12. When OEC# is high, the output is three-stated. Processing is not interrupted by this pin. (Active low.)
TXFR#	36	I	TXFR# is a synchronous clock enable signal that allows the loading of the reference and mask inputs from the preload register to the correlation array. Data is transferred on the rising edge of CLK while TXFR# is low. (Active low.)
DREF0-7	25-32	I	DREF0-7 is an 8-bit wide data reference input. This is the input data bus used to load the reference data. RLOAD# going active initiates the loading of the reference registers. This input bus is used to load the reference registers of the correlation array. The manner in which the reference data is loaded is determined by the window configuration. If the window configuration is 1 x 256, the reference bits are loaded one at a time over DREF7. When the HSP45256 is configured as an 8 x 32 array, the data is loaded into all stages in parallel. In this case, DREF7 is the reference data for the first stage and DREF0 is the reference data for the eighth stage. The contents of the reference data registers are not affected by changing the window configuration. DREF0 is the LSB.
RLOAD#	34	I	RLOAD# enables loading of the reference registers. Data on DREF0-7 is loaded into the preload registers on the rising edge of RLOAD#. This data is transferred into the correlation array by TXFR#. (Active low.)
DCONT0-7	41-48	I	DCONT0-7 is the control data input, which is used to load the mask bit for each tap as well as the configuration registers. The mask data is sequentially loaded into the eight stages in the same manner as the reference data. DCONT0 is the LSB.
CLOAD#	37	I	CLOAD# enables the loading of the data on DCONT0-7. The destination of this data is controlled by A0-2. (Active low.)
A0-2	38-40	I	A0-2 is a 3-bit address that determines what function will be performed when CLOAD# is active. This address bus is set up with respect to the rising edge of the load signal, CLOAD#. A0 is the LSB.
AUXOUT0-8	50-54, 56-59	O	AUXOUT0-8 is a 9-bit bus that provides either the data reference output or the 9-bit correlation score of the second correlator, depending on the configuration. When the user programs the chip to be two separate correlators, the score of the second correlator is output on this bus. When the user has programmed the chip to be one correlator, AUXOUT0-7 represents the reference data out, with the state of AUXOUT0-8 undefined. AUXOUT0 is the LSB.
OEA#	49	I	The OEA# signal is the output enable for the AUXOUT0-8 output. When OEA# is high, the output is disabled. Processing is not interrupted by this pin. (Active low.)

Functional Description

The correlation array consists of eight 32-bit stages. The first stage receives data directly from input pin DIN7. The other seven stages receive input data from either an external data pin, DIN0-6, or from the shift register output of the previous stage, as determined by the Configuration Register. When the part is configured as a single correlator the sum of correlation score, offset register and cascade input appears on CASOUT0-12. Delayed versions of the data and reference inputs appear on DOUT0-7 and AUXOUT0-7, respectively. The input and output multiplexers of the correlation array are controlled together; for example, in a 1 x 256 correlation, the input data is loaded into DIN7 and the output appears on DOUT7. The configuration of the data bits, the length of the correlation (and in the two- dimensional data, the number of rows), is commonly called the correlation window.

Correlator Array

The core of the HSP45256 is the correlation array, which consists of eight 32-tap stages. A single correlator cell consists of an XNOR gate for the individual bit comparison; i.e., if the data and reference bits are either both high or both low, the output of the correlator cell is high. In addition, two latches, one for the reference and one for the control data path are contained in this cell. These latches are loaded from the preload registers on the rising edge of CLK when TXFR# is low so that the reference and mask values are updated without interrupting data processing.

The mask function is implemented with an AND gate. When a mask bit is a logic low, the corresponding correlator cell output is low.

The function performed by one correlation cell is:

$(D_{i,n}$ XNOR $R_{i,n})$ AND $M_{i,n}$

where:

$D_{i,n}$ = Bit i of data register n

$R_{i,n}$ = Bit i of reference register n

$M_{i,n}$ = Bit i of mask register n

The reference and mask bits are loaded sequentially, N bits at a time, where N depends on the current configuration (See Table 3). New reference data is loaded on the rising edge of RLOAD# and new mask data is loaded on the rising edge of CLOAD#. The mask and reference bits are stored internally in shift registers, so that the mask and reference information that was loaded most recently will be used to process the newest data. When new information is loaded in, the previous contents of the mask and reference bits are shifted over by one sample, and the oldest information is lost. There are no registers in the multiplexer array (Figure 1), so the data on DOUT0-7 corresponds to the data in the last element of the correlation array. When monitoring DOUT0-7, AUXOUT0-8, and REFOUT0-7, only those bits listed in Table 3 are valid.

Weight and Sum Logic

The Weight and Sum Logic provides the bit weighting and final correlator score from the eight stages of the correlation array. For a 1 x 256 1-D configuration, the outputs of each of the stages are given a weight of 1 and then added together. In a 8 x 32 (8-bit data) configuration, the output of each stage will be shifted so that the output data represents an 8-bit word, with stage seven being the MSB.

The 13-bit offset register is loaded from the control data bus. Its output is added to the correlation score obtained from the correlator array. This sum then goes to the programmable delay register data input.

When the chip is configured as dual correlators, the user has the capability of loading two different offset values for the two correlators.

The Programmable Delay Register sets the number of pipeline stages between the output of the weight and sum logic and the input of the Cascade Summer. This delay register is used to align the output of multiple correlators in cascaded configurations (See Applications). The number of delays is programmable from 1 to 16, allowing for up to 16 correlators to be cascaded. When the HSP45256 is configured as dual correlators, the delay must be set to 0000, which specifies a delay of 1.

Cascade Summer

This is used for cascading several correlators together. This value on this bus represents the correlation score from the previous HSP45256 that will be summed with the current score to provide the final correlation score. When several correlators are cascaded, the CASOUT0-12 of each of the other correlators is connected to the CASIN0-12 of the next correlator in the chain. The CASIN0-12 of the first chip is tied low. The following function represents the correlation score seen on CASOUT0-12 of each correlator:

CASOUT(n) = (W7 x CO7)(n-Delay) + (W6 x CO6)(n-Delay) +
(W5 x CO5)(n-Delay) + (W4 x CO4)(n-Delay) +
(W3 x CO3)(n-Delay) + (W2 x CO2)(n-Delay) +
(W1 x CO1)(n-Delay) + (W0 x CO0)(n-Delay) +
Offset (n-Delay) + CASIN.

where:

CO0-CO7 are the correlation score outputs out of the correlation stages; W0-W7 is the weight given to each stage; n-Delay represents the delay on the weighted and summed correlation score through the Programmable Delay Register; Offset is the value programmed into the Offset register; CASIN is the cascade input.

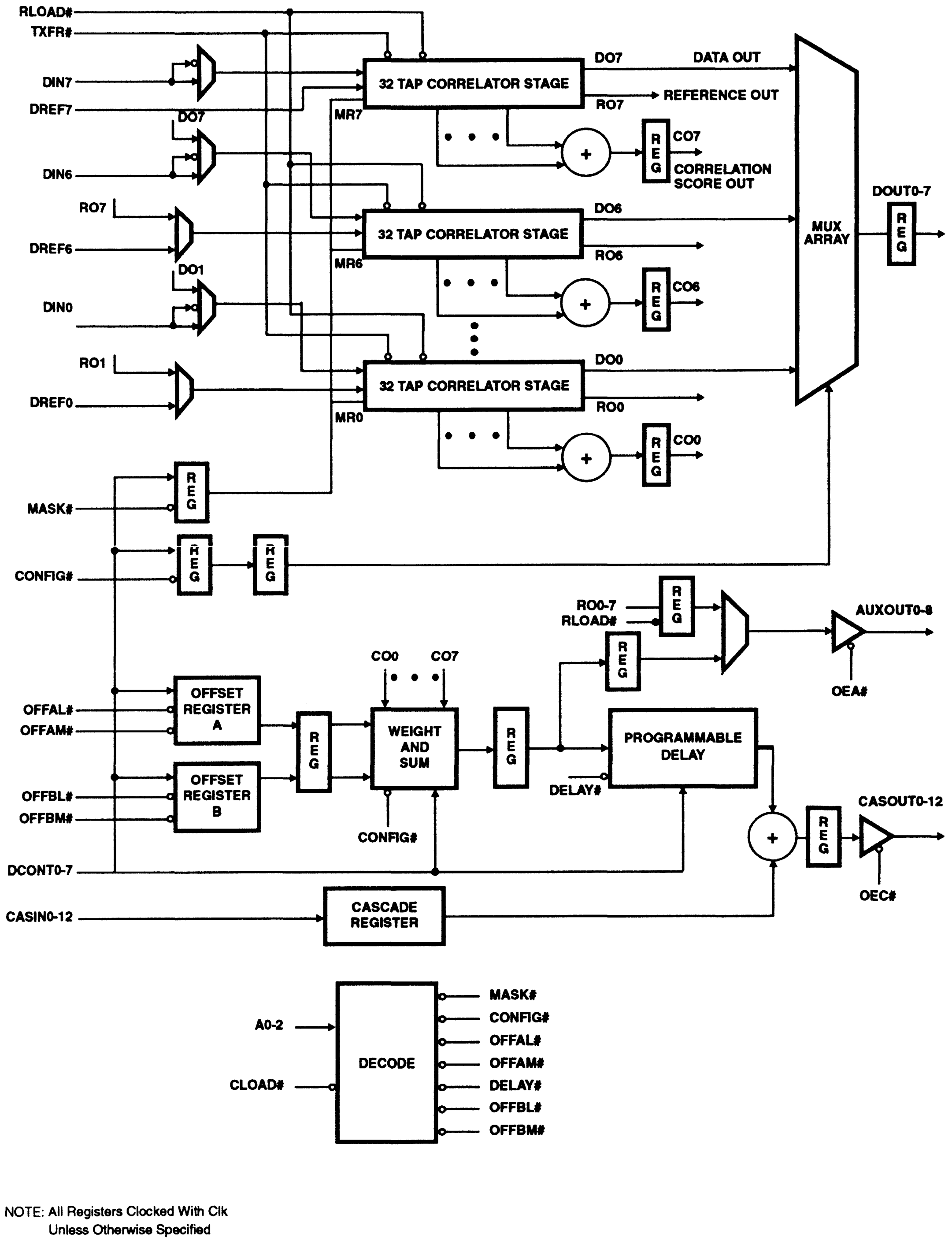


FIGURE 1. CORRELATOR BLOCK DIAGRAM

Control Registers

The 3-bit address value, A0-2, is used to determine which internal register will be loaded with the data on DCONT0-7. The function is initiated when CLOAD# is brought low, and the register is loaded on the rising edge of CLOAD#. Table 1 indicates the function associated with each address. Table 2 shows the function of the bits in each of the registers.

TABLE 1. ADDRESS MAPPING

A2	A1	A0	DESTINATION
0	0	0	Mask Register
0	0	1	Configuration Register
0	1	0	Offset Register A-Most Significant Bits
0	1	1	Offset Register A-Least Significant Bits
1	0	0	Programmable Delay Register
1	0	1	Offset Register B-Most Significant Bits
1	1	0	Offset Register B-Least Significant Bits
1	1	1	Reserved

TABLE 2. CONTROL REGISTER BITS

A0-2 = 000 Mask Register							
MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
MR0-7: Mask Register. When mask register bit N = 1, the corresponding reference register bit is enabled. Mask register data is loaded from the DCONT0-7 bus into a holding register on the rising edge of CLOAD# and is written to the mask register on the rising edge of TXFR#.							
A0-2 = 001 Configuration Register							
-	-	TC	CONFIG4	CONFIG3	CONFIG2	CONFIG1	CONFIG0
TC: Configures correlator for two's complement input. Inverts the MSB of the input data, where the position of the MSB depends on the current configuration. CONFIG4: The state of CONFIG4 sets up the HSP45256 as either one or two correlators. When CONFIG4 = 0, the HSP45256 is configured as one correlator with the correlation score available on CASOUT0-12. When CONFIG4 = 1, the HSP45256 is configured as dual correlators with the first correlator's score available on CASOUT0-8 and the second score available on AUXOUT0-8. When the chip is configured as dual correlators, the Programmable Delay must be set to 0000 for a delay of 1. CONFIG2-3: Control the number of data bits to be correlated. See Table 3. CONFIG0-1: CONFIG1 and CONFIG0 represent the length of the correlation window as indicated in Table 3.							
A0-2 = 010 MS Offset Register A							
-	-	-	OFFA12	OFFA11	OFFA10	OFFA9	OFFA8
OFFA8-12: Most significant bits of Offset Register A. This is the register used in single correlator mode.							
A0-2 = 011 LS Offset Register A							
OFFA7	OFFA6	OFFA5	OFFA4	OFFA3	OFFA2	OFFA1	OFFA0
OFFA0-7: Least significant bits of Offset Register A.							
A0-2 = 100 Programmable Delay							
-	-	-	-	PDELAY3	PDELAY2	PDELAY1	PDELAY0
PDELAY0-3: Controls amount of delay from the weight and sum logic to the cascade summer. The number of delays is 1-16, with PDELAY = 0000 corresponding to a delay of 1 and PDELAY = 1111 corresponding to a delay of 16.							
A0-2 = 101 MS Offset Register B							
-	-	-	-	-	-	-	OFFSETB8
OFFB8: Most significant bit of Offset Register B. In dual correlator mode, this register is used for the correlator whose output appears on the AUXOUT pins.							
A0-2 = 110 LS Offset Register B							
OFFB7	OFFB6	OFFB5	OFFB4	OFFB3	OFFB2	OFFB1	OFFB0
OFFB0-7: Least significant bits of Offset Register B.							

TABLE 3. CONFIGURATION SETUP

CONFIGURATION					NO. OF CORRE-LATORS	DATA BITS	ROWS	LENGTH	CORRE-LATOR	ACTIVE INPUTS		ACTIVE OUTPUTS			OUTPUT WEIGHTING							
4	3	2	1	0						DIN	DREF	DOUT	AUXOUT	CASOUT	CO7	CO6	CO5	CO4	CO3	CO2	CO1	CO0
0	0	0	0	0	1	1	1	256	-	7	7	7	7	12-0	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	2	128	-	7, 3	7, 3	7, 3	7, 3	12-0	1	1	1	1	1	1	1	1
0	0	0	1	0	1	1	4	64	-	7, 5, 3, 1	7, 5, 3, 1	7, 5, 3, 1	7, 5, 3 , 1	12-0	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	8	32	-	7-0	7-0	7-0	7-0	12-0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	2	1	128	-	7, 3	7	7, 3	7, 3	12-0	2	2	2	2	1	1	1	1
0	0	1	1	0	1	2	2	64	-	7, 5, 3, 1	7, 5	7, 5, 3, 1	7, 5, 3, 1	12-0	2	2	2	2	1	1	1	1
0	0	1	1	1	1	2	4	32	-	7-0	7, 6, 5, 4	7-0	7-0	12-0	2	2	2	2	1	1	1	1
0	1	0	1	0	1	4	1	64	-	7, 5, 3, 1	7	7, 5, 3, 1	7, 5, 3, 1	12-0	8	8	2	2	4	4	1	1
0	1	0	1	1	1	4	2	32	-	7-0	7, 6	7-0	7-0	12-0	8	8	2	2	4	4	1	1
0	1	1	1	1	1	8	1	32	-	7-0	7	7-0	7-0	12-0	128	8	32	4	64	2	16	1
1	0	0	0	1	2	1	1	128	A B	7 3	7 3	7 3	- 8-0	12-0 -	1 -	1 -	1 -	1 -	- 1	- 1	- 1	- 1
1	0	0	1	0	2	1	2	64	A B	7, 5 3, 1	7, 5 3, 1	7, 5 3, 1	- 8-0	12-0 -	1 -	1 -	1 -	1 -	- 1	- 1	- 1	- 1
1	0	0	1	1	2	1	4	32	A B	7-4 3-0	7-4 3-0	7-4 3-0	- 8-0	12-0 -	1 -	1 -	1 -	1 -	- 1	- 1	- 1	- 1
1	0	1	1	0	2	2	1	64	A B	7, 5 3, 1	7 3	7, 5 3, 1	- 8-0	12-0 -	2 -	2 -	1 -	1 -	- 2	- 2	- 1	- 1
1	0	1	1	1	2	2	2	32	A B	7-4 3-0	7, 6 3, 2	7-4 3-0	- 8-0	12-0 -	2 -	2 -	1 -	1 -	- 2	- 2	- 1	- 1
1	1	0	1	1	2	4	1	32	A B	7-4 3-0	7 3	7-4 3-0	- 8-0	12-0 -	8 -	2 -	4 -	1 -	- 8	- 2	- 4	- 1

During reference register loading, the 8-bits, DREF0-7 are used as reference data inputs. The falling edge of RLOAD# initiates reference data loading; when RLOAD# returns high, the data on DREF0-7 is latched into the selected correlation stages. The active bits on DREF0-7 are controlled by the current configuration.

The window configuration is determined by the state of control signals upon programming the control register. Table 3 represents the programming information required for each window configuration. In Table 3, note that the data listed for Output Weighting refers to the weights given to each of the Correlation Sum Outputs (CO0-7 in Figure 1).

During initialization, the loading configuration for the reference data is set by the user. Table 3 shows the loading options. These load controls specify whether the reference data for a given stage comes from the shift register output of the previous stage or from an external data pin.

Applications

Single HSP45256 – 1-Bit Data, 256 Samples

A 1 x 256 (1-D configuration) correlation requires only 1 HSP45256. To initialize the correlator, all the reference bits, control bits, the delay value of the variable delay, and the window configuration must be specified.

TABLE 4. REGISTER CONTENTS FOR 1 X 256 CORRELATOR WITH EQUAL WEIGHTING

A0-2	DCONT0-7	NOTES
001	00000000	1 256-tap correlator: 1 x 256 window configuration, reference loaded from DREF7, eight stages weighted equally, DIN 7 and DOUT7 are the data input and output, respectively.
010	00000000	Offset Register A = 0
011	00000000	
100	00000000	Programmable Delay = 0
101	00000000	Offset Register B = 0 (Loading of this register optional in this mode.)
110	00000000	

The loading of the reference and mask registers may be done simultaneously by setting A0-2 = 000, setting the DREF and DCONT inputs to their proper values and pulsing RLOAD# and CLOAD# low. In this configuration, DREF7 loads the reference data and DCONT7 loads the mask information; both sets of data are loaded serially. It will take 256 load pulses (RLOAD#) to load the reference array, and 256 CLOAD# pulses to load the mask array. Upon completion of the mask and register loading, TXFR# is pulsed low, which transfers the reference and control data from the preload registers to the reference and mask registers, updating the data that will be used in the correlation. Reference and mask data can be loaded more quickly by configuring the correlator as an 8 row by 32 sample array, loading the bits eight at a time, then changing the configuration back to 1 x 256 to perform the correlation.

Single HSP45256 – 8-Bit Data, 32 Samples

An 8 x 32 correlation also requires only 1 HSP45256. To initialize the correlator, all the reference bits, control bits, the value of the programmable delay, and the window configuration must be specified.

Again, the loading of the reference and mask registers can be done simultaneously. Due to the programming initialization, DREF0-7 are used to load the reference data 8-bits at a time. It will take 32 load pulses each of RLOAD# and CLOAD# to load both arrays. Upon completion of the mask and register loading, TXFR# is pulsed low, which transfers the reference and control data from the preload registers to the registers that store the active data.

TABLE 5. REGISTER LOADING FOR 8 X 32 CORRELATOR WITH BINARY WEIGHTING

A0-2	DCONT0-7	NOTES
001	00001111	1 256-tap correlator; 8 x 32 window configuration, 8-bit data stream; reference register is loaded from DREF7 for all stages. Correlator score = (128 x CO7) + (64 x CO3) + (32 x CO5) + (16 x CO1) + (8 x CO6) + (4 x CO4) + (2 x CO2) + CO0
010	00000000	Offset Register A = 0000000010000
011	00010000	
100	00000000	Programmable Delay = 0
101	00000000	Offset Register B = 0 (Loading optional in this mode.)
110	00000000	

This configuration performs correlation of an 8-bit number with a 1-bit reference. Each byte out of the correlation array gives an 8-bit level of confidence that the data corresponds to the reference. The correlation score is the sum of these confidence levels.

Single HSP45256 – Dual Correlators, 2-Bit Data, 64 Samples

Dual 2 x 64 correlators require only one HSP45256. To initialize the correlator, all the reference bits, control bits, the delay value of the variable delay, and the window configuration must be specified.

In this example, each of the dual correlators compares 2-bit data to a 1-bit reference. It will take 64 load pulses (RLOAD#/CLOAD#) to completely load the reference and mask registers in the array. The programmable delay must be set to 0 for the output of the two correlators to be aligned.

TABLE 6. REGISTER LOADING FOR DUAL 2 X 64 CORRELATORS WITH EQUAL WEIGHTING

AO-2	DCONT0-7	NOTES
001	00010010	Dual correlators: each 2 bit data, 64 taps; reference register for correlation A is loaded from DREF7 and DREF5, the reference register for correlator B is loaded from DREF3 and DREF1. Correlator #1 = 2x C07 + 2 x CO6 + CO5 + CO4, correlator #2 = 2 x CO3 + 2x CO2 + CO1 + CO0.
010	00000000	Offset Register A = 0000000010000
011	00010000	
100	00000000	Programmable Delay = 0
101	00000000	Offset Register B = 0
110	00000000	

Cascading Correlators

Correlators can be cascaded in either a serial or parallel fashion. Longer correlations can be achieved by connecting several correlators together as shown in Figure 2. Each correlator is in a one data bit, one row, 256 tap configuration. The number of bits of significance at the CASOUT output of each correlator builds up from one correlation to the next, that is, the maximum score out of the first correlator is 256, the maximum output of the second correlator is 512, etc. In this configuration, the maximum length of the correlation is 4096. This would be implemented with 16 HSP45256's. The programmable delay register in the first correlator would be set for one delay, the second would be set for two, and so on, with the final HSP45256 being set for a delay of 16.

Correlations of more bits can be calculated by connecting CASOUT of each chip to the CASIN of the following chip (Figure 3). The data on the CASOUT lines accumulates in a similar manner as in the 1 x 256 mode, except that the maximum output of the first correlator is decimal 960, (hexadecimal 3C0); in the general case, the maximum number of correlators that can be cascaded in this manner is eight, since the maximum output of the last one would be 1E00, which nearly uses up the 13-bit range of the cascade summer. More parts could be cascaded together if some bits are to be masked out or if the user has a prior knowledge of the maximum value of the correlation score. As before, the delay in the first correlator would be set to one, the second correlator would be set for a delay of two, and so on.

Multiple HSP45256's can be cascaded for two dimensional one bit data (Figure 4). The maximum output for each chip is the same as in the 1 x 256 case; the only difference is in the manner in which the correlators are connected. The programmable delay registers would be set as before.

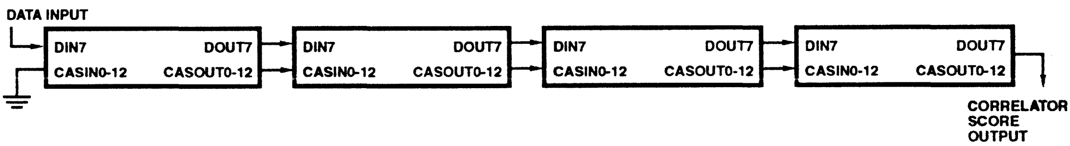


FIGURE 2. 1 BIT, 1024 SAMPLE CONFIGURATION

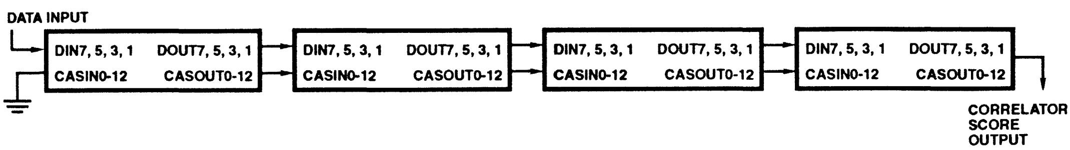


FIGURE 3. 4 BIT, 256 SAMPLE CONFIGURATION

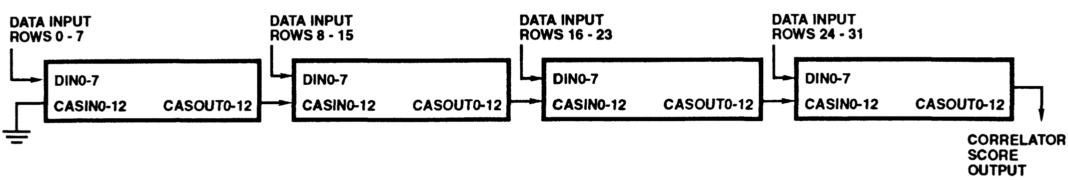


FIGURE 4. 1 BIT, 32 X 32 WINDOW CONFIGURATION

Reloading Data During Operation

RLOAD# and CLOAD# are asynchronous signals that are designed to be driven by the memory interface signals of a microprocessor. TXFR# is synchronized to CLK so that the mask or reference data is updated on a specific clock cycle. In the normal mode of operation, the user loads the reference and mask memories, then pulses TXFR# to use that data. The correlator uses the new mask or reference information immediately. Loading of the reference and mask data remains asynchronous as long as there is at least one cycle of CLK between the rising edge of RLOAD# or CLOAD# and the TXFR# pulse.

If the system timing makes it necessary for TXFR# and RLOAD# and/or CLOAD# to be active during the same clock cycle, then they must be treated as synchronous signals; the timing for this case is shown in Figure 5 and given in the AC Timing Specifications (T_{THCL} and T_{CLLH}). In this example, data is loaded during clock cycle 1 and transferred on the rising edge of CLK that occurs in clock cycle two. Another set of data is loaded during clock cycle 2, which will be transferred by a later TXFR# pulse. The sequence of events is as follows:

1. In clock cycle 1, TXFR# becomes active at least T_{TH} nanoseconds after the rising edge of CLK.
2. RLOAD and/or CLOAD# pulses low; the timing is not critical as long as its rising edge occurs before the end of clock cycle 1. If this condition is not met, it is undetermined whether the data loaded by this pulse will be transferred by the current TXFR# pulse.
3. The rising edge of TXFR# occurs while CLK is high during clock cycle 2. The margin between the rising edge of TXFR# and the falling edge of CLK is defined by T_{THCL}.
4. RLOAD# and/or CLOAD# pulses low. The rising edge of RLOAD# and CLOAD# must occur after the falling edge of CLK. The margin between the two is defined by T_{CLLH}.

The time from the rising edge of TXFR# to the falling edge of CLK must be greater than T_{THCL}, and the time from the falling edge of CLK to the rising edge of RLOAD# or CLOAD# must be greater than T_s. If this timing is violated, the data being transferred by the TXFR# pulse shown may or may not include the data loaded in clock cycle 2.

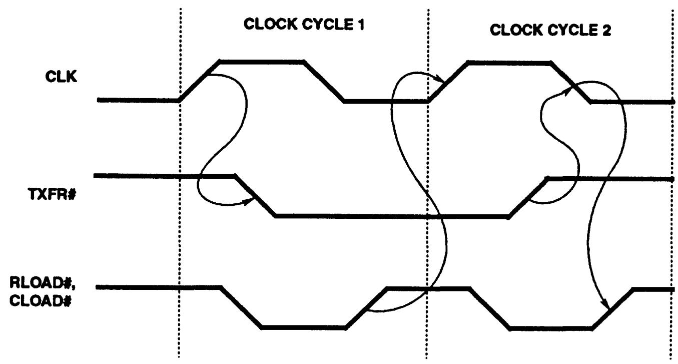


FIGURE 5. LOADING AND TRANSFERRING DATA DURING THE SAME CLOCK CYCLE

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output or I/O Voltage .... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature........... +150°C (PLCC), +175°C (PGA)
Lead Temperature (Soldering 10s).................... +300°C
ESD Classification .... Class 1

Thermal Resistance	θ_{JA}	θ_{JC}
PLCC Package	34°C/W	11.3°C/W
PGA Package	36°C/W	10°C/W

Maximum Package Power Dissipation at +125°C
PLCC Package 2.2W
PGA Package 2.9W
Gate Count .... 13,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range................... +4.75V to +5.25V
Operating Temperature Range .... 0°C to +70°C

DC Electrical Specifications

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.0	-	V	V_{CC} = 5.25V
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = 4.75V
High Level Clock Input	V_{IHC}	3.0	-	V	V_{CC} = 5.25V
Low Level Clock Input	V_{ILC}	-	0.8	V	V_{CC} = 4.75V
Output High Voltage	V_{OH}	2.6	-	V	I_{OH} = 400µA, V_{CC} = 4.75V
Output Low Voltage	V_{OL}	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.75V
Input Leakage Current	I_I	-10	10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V
Output Leakage Current	I_O	-10	10	µA	V_{OUT} = V_{CC} or GND, V_{CC} = 5.25V
Standby Power Supply Current	I_{CCSB}	-	500	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Note 3
Operating Power Supply Current	I_{CCOP}	-	179	mA	f = 25.6MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Note 1, Note 3

Capacitance (T_A = 25°C, Note 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_{IN}	-	10	pF	Frequency = 1MHz, V_{CC} = Open. All measurements are referenced to device ground.
Output Capacitance	C_O	-	10	pF	

NOTES:

1. Power supply current is proportional to operating frequency. Typical rating for ICCOP is 7mA/MHz.
2. Not tested, but characterized at initial design and at major process/design changes.
3. Output load per test load circuit and C_L = 40pF.

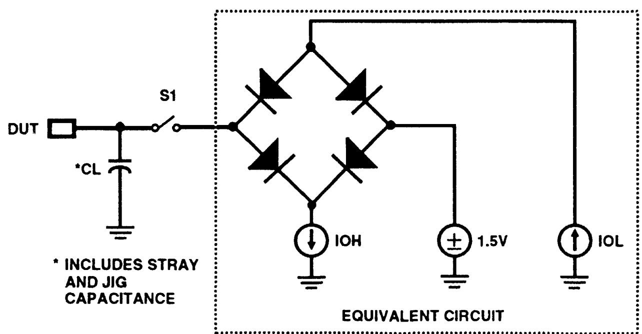
AC Electrical Specifications (V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C, Note 1)

PARAMETER	SYMBOL	33MHz MIN	33MHz MAX	25.6MHz MIN	25.6MHz MAX	UNITS	TEST CONDITIONS
CLK Period	T_{CP}	30	-	39	-	ns	
CLK High	T_{CH}	12	-	15	-	ns	
CLK Low	T_{CL}	12	-	15	-	ns	
Set-Up Time DIN to CLK High	T_{DS}	12	-	13	-	ns	
Hold Time CLK High to DIN	T_{DH}	0	-	0	-	ns	
TXFR# Set-Up Time	T_{TS}	12	-	13	-	ns	
TXFR# Hold Time	T_{TH}	0	-	0	-	ns	
Output Delay DOUT, AUXOUT, CASOUT	T_{DO}	-	15	-	20	ns	
CLOAD# Cycle Time	T_{CLC}	30	-	39	-	ns	
CLOAD# High	T_{CLH}	12	-	15	-	ns	
CLOAD# Low	T_{CLL}	12	-	15	-	ns	
Set-Up Time, A to RLOAD#, CLOAD#	T_{AS}	12	-	13	-	ns	
Hold Time, RLOAD#, CLOAD# to A	T_{AH}	0	-	0	-	ns	
RLOAD# Cycle Time	T_{RLC}	30	-	39	-	ns	
RLOAD# High	T_{RLH}	12	-	15	-	ns	
RLOAD# Low	T_{RLL}	12	-	15	-	ns	
Set-Up Time, DCONT to CLOAD#	T_{DCS}	12	-	13	-	ns	
Hold Time, CLOAD# to DCONT	T_{DCH}	0	-	0	-	ns	
Set-Up Time, DREF to RLOAD#	T_{RS}	12	-	13	-	ns	
Hold Time, RLOAD# to DREF	T_{RH}	0	-	0	-	ns	
Output Enable Time	T_{OE}	-	15	-	15	ns	
Output Disable Time	T_{OD}	-	15	-	15	ns	Note 2
Output Rise, Fall Time	T_{RF}	-	6		6	ns	Note 2
TXFR# High to CLK Low	T_{THCL}	3	-	3	-	ns	Note 2
CLK Low to RLOAD#, CLOAD# High	T_{CLLH}	1	-	1	-	ns	Note 2

NOTES:

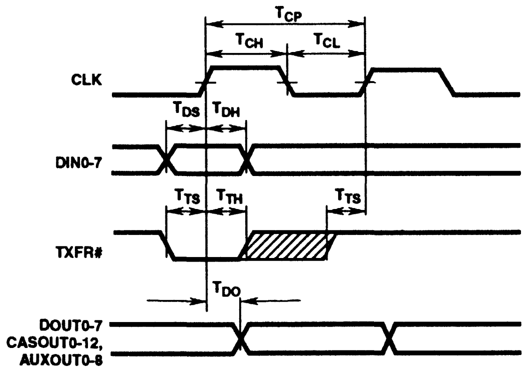
1. AC testing is performed as follows: Input levels (CLK Input) 4.0V and 0V; Input levels (all other inputs) 0V and 3.0V; Timing reference levels (CLK) 2.0V; All others 1.5V. Output load per test load circuit with C_L = 40pF. Output transition is measured at V_{OH} > 1.5V and V_{OL} < 1.5V.
2. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

Test Load Circuit

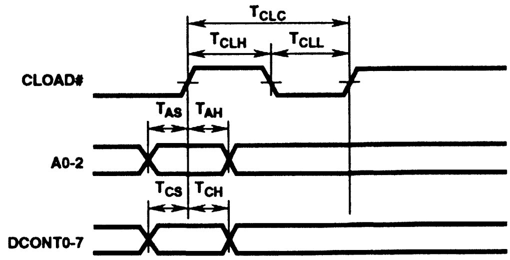


SWITCH S1 OPEN FOR I_{CCSB} AND I_{CCOP} TEST

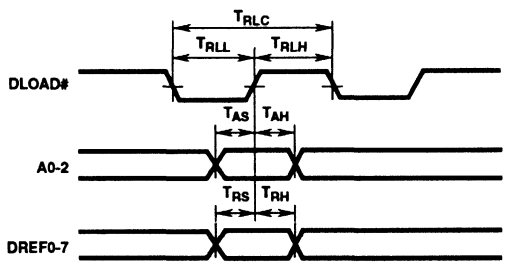
Timing Waveforms



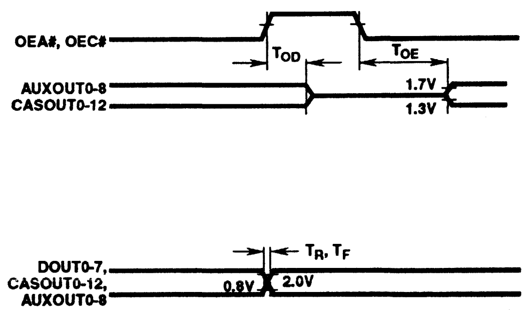
INPUT, OUTPUT TIMING



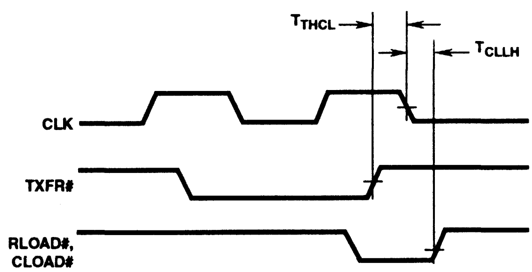
CONTROL INPUT TIMING



REFERENCE INPUT TIMING



OUTPUT TIMING



TRANSFER, LOAD TIMING WHEN BOTH OCCUR ON A SINGLE CYCLE

7

SPECIAL FUNCTION

HSP45256/883

January 1994

Binary Correlator

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Reconfigurable 256 Stage Binary Correlator**
- **1-Bit Reference x 1, 2, 4, or 8-Bit Data**
- **Separate Control and Reference Interfaces**
- **Configurable for 1-D and 2-D Operation**
- **Double Buffered Mask and Reference**
- **Programmable Output Delay**
- **Cascadable**
- **Standard Microprocessor Interface**

Applications

- **Radar/Sonar**
- **Spread Spectrum Communications**
- **Pattern/Character Recognition**
- **Error Correction Coding**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP45256GM-20/883	-55°C to +125°C	85 Lead PGA
HSP45256GM-25/883	-55°C to +125°C	85 Lead PGA

Description

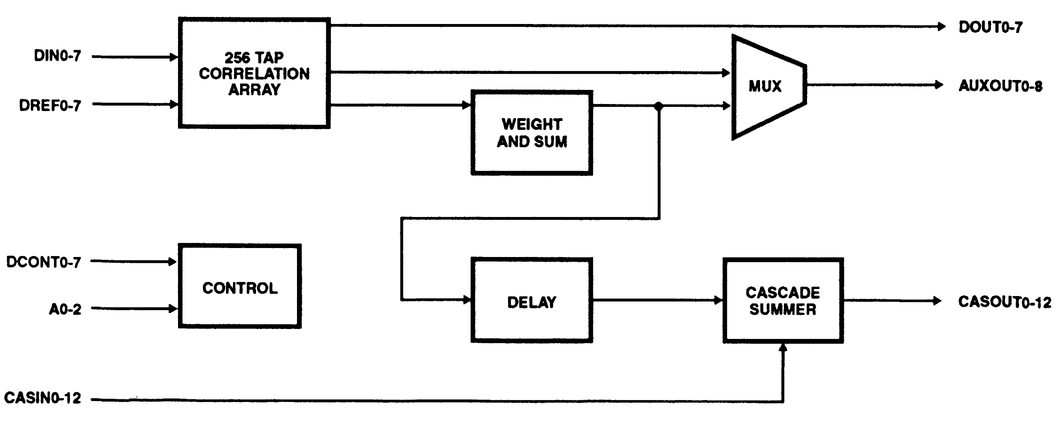
The Harris HSP45256 is a high-speed, 256 tap binary correlator. It can be configured to perform one- or two-dimensional correlations of selectable data precision and length. Multiple HSP45256's can be cascaded for increased correlation length. Unused taps can be masked out for reduced correlation length.

The correlation array consists of eight 32-tap stages. These may be cascaded internally to compare 1, 2, 4 or 8-bit input data with a 1-bit reference. Depending on the number of bits in the input data, the length of the correlation can be up to 256, 128, 64, or 32 taps. The HSP45256 can also be configured as two separate correlators with window sizes from 4 by 32 to 1 by 128 each. The mask register can be used to prevent any subset of the 256 bits from contributing to the correlation score.

The output of the correlation array (correlation score) feeds the weight and sum logic, which gives added flexibility to the data format. In addition, an offset register is provided so that a preprogrammed value can be added to the correlation score. This result is then passed through a user programmable delay stage to the cascade summer. The delay stage simplifies the cascading of multiple correlators by compensating for the latency of previous correlators.

The Binary Correlator is configured by writing a set of control registers via a standard microprocessor interface. To simplify operation, both the control and reference registers are double buffered. This allows the user to load new mask and reference data while the current correlation is in progress.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

Pinouts

85 PIN PGA
TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11
A	CASIN 2	CASIN 4	CASIN 5	CASIN 7	CASIN 10	CASIN 11	CAS OUT 0	CAS OUT 3	CAS OUT 5	GND	CAS OUT 8
B	GND	CASIN 1	CASIN 3	CASIN 6	CASIN 9	CAS OUT 2	CAS OUT 1	CAS OUT 4	CAS OUT 6	CAS OUT 7	CAS OUT 10
C	CLK	CASIN 0	INDEX PIN		CASIN 8	CASIN 12	OEC#			CAS OUT 9	CAS OUT 11
D	DIN7	VCC								GND	CAS OUT 12
E	DIN4	DIN5	DIN6						DOUT0	DOUT1	DOUT2
F	DREF 6	DIN3	DIN2						DOUT 4	DOUT 7	DOUT 3
G	DIN0	DREF 7	DIN1						VCC	DOUT 6	DOUT 5
H	DREF 5	DREF 4								AUX OUT 1	AUX OUT 0
J	DREF 3	DREF 1			A1	DCONT 5	DCONT 4			GND	AUX OUT 2
K	DREF 2	VCC	R LOAD#	C LOAD#	A0	DCONT 6	DCONT 2	OEA#	AUX OUT 6	AUX OUT 4	AUX OUT 3
L	DREF 0	GND	TXFR#	A2	DCONT 7	DCONT 1	DCONT 3	DCONT 0	AUX OUT 8	AUX OUT 7	AUX OUT 5

85 PIN PGA
BOTTOM VIEW

	1	2	3	4	5	6	7	8	9	10	11
L	DREF0	GND	TXFR#	A2	DCONT 7	DCONT 1	DCONT 3	DCONT0	AUXOUT 8	AUXOUT 7	AUXOUT 5
K	DREF2	V_{CC}	RLOAD#	CLOAD#	A0	DCONT 6	DCONT 2	OEA#	AUXOUT 6	AUXOUT 4	AUXOUT 3
J	DREF3	DREF1			A1	DCONT 5	DCONT 4			GND	AUXOUT 2
H	DREF5	DREF4								AUXOUT 1	AUXOUT 0
G	DIN0	DREF7	DIN1						V_{CC}	DOUT6	DOUT5
F	DREF6	DIN3	DIN2						DOUT4	DOUT7	DOUT3
E	DIN4	DIN5	DIN6						DOUT0	DOUT1	DOUT2
D	DIN7	V_{CC}								GND	CASOUT 12
C	CLK	CASIN0	INDEX PIN		CASIN 8	CASIN 12	OEC#			CASOUT 9	CASOUT 11
B	GND	CASIN1	CASIN3	CASIN6	CASIN 9	CASOUT 2	CASOUT 1	CASOUT 4	CASOUT 6	CASOUT 7	CASOUT 10
A	CASIN 2	CASIN 4	CASIN 5	CASIN 7	CASIN 10	CASIN 11	CASOUT 0	CASOUT 3	CASOUT 5	GND	CASOUT 8

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	D2, G9, K2		The +5V power supply pin
GND	A10, B1, D10, J10, L2		Ground.
DIN0-7	D1, E1-E3, F2, F3, G1, G3	I	The DIN0-7 bus consists of eight single data input pins. The assignment of the active pins is determined by the configuration. Data is loaded synchronous to the rising edge of CLK. DIN0 is the LSB.
DOUT0-7	E9-E11, F9-F11, G10, G11	O	The DOUT0-7 bus is the data output of the correlation array. The format of the output is dependent on the window configuration and bit weighting. DOUT0 is the LSB.
CLK	C1	I	System clock. Positive edge triggered.
CASIN0-12	A1-A6, B2-B5, C2, C5, C6	I	CASIN0-12 allows multiple correlators to be cascaded by connecting CASOUT0-12 of one correlator to CASIN0-12 of another. The CASIN bus is added internally to the correlation score to form CASOUT. CASIN0 is the LSB.
CASOUT0-12	A7-A9, A11, B6-B11, C10, C11, D11	O	CASOUT0-12 is the output correlation score. This value is the delayed sum of all the 256 taps of one chip and CASIN0-12. When the part is configured to act as two independent correlators, CASOUT0-8 represents the correlation score for the first correlator while the second correlation score is available on the AUXOUT0-8 bus. In this configuration, the cascading feature is no longer an option. CASOUT0 is the LSB.
OEC#	C7	I	OEC# is the output enable for CASOUT0-12. When OEC# is high, the output is three-stated. Processing is not interrupted by this pin. (Active low.)
TXFR#	L3	I	TXFR# is a synchronous clock enable signal that allows the loading of the reference and mask inputs from the preload register to the correlation array. Data is transferred on the rising edge of CLK while TXFR# is low. (Active low.)
DREF0-7	F1, G2, H1, H2, J1, J2, K1, L1	I	DREF0-7 is an 8-bit wide data reference input. This is the input data bus used to load the reference data. RLOAD# going active initiates the loading of the reference registers. This input bus is used to load the reference registers of the correlation array. The manner in which the reference data is loaded is determined by the window configuration. If the window configuration is 1 x 256, the reference bits are loaded one at a time over DREF7. When the HSP45256 is configured as an 8 x 32 array, the data is loaded into all stages in parallel. In this case, DREF7 is the reference data for the first stage and DREF0 is the reference data for the eighth stage. The contents of the reference data registers are not affected by changing the window configuration. DREF0 is the LSB.
RLOAD#	K3	I	RLOAD# enables loading of the reference registers. Data on DREF0-7 is loaded into the preload registers on the rising edge of RLOAD#. This data is transferred into the correlation array by TXFR#. (Active low.)
DCONT0-7	J6, J7, K6, K7, L5-L8	I	DCONT0-7 is the control data input, which is used to load the mask bit for each tap as well as the configuration registers. The mask data is sequentially loaded into the eight stages in the same manner as the reference data. DCONT0 is the LSB.
CLOAD#	K4	I	CLOAD# enables the loading of the data on DCONT0-7. The destination of this data is controlled by A0-2. (Active low.)
A0-2	J5, K5, L4	I	A0-2 is a 3-bit address that determines what function will be performed when CLOAD# is active. This address bus is set up with respect to the rising edge of the load signal, CLOAD#. A0 is the LSB.
AUXOUT0-8	H10, H11, J11, K9-K11, L9-L11	O	AUXOUT0-8 is a 9-bit bus that provides either the data reference output or the 9-bit correlation score of the second correlator, depending on the configuration. When the user programs the chip to be two separate correlators, the score of the second correlator is output on this bus. When the user has programmed the chip to be one correlator, AUXOUT0-7 represents the reference data out, with the state of AUXOUT0-8 undefined. AUXOUT0 is the LSB.
OEA#	K8	I	The OEA# signal is the output enable for the AUXOUT0-8 output. When OEA# is high, the output is disabled. Processing is not interrupted by this pin. (Active low.)
Index Pin	C3		Used for orienting pin in socket or printed circecuit board. Must be left as a no connect in circuit.

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output or I/O Voltage .... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering 10s) .... +300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic PGA Package	36°C/W	10°C/W

Maximum Package Power Dissipation at +125°C
Ceramic PGA Package 1.39W
Gate Count .... 13,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range .... -55°C to +125°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1,2,3	$-55° \le T_A \le +125°C$	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1,2,3	$-55° \le T_A \le +125°C$	-	0.8	V
Logical One Input Voltage Clock	V_{IHC}	V_{CC} = 5.5V	1,2,3	$-55° \le T_A \le +125°C$	3.0	-	V
Logical Zero Input Voltage Clock	V_{ILC}	V_{CC} = 4.5V	1,2,3	$-55° \le T_A \le +125°C$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA V_{CC}= 4.5V (Note 1)	1,2,3	$-55° \le T_A \le +125°C$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC}= 4.5V (Note 1)	1,2,3	$-55° \le T_A \le +125°C$	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1,2,3	$-55° \le T_A \le +125°C$	-10	+10	µA
Output Leakage Current	I_O	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1,2,3	$-55° \le T_A \le +125°C$	-10	+10	µA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND V_{CC} = 5.5V, Outputs Open	1,2,3	$-55° \le T_A \le +125°C$	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 20 MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.5V (Note 2)	1,2,3	$-55° \le T_A \le +125°C$	-	140	mA
Functional Test	FT	(Note 3)	7,8	$-55° \le T_A \le +125°C$	-	-	-

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 7mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH}(clock inputs) = 3.4V, V_{IH} (all other inputs) = 2.6V, V_{IL} = 0.4V, $V_{OH} \ge 1.5V$, and $V_{OL} \le 1.5V$.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	-25 (25.6MHz)		-20 (20MHz)		UNITS
					MIN	MAX	MIN	MAX	
CLK Period	T_{CP}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	39	-	50	-	ns
CLK High	T_{CH}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	15	-	20	-	ns
CLK Low	T_{CL}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	15	-	20	-	ns
CLOAD# Cycle Time	T_{CLC}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	39	-	50	-	ns
CLOAD# High	T_{CLH}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	15	-	20	-	ns
CLOAD# Low	T_{CLL}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	15	-	20	-	ns
RLOAD# Cycle Time	T_{RLC}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	39	-	50	-	ns
RLOAD# High	T_{RLH}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	15	-	20	-	ns
RLOAD# Low	T_{RLL}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	15	-	20	-	ns
Set-up Time; DIN to CLK High	T_{DS}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	13	-	15	-	ns
Hold Time; DIN to CLK High	T_{DH}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	1	-	1	-	ns
Set-up Time; DREF to RLOAD High	T_{RS}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	14	-	15	-	ns
Hold Time; DREF to RLOAD High	T_{RH}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	1	-	1	-	ns
DCONT Set up Time	T_{DCS}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	13	-	15	-	ns
DCONT Hold Time	T_{DCH}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	1	-	1	-	ns
Address Set up Time	T_{AS}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	13	-	15	-	ns
Address Hold Time	T_{AH}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	1	-	1	-	ns
TXFR# Set up Time	T_{TS}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	13	-	15	-	ns
TXFR# Hold Time	T_{TH}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	1	-	1	-	ns
CLK to Output Delay DOUT, AUXOUT, CASOUT	T_{DO}		9, 10, 11	$-55^o \leq T_A \leq +125^oC$	-	20	-	25	ns
Output Enable Time	T_{OE}	Note 2	9, 10, 11	$-55^o \leq T_A \leq +125^oC$	-	20	-	20	ns
TXFR# High to CLK Low	T_{THCL}	Note 3	9, 10, 11	$-55^o \leq T_A \leq +125^oC$	3	-	4	-	ns
CLK Low to RLOAD#, CLOAD# High	T_{CLLH}	Note 3	9, 10, 11	$-55^o \leq T_A \leq +125^oC$	1	-	1	-	ns

NOTES:

1. AC testing is performed as follows: V_{CC} = 4.5V and 5.5V. Input levels (CLK Input) 4.0V and 0V; Input levels (all other inputs) 3.0V and 0V; Timing reference levels (CLK) 2.0V; All others 1.5V. Output load per test load circuit with C_L = 40pF. Output transistion is measured at $V_{OH} \geq$ 1.5V and $V_{OL} \leq$ 1.5V.
2. Transistion is measured at ±200mV from steady state voltage, Output loading per test load circuit, C_L = 40pF.
3. Applicable only when TXFR# and RLOAD# or CLOAD# are active on the same cycle of CLK.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

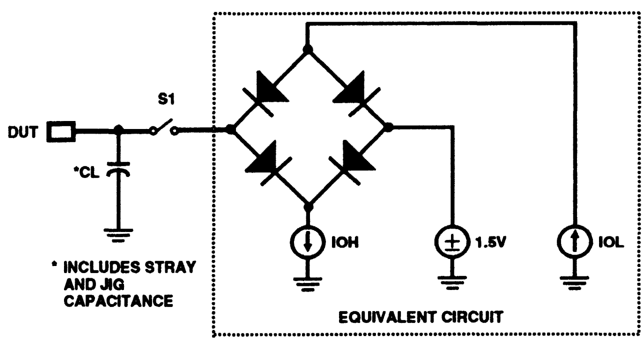
PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	-25 MIN	-25 MAX	-20 MIN	-20 MAX	UNITS
Input Capacitance	C_{IN}	VCC = Open, f=1 MHz All measurements are referenced to device GND.	1	$-55° \leq T_A \leq +125°C$	-	10	-	10	pF
Output Capacitance	C_{OUT}		1	$-55° \leq T_A \leq +125°C$	-	10	-	10	pF
Output Disable Time	T_{OD}		1, 2	$-55° \leq T_A \leq +125°C$	-	20	-	20	ns
Output Rise Time	T_R	From 0.8V to 2.0V	1, 2	$-55° \leq T_A \leq +125°C$	-	8	-	8	ns
Output Fall Time	T_F	From 2.0V to 0.8V	1, 2	$-55° \leq T_A \leq +125°C$	-	8	-	8	ns

NOTES:
1. The parameters in Table 3 are controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
2. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

Test Load Circuit



SWITCH S1 OPEN FOR I_{CCSB} AND I_{CCOP} TEST

Burn-In Circuits

	1	2	3	4	5	6	7	8	9	10	11
A	CASIN 2	CASIN 4	CASIN 5	CASIN 7	CASIN 10	CASIN 11	CAS OUT 0	CAS OUT 3	CAS OUT 5	GND	CAS OUT 8
B	GND	CASIN 1	CASIN 3	CASIN 6	CASIN 9	CAS OUT 2	CAS OUT 1	CAS OUT 4	CAS OUT 6	CAS OUT 7	CAS OUT 10
C	CLK	CASIN 0	INDEX PIN		CASIN 8	CASIN 12	OEC#			CAS OUT 9	CAS OUT 11
D	DIN7	V_{CC}								GND	CAS OUT 12
E	DIN4	DIN5	DIN6						DOUT0	DOUT1	DOUT2
F	DREF 4	DIN3	DIN2			85 PIN PGA TOP VIEW			DOUT 4	DOUT 7	DOUT 3
G	DIN0	DREF 7	DIN1						V_{CC}	DOUT 6	DOUT 5
H	DREF 5	DREF 4								AUX OUT 1	AUX OUT 0
J	DREF 3	DREF 1			A1	DCONT 5	DCONT 4			GND	AUX OUT 2
K	DREF 2	V_{CC}	R LOAD#	C LOAD#	A0	DCONT 6	DCONT 2	OEA#	AUX OUT 6	AUX OUT 4	AUX OUT 3
L	DREF 0	GND	TXFR#	A2	DCONT 7	DCONT 1	DCONT 3	DCONT 0	AUX OUT 8	AUX OUT 7	AUX OUT 5

PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	CASIN2	F3
A2	CASIN4	F5
A3	CASIN5	F6
A4	CASIN7	F1
A5	CASIN10	F4
A6	CASIN11	F5
A7	CASOUT0	$V_{CC}/2$
A8	CASOUT3	$V_{CC}/2$
A9	CASOUT5	$V_{CC}/2$
A10	GND	GND
A11	CASOUT8	$V_{CC}/2$
B1	GND	GND
B2	CASIN1	F2
B3	CASIN3	F4
B4	CASIN6	F7
B5	CASIN9	F3
B6	CASOUT2	$V_{CC}/2$
B7	CASOUT1	$V_{CC}/2$
B8	CASOUT4	$V_{CC}/2$
B9	CASOUT6	$V_{CC}/2$
B10	CASOUT7	$V_{CC}/2$
B11	CASOUT10	$V_{CC}/2$
C1	CLK	F0
C2	CASIN0	F1
C5	CASIN8	F2
C6	CASIN12	F6
C7	OEC#	F11
C10	CASOUT9	$V_{CC}/2$
C11	CASOUT11	$V_{CC}/2$
D1	DIN7	F8
D2	V_{CC}	V_{CC}
D10	GND	GND
D11	CASOUT12	$V_{CC}/2$
E1	DIN4	F5
E2	DIN5	F6
E3	DIN6	F7
E9	DOUT0	$V_{CC}/2$
E10	DOUT1	$V_{CC}/2$
E11	DOUT2	$V_{CC}/2$
F1	DREF6	F7
F2	DIN3	F4
F3	DIN2	F3
F9	DOUT4	$V_{CC}/2$
F10	DOUT7	$V_{CC}/2$
F11	DOUT3	$V_{CC}/2$
G1	DIN0	F1
G2	DREF7	F8
G3	DIN1	F2
G9	V_{CC}	V_{CC}
G10	DOUT6	$V_{CC}/2$
G11	DOUT5	$V_{CC}/2$
H1	DREF5	F6
H2	DREF4	F8
H10	AUXOUT1	$V_{CC}/2$
H11	AUXOUT0	$V_{CC}/2$
J1	DREF3	F7
J2	DREF1	F5
J5	A1	F10
J6	DCONT5	F6
J7	DCONT4	F8
J10	GND	GND
J11	AUXOUT2	$V_{CC}/2$
K1	DREF2	F6
K2	V_{CC}	V_{CC}
K3	RLOAD#	F3
K4	CLOAD#	F3
K5	A0	F9
K6	DCONT6	F7
K7	DCONT2	F6
K8	OEA#	F11
K9	AUXOUT6	$V_{CC}/2$
K10	AUXOUT4	$V_{CC}/2$
K11	AUXOUT3	$V_{CC}/2$
L1	DREF0	F4
L2	GND	GND
L3	TXFR#	F2
L4	A2	F11
L5	DCONT7	F8
L6	DCONT1	F5
L7	DCONT3	F7
L8	DCONT0	F4
L9	AUXOUT8	$V_{CC}/2$
L10	AUXOUT7	$V_{CC}/2$
L11	AUXOUT5	$V_{CC}/2$

NOTES:

1. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
2. 47kΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5 ± 0.5V.
4. 0.1μF (min) capacitor between V_{CC} and GND per position.
5. FO = 100kHz ± 10%, F1 = F0/2, F2 = F1/2 . . . F11 = F10/2, 40 - 60% Duty Cycle.
6. Input Voltage Limits: V_{IL} = 0.8V max, V_{IH} = 4.5 ± 10%.

Metal Topology

DIE DIMENSIONS:

254 x 214 x 19 ± 1mils

METALLIZATION:

Type: Si - Al or Si-Al-Cu
Thickness: 8kÅ

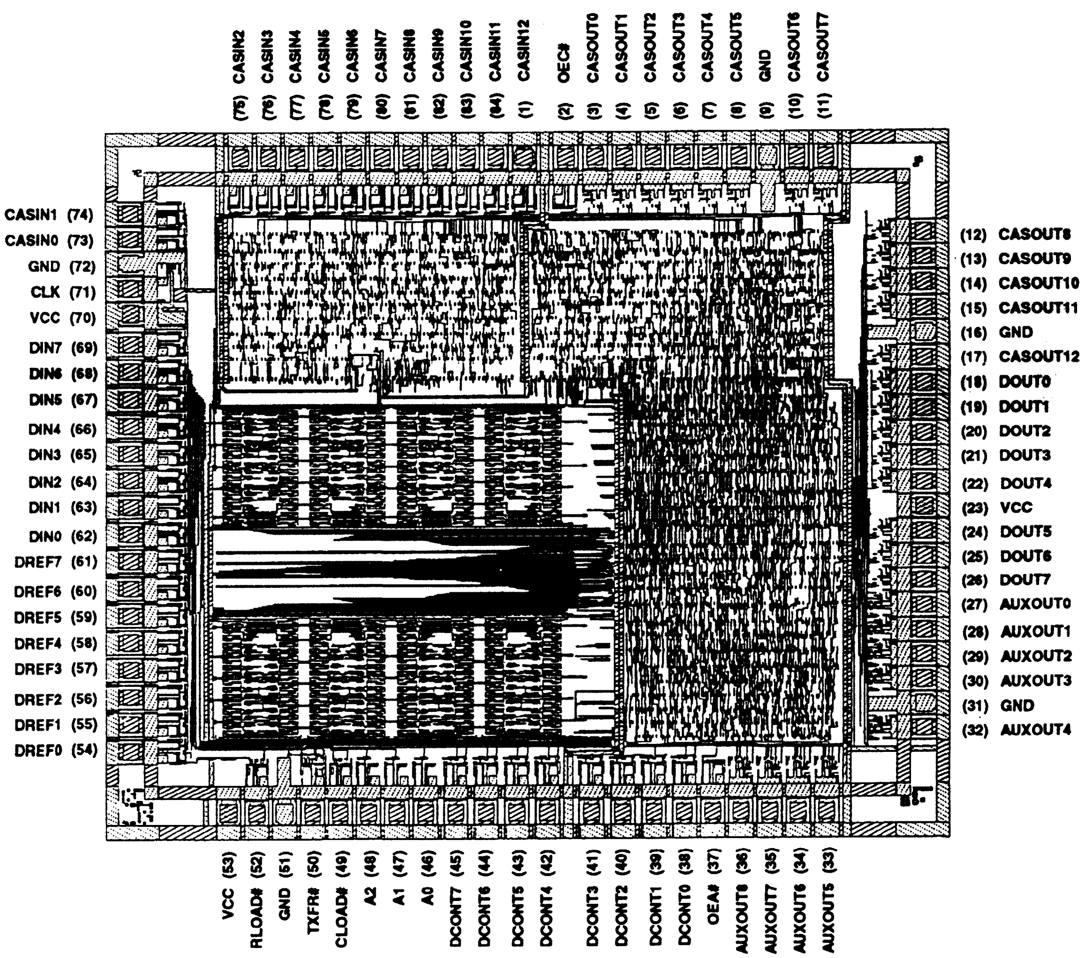
GLASSIVATION:

Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:

0.96 x 10^5 A/cm^2

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HSP9520, HSP9521

February 1994

Multilevel Pipeline Registers

Features

- Four 8-Bit Registers
- Hold, Transfer and Load Instructions
- Single 4-Stage or Dual-2 Stage Pipelining
- All Register Contents Available at Output
- Fully TTL Compatible
- Three-State Outputs
- High Speed, Low Power CMOS

Applications

- Array Processor
- Digital Signal Processor
- A/D Buffer
- Telecommunication
- Byte Wide Shift Register
- Mainframe Computers

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP9520CP	0°C to +70°C	24 Lead Plastic DIP
HSP9520CS	0°C to +70°C	24 Lead SOIC
HSP9521CP	0°C to +70°C	24 Lead Plastic DIP
HSP9521CS	0°C to +70°C	24 Lead SOIC

Description

These devices are multilevel pipeline registers implemented using a low power CMOS process. They are pin for pin compatible replacements for industry standard multilevel pipeline registers such as the L29C520 and L29C521. The HSP9520 and HSP5921 are direct replacemens for the AM29520 and AM29521 and WS59520 and WS59521.

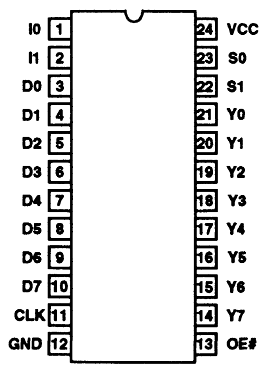
They consist of four 8-bit registers which are dual ported. They can be configured as a single four level pipeline or a dual two level pipeline. A single 8-bit input is provided, and the pipelining configuration is determined by the instruction code input to the I0 and I1 inputs (see instruction control).

The contents of any of the four registers is selectable at the multiplexed outputs through the use of the S0 and S1 multiplexer control inputs (see register select).The output is 8-bits wide and is three-stated through the use of the OE# input.

The HSP9520 and HSP9521 differ only in the way data is loaded into and between the registers in dual two-level operation. In the HSP9520 when data is loaded into the first level the existing data in the first level is moved to the second level. In the HSP9521 loading the first level simply causes the current data to be overwritten. Transfer of data to the second level is achieved using the single four level mode (I1, I0 = '0'). This instruction also causes the first level to be loaded. The HOLD instruction (I1, I0 = '1') provides a means of holding the countents of all registers.

Pinout

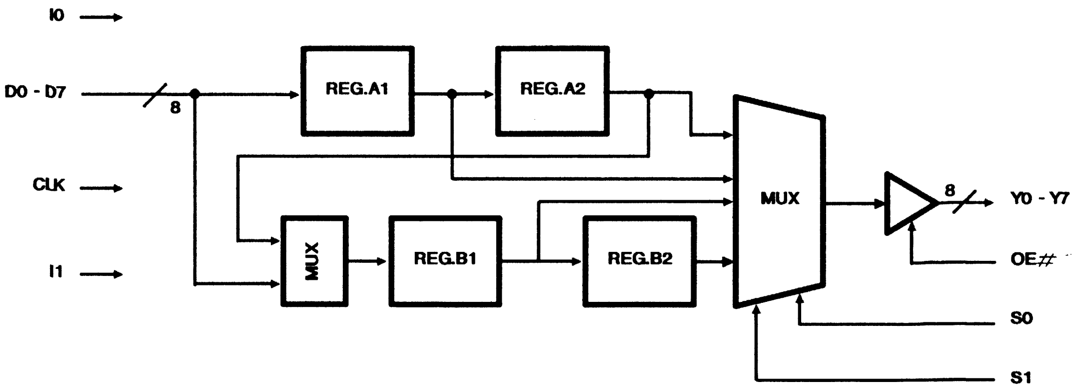
HSP9520, HSP9521 (24 PIN SOIC, NPDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2811.4**

Block Diagram



Pin Descriptions

NAME	DIP PIN	TYPE	DESCRIPTION
V_{CC}	24		The +5V power supply pin. A 0.1μF capacitor between the V_{CC} and GND pin is recommended.
GND	12		The device ground.
CLK	11	I	Input Clock. Data is latched on the low to high transition of this clock signal. Input setup and hold times with respect to the clock must be met for proper operation.
D0-7	3-10	I	Data Input Port. These inputs are used to supply the 8 bits of data which will be latched into the selected register on the next rising clock edge.
Y0-7	21-14	O	Data Output Port. This 8-bit port provides the output data from the four internal registers. They are provided in a multiplexed fashion, and are controlled via the multiplexer control inputs (S0 and S1).
I0, I1	1, 2	I	Instruction Control Inputs. These inputs are used to provide the instruction code which determines the internal register pipeline configuration. Refer to the Instruction Control Table for the specific codes and their associated configurations.
S0, S1	23, 22	I	Multiplexer Control Inputs. These inputs select which of the four internal registers' contents will be available at the output port. Refer to the Register Select Table for the codes to select each register.
OE#	13	I	Output Enable. This input controls the state of the output port (Y0-Y7). A LOW on this control line enables the port for ouput. When OE# is HIGH, the output drivers are in the high impedance state. Internal latching or transfer of data is not affected by this pin.

7

SPECIAL FUNCTION

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input or Output Voltage Applied .... GND -0.5V to V_{CC} +0.5V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +300°C

Operating Conditions

Operating Voltage Range .... +4.75V to +5.25V
Operating Temperature Range .... 0°C to +70°C
Reliability Information
θ_{ja} .... 51.4°C/W (DIP), 77.0W/°C (SOIC)
θ_{jc} .... 22.3°C/W (DIP), 23.2W/°C (SOIC)
Maximum Package Power Dissipation.... 1.5W (DIP), 1.0W (SOIC)

D.C. Electrical Specifications (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.0	-	V	V_{CC} = 5.25V
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = 4.75V
Output HIGH Voltage	V_{OH}	2.4	-	V	I_{OH} = -6.5mA, V_{CC} = 4.75V
Output LOW Voltage	V_{OL}	-	0.5	V	I_{OL} = +20.0mA, V_{CC} = 4.75V
Input Leakage Current	I_I	-10	10	μA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V
Output Leakage Current	I_O	-10	10	μA	V_{OUT} = V_{CC} or GND V_{CC} = 5.25V
Standby Power Supply Current	I_{CCSB}	-	500	μA	V_{IN} = V_{CC} or GND V_{CC} = 5.25V Outputs Open
Operating Power Supply Current	I_{CCOP}	-	12	mA	f = 5.0MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.25V, Ouputs Open, Note 1

Capacitance (T_A = +25°C, Note 3)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Capacitance	CIN	-	12	pF	FREQ = 1 MHz, V_{CC} = Open, all measurements are referenced to device ground.
Output Capacitance	CO	-	12	pF	

A.C. Electrical Specifications (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C, Note 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS (Note 2)
Clock to Data Out	T_{PD}	-	21	ns	
Mux Select to Data Out	T_{SELD}	-	20	ns	
Input Setup Time (D0-7/I0-7)	T_S	10	-	ns	
Input Hold Time (D0-7/I0-7)	T_H	3	-	ns	
Output Enable Time	T_{ENA}	-	20	ns	
Output Disable Time	T_{DIS}	-	13	ns	Note 3
Clock Pulse Width	T_{PW}	10	-	ns	

NOTES:

1. Power supply current is proportional to frequency. Typical rating for I_{CCOP} is 2.4mA/MHz.
2. A.C. Testing is performed as follows: Input levels: 0V and 3.0V, Timing reference levels = 1.5V, Input rise and fall times driven at 1ns/V, Output load C_L = 40pF.
3. Controlled by design or process parameters and not directly tested. Characterized upon initial design and after major design and/or process changes.

Timing Waveform

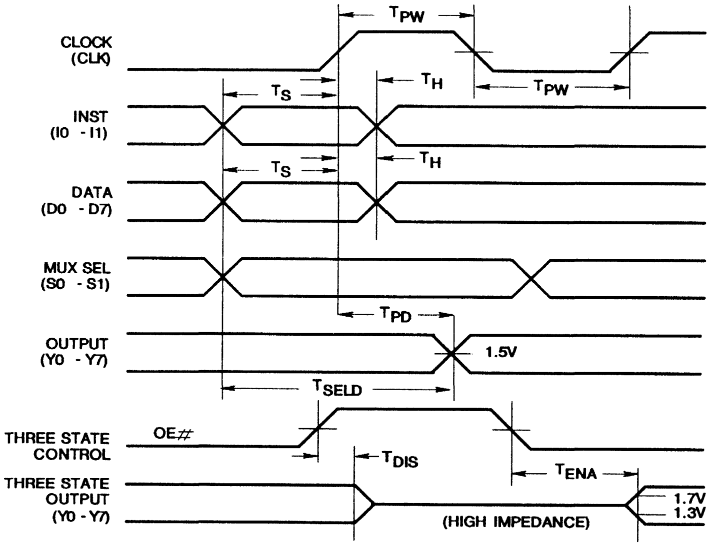


TABLE 1. INSTRUCTION CONTROL

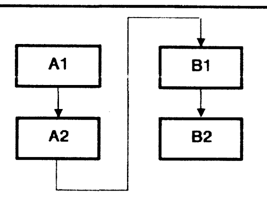
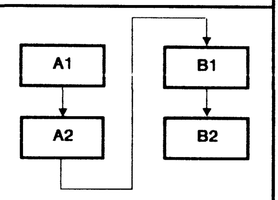
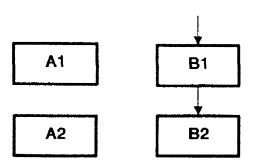
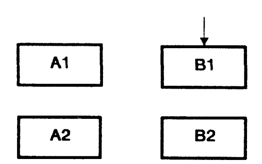
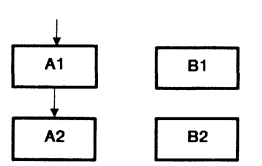
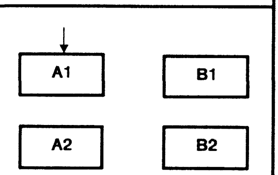
I1	I0	'9520	'9521
0	0		
0	1		
1	0		
1	1	ALL REGISTERS HOLD	ALL REGISTERS HOLD

TABLE 2. REGISTER SELECT

S1	S0	'9520 OR '9521
0	0	B2
0	1	B1
1	0	A2
1	1	A1

DSP 8

DEVELOPMENT TOOLS

NOTE: Bold Type Designates a New Product from Harris.

8

DEVELOPMENT TOOLS

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HARRIS SEMICONDUCTOR

DECI•MATE™

Harris HSP43220 Decimating Digital Filter Development Software

January 1994

Harris DECI • MATE Development Software assists the design engineer to prototype designs for the Harris HSP43220 Decimating Digital filter (DDF). Developed specifically for the DDF, this software consists of three integrated modules: DDF Design, DDF Simulator and DDF PROM. The Design module designs a filter from a set of user specifications for the DDF. The Simulator module models the DDF's internal operation. The PROM module uses the device configuration created by the Design module to build a PROM data file that can be used to store and download the DDF configuration.

DDF System Design

The DDF consists of two stages: a High Decimation Filter (HDF) and a Finite Impulse Response (FIR) filter. Together these provide a unique narrow band, low pass filter. Because of this unique architecture, special software is required to configure the device for a given set of filter parameters. This software uses system level filter parameters (listed below) to perform the trade off analysis and calculate the values for the DDF's configuration registers and FIR coefficients.

Design specifications are supplied by the user in terms of:

1. Input sample frequency
2. Required output sample frequency
3. Passband signal bandwidth
4. Transition bandwidth
5. Amount of attenuation allowed in the passband
6. Amount of stopband attenuation required for signals outside of the band of interest.

This information is entered into a menu screen (See Figure 1), providing immediate feedback on the design validity. The design module calculates the order of the HDF, HDF decimation required, the FIR input data rate, minimum clock frequency for the FIR, FIR order and decimation required in the FIR.

The design module will then generate the FIR filter. Four different methods are provided for the FIR design:

1. A Standard FIR automatically designed by the module using the Parks-McClellan method to compute the coefficients of an equiripple (Chebyshev) filter.
2. Any FIR imported into the Design module from another FIR design program.
3. A precompensated FIR which is automatically designed by the module to compensate for the roll-off in the passband of the HDF frequency response.
4. The FIR may also be bypassed in which case the optimal HDF is designed from the user specifications.

Frequency response curves are then displayed showing the resulting responses in the HDF, FIR and for the entire chip using the given filter design. Figure 2 is a typical display. The user may save this frequency response data for further analysis. The design module also creates a report file documenting the filter design and providing the coefficients and setup register values for programming the device.

DDF Simulator

The simulator provides an accurate simulation of the device before any hardware is built. It can be used to simulate any filter designed with DECI • MATE. The simulator takes into account the fixed point bus widths and pipeline delays for every element in the DDF.

The simulator provides the user with an input signal which can be used to stimulate the filter. This signal is created from the options shown in Table 1. The user can select a pure step, impulse, cosine, chirp, uniform or Gaussian noise as the input signal, or a more complex signal can be generated by combining that data with an option selected from the Signal #2 column, with the combining operator chosen from the middle column. The user can also import a signal from an outside source.

TABLE 1.

SIGNAL #1	OPERATION	SIGNAL #2
Step		Step
Impulse	No Operation	Impulse
COSINE	Add	COSINE
Chirp	Concatenate	Chirp
Uniform Noise	Multiply	Uniform Noise
Gaussian Noise		Gaussian Noise
	Imported From Outside	

Probes are provided to select specific areas to graphically display data values as well as save into data files for further processing. The DDF Simulator has two levels; the DDF Simulator Specification screen and the DDF Simulator Main Screen.

The specification screen (see Figure 3) is used to input the simulation parameters. The users selects display modes in either continuous or decimated format and data formats in either decimal or hexadecimal. The specification screen also provides for selection of the input signal.

The simulator main screen (see Figure 4) defines the simulator test probes and displays the data values per clock cycle. The interactive simulator screen consists of the HSP43220 block diagram, test probes and register contents. The user selects the step size of the input sample clock and also selects the probes to be monitored. The simulator will then clock through the specified number of clock cycles and display the resulting time domain response. Figure 5 shows a typical probe display.

HARRIS SEMICONDUCTOR

HSP45116-DB

USER'S MANUAL

January 1994

HSP45116 Daughter Board

Features

- **Designed for use with HSP-EVAL**
- **Access to HSP45116's input, output, and control signals through three 50 Pin Headers**
- **HSP45116 control signal states may be set through hardware configuration or software.**
- **Two separate software packages for daughter board I/O and control**
- **High speed I/O supported**

Applications

- **PC Based performance analysis of HSP45116 when used with HSP-EVAL**
- **Rapid prototyping**

Description

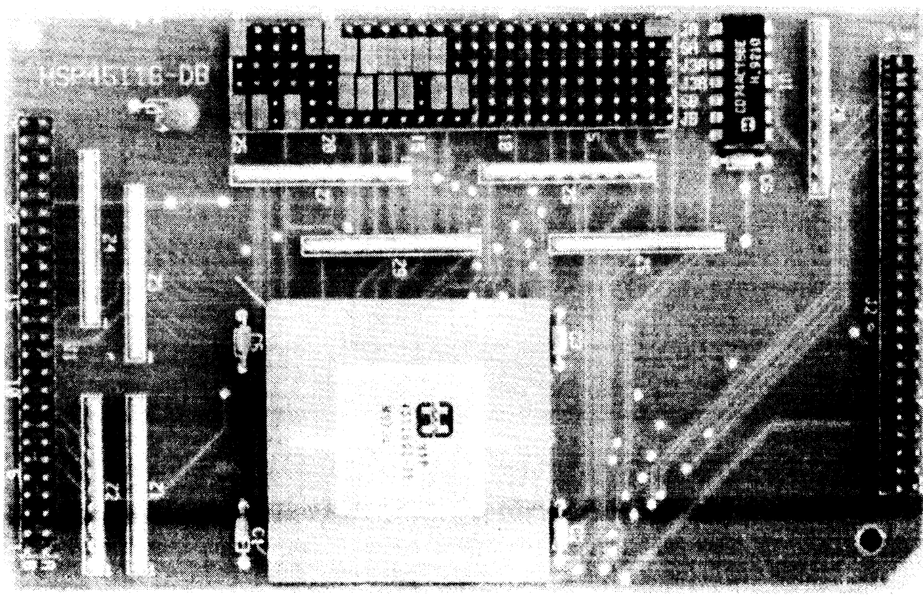
The HSP45116-DB is a daughter board designed to mate with the HSP-EVAL for rapid evaluation and prototyping of the HSP45116 Numerically Controlled Oscillator Modulator. Together, the board set provides a mechanism to evaluate HSP45116 operation using IBM PC™ based I/O and control. As shown in the Figure 1, the HSP45116-DB maps the input, output, and control signals of the HSP45116 to three 50 pin headers. These headers mate with connectors on board the HSP-EVAL to interface the HSP45116's various I/O and control signals with the HSP-EVAL's data busses. This interface establishes a path for PC™ based I/O and control of the HSP45116-DB via the HSP-EVAL.

An IBM PC™ based software package is supplied which controls operation to the HSP45116-DB/HSP-EVAL board set. The software package provides the user with a DOS command line interface and graphical user interface for daughter board I/O and control. Since the software supports data acquisition from the HSP45116, software based signal analysis may be used to quantify part performance.

The degree of control exerted by the software varies depending upon the clock supplied to the HSP45116-DB. If a high speed clock is supplied via the HSP-EVAL's on board oscillator or external clock pin, the software can be used to exert real time control. If a software controlled clock is provided, the HSP45116-DB can be driven with a user defined data set while storing results back to the PC for later analysis.

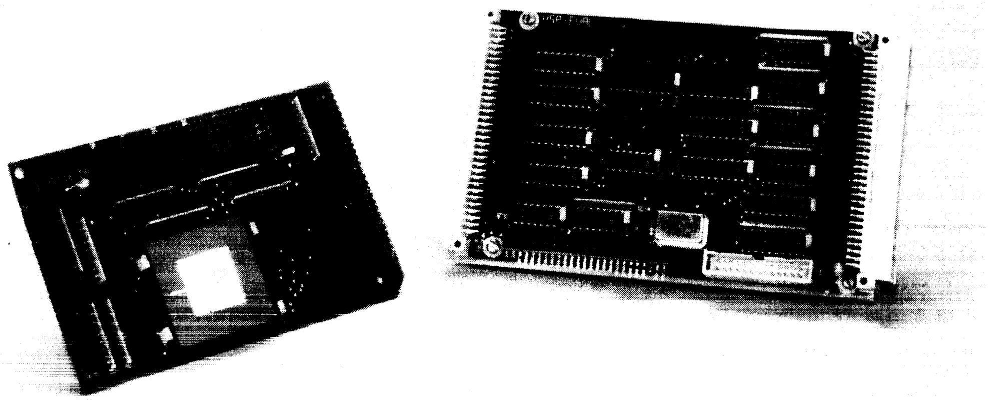
The HSP45116-DB is a 6 layer printed circuit board which comes populated with one HSP45116GC-25. The PC based software required to control the daughter board via the HSP-EVAL is also provided

HSP45116 Daughter Board



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3367.



The evaluation hardware for the HSP family of products consists of the motherboard, which forms the interface to the PC, and the daughterboard, which carries the part under evaluation.

The hardware to evaluate the HSP45116 consists of the HSP-EVAL motherboard and the HSP45116-DB daughterboard. Two software packages are provided for the data and control interface between the HSP45116-DB and the PC. One is menu driven and the other accepts DOS command lines.

HARRIS SEMICONDUCTOR

HSP50016-EV

USER'S MANUAL

January 1994

DDC Evaluation Platform

Features

- Single HSP50016-EV may be Used to Evaluate the HSP50016
- May be Daisy Chained to Support Evaluation of Multi-Chip Solutions
- Parallel Port Interface to Support IBM PC™ Based Evaluation and Control
- Three Clocking Modes for Flexibility in Performance Analysis and Prototyping
- Dual 96-Pin Input/Output Connectors Conforming to the VME J2/P2 Connector Standard

Applications

- PC Based Performance Analysis of HSP50016
- Rapid Prototyping

Description

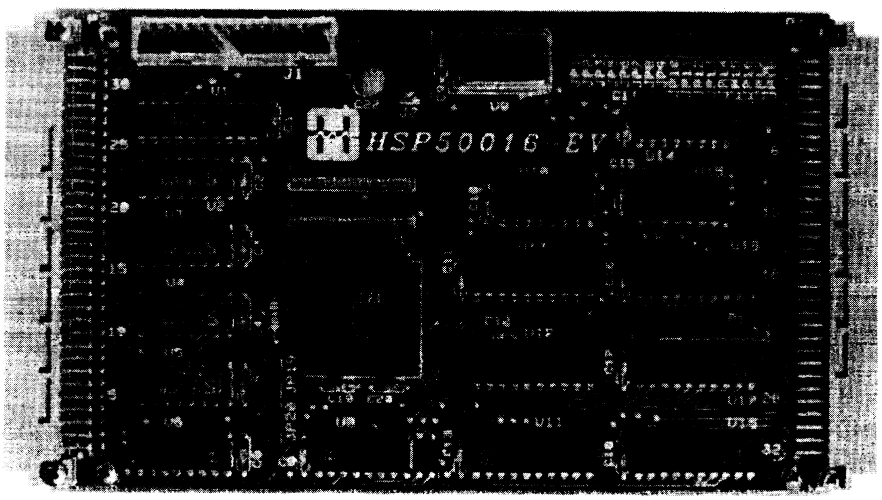
The HSP50016-EV is the evaluation board for the HSP50016 Digital Down Converter (DDC). It provides a mechanism for rapid evaluation and prototyping. The HSP50016-EV consists of a series of busses which provide input, output, and control to the DDC. These busses are brought out through dual 96 Pin connectors to support daisy chaining HSP50016-EV's with other Harris evaluation boards for multichip prototyping and evaluation.

For added flexibility, the input and control busses can be driven by registers on-board the HSP50016-EV which have been down loaded with data via the parallel printer port of an IBM PC™ or compatible. In addition, the DDC output can be read into the PC via the status lines of the parallel port. Together, the I/O and Control registers can be used to drive the target DDC with a PC based vector set while collecting output data on the PC's disk.

Jumper selectable clock sources provide three different methods of clocking the part under evaluation. In mode one, the clock signal is generated under PC based software control. In mode two, the HSP50016-EV's on-board oscillator may be selected as the clock source. In mode three, the user may provide an external clock through the 96 pin input connector.

The HSP50016-EV was built into a 3U Euro-Card form factor with dual 96-pin Input/Ouput connectors. The I/O connectors conform to the VME J2/P2 connector standard.

HSP50016 Evaluation Platform



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DSP 9

APPLICATION NOTES AND TECH BRIEFS

Harris Semiconductor

APP NOTE

No. AN9401 February 1994 **Harris Digital Signal Processing**

REDUCING THE MINIMUM DECIMATION RATE OF THE HSP50016 DIGITAL DOWN CONVERTER

Author: Dr. David B. Chester

Introduction

This application note discusses a method for reducing the minimum decimation rate of the Harris HSP50016 Digital Down Converter (DDC). As will be described in detail in this application note, reduction in the minimum decimation rate is accomplished by first sample rate expanding the data stream which would normally be directly input to the DDC by a factor L (placing L-1 zero valued samples between each sampled data point). While the sample rate expansion process reduces the maximum input sampling rate that the aggregate circuit (DDC and sample rate expander) can accept by a factor of L, the ratio of the maximum output bandwidth to input sample rate of the aggregate circuit is increased by a factor of L. The output bandwidths as a function of HDF decimation rate M_1, aggregate circuit input sample rate f_{SA}, and sample rate expansion L are:

$$-3dB\ BW = 0.13957\ Lf_{SA}/M_1 \quad (1)$$

$$-102dB\ BW = 0.19903\ Lf_{SA}/M_1. \quad (2)$$

The DDC is a fully programmable single chip down converter architected to meet a wide range of down convert applications. A top level functional block diagram of the DDC architecture is shown in Figure 1. The principal goal of the DDC is to filter and translate a band of interest to baseband and to output the band of interest at a sample rate commensurate with its bandwidth.

The decimation occurs in a two step process. Once the center of the band of interest is shifted to DC by the quadrature modulator the real and imaginary outputs are each passed to a high decimation filter (HDF). The decimation rate of the HDFs, denoted M_1, is programmable from a minimum of 16 to a maximum of 32,768. The outputs of the HDF filters must be scaled for gain compensation.

The lowpass response of the HDF has a gradual roll off characteristic requiring a subsequent conventional FIR to achieve a sharp transition. The DDC employs a fixed shaping filter for ease of use. The output bandwidth of the DDC is a function of the input sampling rate, the programmable HDF decimation rate and the fixed shape of the FIR. This relationship is:

$$-3dB\ BW = 0.13957\ f_S/M_1 \quad (3)$$

$$-102dB\ BW = 0.19903\ f_S/M_1 \quad (4)$$

where BW is the double sided bandwidth and fs is the input sample rate.

The FIR filter's passband compensates for the roll-off inherent in the passband of the HDF filter to meet the goal of a low passband ripple [1].

The FIR filter automatically decimates by a factor of 4 if a quadrature output format has been selected. When a real output is selected, the FIR filters in the DDC automatically decimate by a factor of 2. The FIR decimation rate is

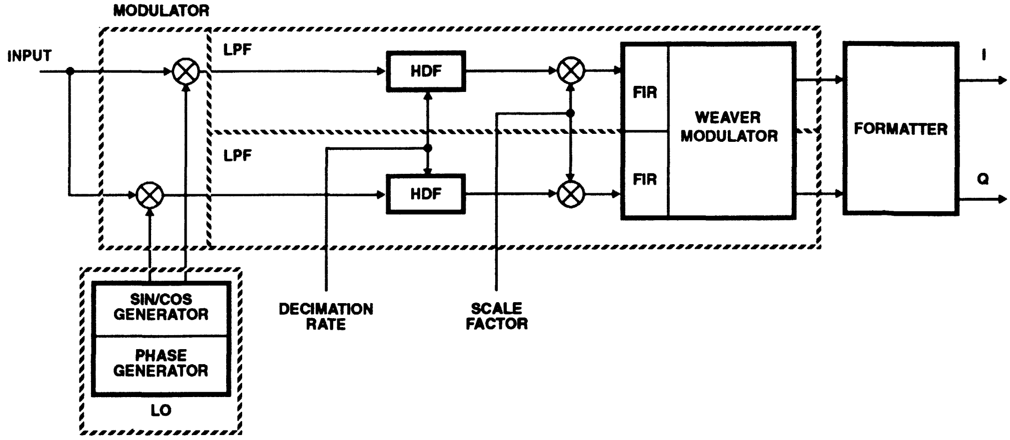

FIGURE 1. DDC FUNCTIONAL BLOCK DIAGRAM

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denoted M_2. In the real output mode the FIR outputs are spectrally shifted by one fourth of the output sampling frequency and combined to produce a two sided spectrum. This process is conceptually performed by the Weaver Modulator [2] following the FIR filter pair.

For quadrature output mode we see that the minimum DDC decimation rate is

$$\min(M) = \min(M_1) \times M_2 = 16 \times 4 = 64. \quad (5)$$

The minimum decimation rate for real output mode is 32.

The resulting signal is converted into one of several selectable formats for output. See reference [1] for a detailed description of the DDC and its operation.

A simple procedure can be used to reduce the minimum aggregate decimation rate of the DDC with a minimum of external circuitry. The trade-off in reducing the aggregate decimation rate is a one to one reduction in maximum input sampling rate.

Reduction of the Minimum Decimation Rate

The minimum decimation rate of the DDC can be reduced by using a minimal amount of external circuitry to convert the DDC from a strictly decimating device to a rate change device. By doing this, the DDC and external circuitry can first interpolate the input signal to a higher sampling rate before decimating it. This restricts the sampling frequency, and correspondingly the bandwidth, of the input signal to be less than the clock frequency of the DDC. The result however is a reduction in the end-to-end decimation rate of the aggregate circuit.

A rate change filter is an interpolation filter combined with a decimation filter. The combining of the actual filtering processes is done by implementing the filter process that requires the narrowest bandwidth of the two.

Because interpolation via digital filtering is not introduced in the DDC data sheet, it is presented at a top level here.

Interpolation

Interpolation is the increase in the sampling rate of a signal while preserving its original spectral content. The first step in interpolation is to stuff L-1 zero valued samples between each valid input sample to expand the sampling rate by a factor of L. The zero stuffing causes the original signal spectrum to be repeated L-1 times. To perform the actual interpolation the zero valued input samples must be converted to approximations of signal samples. This is equivalent to preserving the original signal spectrum. Thus, the zero stuffed input stream is filtered by a lowpass filter which has its passband at the original spectrum location and filters out all of the repeated spectra. This process is shown pictorially in Figure 2.

Rate Change

The top level block diagram of a rate change filter [2] is shown in Figure 3A. In the diagram the sampling rate of the incoming signal is first expanded by a rate L by placing L-1 zero valued samples between each original sample. The lowpass filter following the sample rate expander is designed to: 1) remove the L-1 spectral images which result from the zero padding; 2) multiply the result by a gain of L to compensate for the power loss that occurs when the spectral images are removed; and 3) limit the width of the spectrum to allow sample rate compression by M without aliasing. An example of this process is illustrated spectrally in Figure 3B.

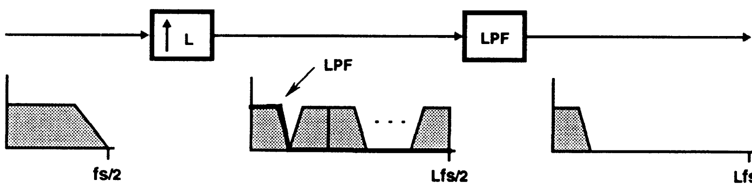

FIGURE 2. BLOCK DIAGRAM SPECTRAL REPRESENTATION OF THE RATE CHANGE PROCESS

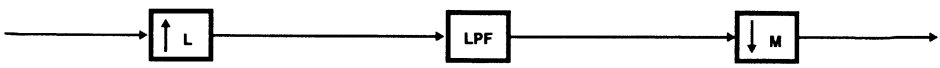

FIGURE 3A. TOP LEVEL BLOCK DIAGRAM OF A RATE CHANGE FILTER

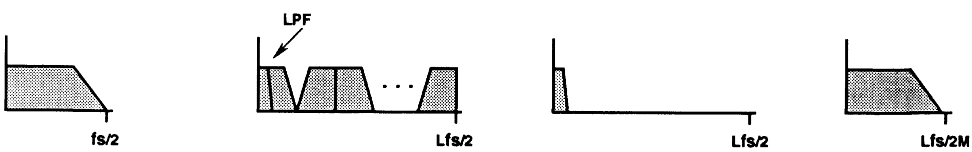

FIGURE 3B. SPECTRAL REPRESENTATION OF THE RATE CHANGE PROCESS

The first and third design criteria are combined by taking the more severe (narrowest bandwidth & shape factor) of the two.

In most implementations the least common denominator (LCD) of L and M is 1. In the application described here this is not generally true because the DDC itself is not a rate change device.

The DDC in a Rate Change Configuration to Reduce the Minimum Decimation Rate

Figure 4 shows a conceptual block diagram of the modulation and filter processes in one of the two real processing chains in the DDC. The two stage decimation filter configuration is a conventional architecture [2] with the exception of the scaling multiplier between the first sample rate compressor and the second lowpass filter. The scaling multiplier is used to compensate for the variable gain of the programmable HDF [1,3,4,5,].

The input to the DDC is first multiplied by a sinusoid from the digital local oscillator (LO). The sinusoids for the inphase and quadrature paths are offset in phase by 90 degrees. The product is passed to the HDF.

Placing a sample rate expander in front of the HDF and using the fact that the multiplication of the input signal by the LO is a linear operation we can redraw Figure 4 to get the rate change capability shown in Figure 5.

In the configuration shown in Figure 5 it is assumed that the constraint placed on the lowpass filtering by decimation is more severe than the interpolation constraint. This is in general the case when the decimation rate of the DDC is higher than the interpolation rate being generated by the external sample rate expander.

From Figure 5 it can be seen that the sample rate of the input to the sample rate expander has a maximum value of clk/L where clk is the DDC clock.

The sample rate expander can be constructed simply as a divide by L counter and a series of AND gates. Example implementations are shown later in this applications note.

Example: Decimation By 8

As an example case we will use the DDC to decimate by 8 with a quadrature output. In this example the HDF section is programmed to decimate by the minimum value of 16 and the FIR section automatically decimates by 4. The aggregate DDC decimation rate is 16 x 4 = 64. To get a decimation rate of 8 we must interpolate by

$$L = \frac{\text{DDC Decimation}}{\text{Desire Decimation}} \tag{6}$$

$$= 64/8 = 8$$

The sample rate expander therefore pads 7 zero samples between each sample that enters it. The maximum sampling frequency of the input signal is clk/8. For a maximum DDC clock of 75MHz the maximum input clock for this example is 9.375MHz.

Assume that the input signal is wideband and that it is sampled at 2.5 times the highest frequency of interest. The resulting spectrum at the input to the sample rate expander is shown in Figure 6. Notice in the figure that to relax the anti-aliasing filter design, aliasing is allowed to occur at frequencies above the maximum frequency of interest.

When the input signal has passed through the sample rate expander and has been padded with 7 zero samples between each input sample the one sided spectrum illustrated in Figure 7 results. Also shown in the figure is the HDF lowpass response. Notice that the power in the original signal and each image is reduced by 18dB from the input power level, defined as 0dB in the figure. This phenomenon occurs in digital interpolation because padding by L-1 zeros adds L-1 spectral repetitions without adding power.

The interpolation process is completed by removing the spectral images via a lowpass filter operation. This loss of power of 20 x log(L) dB in the filtering operation would result in a corresponding loss in dynamic range if it is not corrected for.

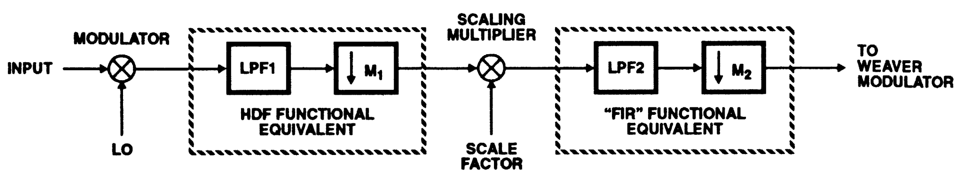

FIGURE 4. CONCEPTUAL BLOCK DIAGRAM OF ONE SIDE OF THE DDC MODULATION AND FILTER PROCESS

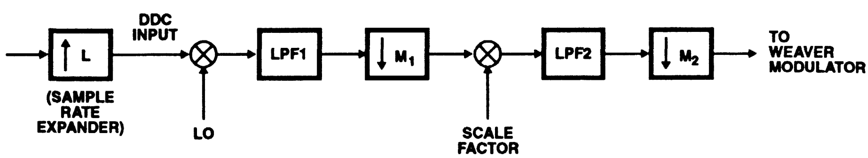

FIGURE 5. CONCEPTUAL BLOCK DIAGRAM OF ONE SIDE OF THE DDC MODULATION AND FILTER PROCESS WITH A SAMPLE RATE EXPANDER

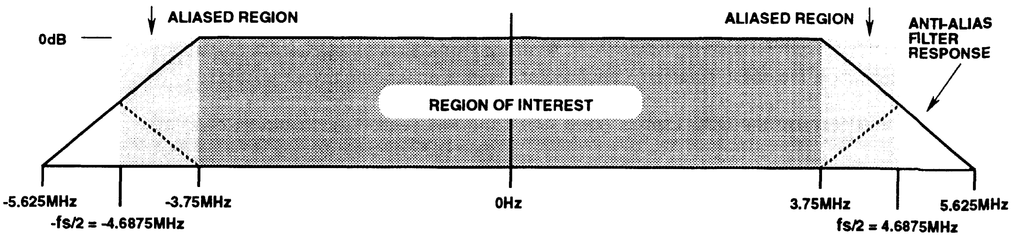

FIGURE 6. SPECTRUM OF DIGITAL INPUT SIGNAL

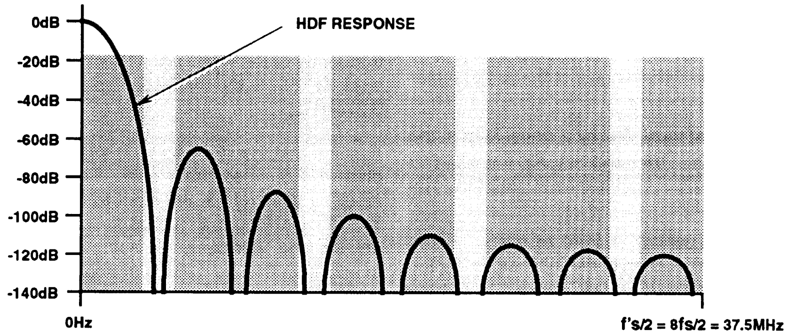

FIGURE 7. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE SUPERIMPOSED

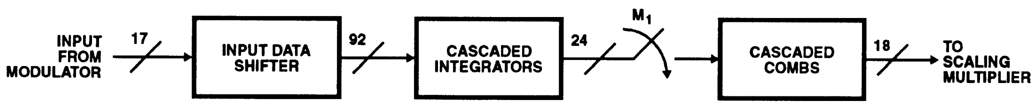

FIGURE 8. TOP LEVEL BLOCK DIAGRAM OF THE HIGH DECIMATION FILTER

The output -3dB bandwidth can be calculated from equation 1 where f_{SA} is equal to 9.375 megasamples per second (MSPS). We get:

-3dB BW = 0.13957 x 8 x 9.375MSPS/16 = 654.234kHz.

From this result we see that for a DDC clock of 75MHz the maximum output bandwidth has not changed. What has changed is the maximum output bandwidth relative to the actual input sample rate of 9.375MSPS.

Implementation Details

Figure 8 shows a more detailed block diagram of the HDF. The HDF is an efficient, multiplier free, decimating lowpass filter for moderate to high decimation rates[3]. As shown in the figure, the HDF actually decimates before completion of the filtering process. However, the process is functionally equivalent to the process of filtering by LPF1 followed by sample rate compression by a rate M_1 shown in Figure 4.

The frequency domain response of an unscaled HDF is:

$$H(f) = (\mathrm{Sin}(\pi f)/\mathrm{Sin}(\pi f/M_1))^5 \qquad (7)$$

The DC gain of this response is M_1^5. This gain must be compensated for by multiplying by the inverse of the DC gain. The gain compensation is distributed between the input and output of the HDF in the DDC implementation. The gain compensation at the input of the HDF is accomplished via a shift register labeled the Input Data Shifter in Figure 8. Consequently, this gain compensation is in the form of powers of two. The gain compensation at the output of the HDF is accomplished via a multiplier. The multiplier compensates for non powers of two in the gain compensation.

The HDF Input Data Shifter positions the input data, as a function of the HDF decimation rate, so that the MSB of the output data will be aligned with the MSB of the output bus. The data shifter is programmed in terms of a data shift value. That is, the number of bits between the LSB of the input to the HDF and the LSB of the HDF. The data shift equation is:

$$\text{Data Shift} = 75 - \mathrm{Ceiling}(5 \log_2(M_1)). \qquad (8)$$

where Ceiling(**X**) denotes taking the next greatest integer if X has a non integer component. In point of fact, the shift divides the HDF gain by a value which is greater than or equal to M_1^5 to guarantee that the input to the scaling multiplier is between 0.5 non inclusive and 1 inclusive. For a detailed explanation see reference [3].

After the data shift has been performed the HDF gain at the output is given by

$$\text{HDF Gain} = M_1^{\,5} / 2^{\text{CEILING}(5\text{LOG}_2(M_1))} \qquad (9)$$

The compensating scale factor, which is the input to the Scaling Multiplier quantized to 16 bits, is given by the equation:

$$\text{Scale Factor} = 2^{\text{CEILING}(5\text{LOG}_2(M_1))}/M_1^{\,5} \qquad (10)$$

The computed scale factor can take on values from 1 inclusive to 2 non inclusive. The programmable quantized scale factor can take on values from 0 to $2 - 2^{-15}$.

The validity of the HDF gain equation is predicated on the correct programming of the HDF data shifter. See referenced [1] for details.

The following two examples are used to illustrate the gain compensation procedure.

Example 1: $M_1 = 512$

In this example we are decimating by a power of 2. The Data Shift value is

$75 - \text{Ceiling}(5 \log_2(512)) = 30.$

The Scale Factor value is

$2^{\text{CEILING}(5\text{LOG}_2(512))}/512^5 = 1.$

Example 2: $M_1 = 513$

The Data Shift value is

$75 - \text{Ceiling}(5 \log_2(513)) = 29.$

The Scale Factor value is

$2^{\text{CEILING}(5\text{LOG}_2(513))}/513^5 = 1.98058267$

Interpolation Gain Compensation

An explanation of how to preserve the DDC's dynamic range when reducing its minimum decimation rate is now given in detail. In most normal operating conditions this procedure is simple and straight forward. Under certain worst case conditions however, special considerations must be made. We describe the straight forward case first. We then describe how to handle the worst case conditions.

The removal of spectral images created in the sample rate expansion process is accomplished by the lowpass filtering in the DDC. As mentioned above, the removal of the images results in a loss in gain since no power is added to the signal during the sample rate expansion process. Power is removed in the lowpass filter process. Dynamic range through the DDC can be preserved by compensating for the gain loss due to the spectral image removal by adjusting the gain through the HDF.

Because the lowpass filter process is a two step process involving the HDF and FIR, the HDF may not suppress all images to the attenuation required to prevent overflow during the standard scaling process. This is the case in Figure 14 as will be explained in detail below. As long as the images are suppressed sufficiently to preclude overflow in the HDF and scaling operation however, no distortion occurs in the process.

Standard Gain Compensation

For an example of standard gain compensation, assume that an overall decimation rate of 4 is desired in the DDC. The input samples are expanded by 16 by placing 15 zero valued samples between each input sample. The resulting spectrum is illustrated in Figure 9.

(Note: Figures 9 through 24 show the repeated input spectrum superimposed on the HDF response curve. These superimpositions assume that the down convert frequency is zero. The analysis holds for any valid down convert frequency. Also shown in the figures by the vertical solid lines are the positions of the images of near DC areas of the spectra.)

Assume that the input signal consists of two equal amplitude tones, one at DC (desired in this example) and one at 4/5 of the pre-expanded input sampling frequency (to be ultimately rejected in this example). In the expanded spectrum the DC component repeats as illustrated by the vertical solid lines in Figure 9 and the 4/5 sampling frequency tone is repeated at each interface between the two shaded areas in the figure. Each tone is at -6dB on the pre-expanded input and down 30dB on the expanded spectrum.

To compensate for the gain loss due to the rejection of images requires a 24dB gain in the HDF. The requirement to prevent overflow in the gain compensation operation is that the sum of the signal power after compensation is ≤ 0dB.

As can be seen in Figure 9 all DC images lie in the HDF nulls. Since the original DC component is at -6dB after compensation it is required that the sum of the power in the original 4/5 sampling frequency tone and it's images be ≤ -6dB after compensation. From the HDF curve it is determined that the total power from the tone and its images is approximately -10.9dB. As a result no overflow will occur in the HDF or scaling multiplier due to gain compensation. The residual signals are then filtered in the FIR.

The compensation scale factor required is equal to the interpolation factor, L. Combining the interpolation gain compensation with the HDF response gain compensation we have a total compensation of $L/M_1^{\,5}$. We now rewrite equations 8 and 10 to incorporate the interpolation gain compensation.

$$\text{Data Shift} = 75 - \text{Ceiling}(\log_2(M_1^{\,5}/L)). \qquad (11)$$

Scale Factor =

$$L2^{\text{CEILING}(\text{LOG}_2(M_1/L))}/M_1^{\,5} \qquad (12)$$

Equations 11 and 12 are used when no overflow is possible in the HDF as a result of the interpolation and scaling process.

Special Case 1 - Overflow Possibilities When the Interpolation Factor Is Less Than or Equal to the HDF Decimation Factor

Figures 9 through 23 show interpolated spectra superimposed on the HDF filter response curve for interpolation cases 16 through 2. The figures are supplied to illustrate the possibility of overflow in the extreme case where full scale inputs to the DDC are supplied and all of the dominant spectral components meet two criteria. First, they are all within 1/125th of the main lobe and second, the majority of them generate an image or images that lie at the peaks of the first or second side lobe. (The peak value of the first HDF sidelobe is 1.168 x 10^{-4} which is approximately equal to 1 - the magnitude of the mainlobe at a frequency of 1/125th of the first HDF null.)

(Note: the above paragraph describes a condition, specifically a full scale input, which should not occur in typical operations. The description of this special case is included for completeness.)

To illustrate the potential for overflow in the extreme case described above we select a full scale single tone input which is mixed to DC in the down convert section of the DDC. The dark vertical lines in the figures highlight DC images. Examining Figure 14, the interpolate by 11 example, we see that the first image lies at 6.818MHz for a 75MSPS DDC input rate. This image is very near the 6.713MHz peak of the first HDF sidelobe.

The attenuated magnitude of the first and second images and fifth and sixth (not including the attenuation due to sample rate expansion) sum to approximately 5.109 x 10^{-4}. As a result, if equations 11 and 12 are used for gain compensation then the peak signal value coming out of the HDF would be 1.0005109 and the HDF would overflow. This would generate catastrophic errors.

To correct for the image components we can modify equations 11 and 12 as follows. Let Sc be defined as the sum of the signal component magnitudes in the original spectrum times the normalized HDF response. For a single DC input to the HDF Sc = 1. Let Slg be the sum of the compensated image magnitudes times the normalized HDF response. In the interpolate by 11 example Slg ≅ 0.0005109.

If Sc + Slg is greater than 1 then

Data Shift =

$$75 - \text{Ceiling}(\log_2(M_1{}^5(Sc + Slg)/L)). \quad (13)$$

Scale Factor =

$$L2^{\text{CEILING}(\text{LOG}_2(M_1\,(SC + SLG)/L))}/(Sc + Slg)M_1{}^5 \quad (14)$$

Applying equations 13 and 14 would cause a negligeable loss in dynamic range.

The image power which is passed in the HDF will be removed in the subsequent FIR filter.

It can be observed from Figures 9 through 23 that for the HDF set to decimation by 16 near DC images are so greatly attenuated for interpolation by power of 2 cases that equations 11 and 12 can be used even for peak input conditions.

Special Case 2 - Overflow Possibilities When the Interpolation Factor Is Greater Than the HDF Decimation Factor

It is not recommended to use the DDC in a wideband application which requires an interpolation rate greater than the HDF decimation rate unless a loss in dynamic range can be tolerated. As a general rule a 6dB loss in dynamic range will result for every factor of 2 that the interpolation rate is greater than the decimation rate.

An example of the interpolation factor being greater than the HDF decimation factor is shown in Figure 24. In this example the interpolation factor is 32 and the HDF decimation factor is 16.

As seen in Figure 24 images can lie in the main lobe of the HDF filter curve as well as side lobes. In this case equations 13 and 14 are still applied with the exception that near DC image components in the HDF main lobe must be included in the Slg calculation. Further, the definition of near DC components is now dependent on the number of image components that can lie in the main lobe and the side lobes. The near DC "width" can be calculated by considering the slope of the HDF response curve in the area of the original spectrum and the total magnitude of the images. Since this is highly dependent on the interpolation rate in the case where the interpolation rate is greater than the HDF decimation rate, it is left to the user to derive.

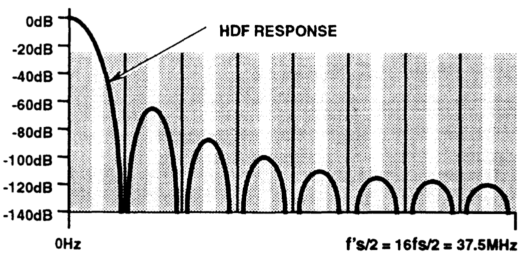

FIGURE 9. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 16 CASE

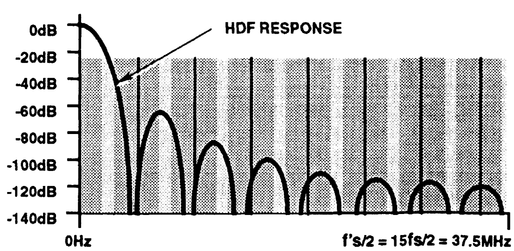

FIGURE 10. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 15 CASE

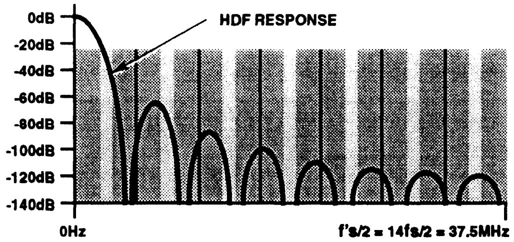

FIGURE 11. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 14 CASE

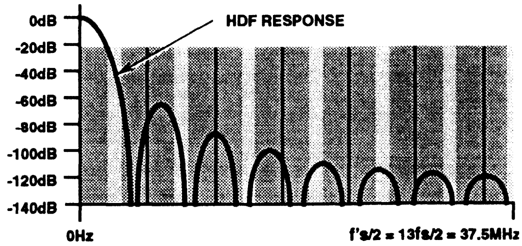

FIGURE 12. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 13 CASE

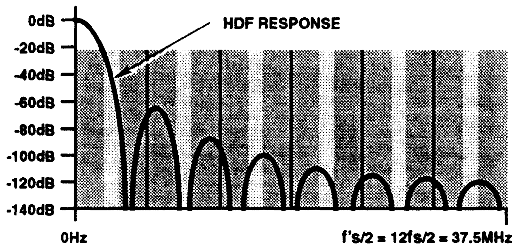

FIGURE 13. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 12 CASE

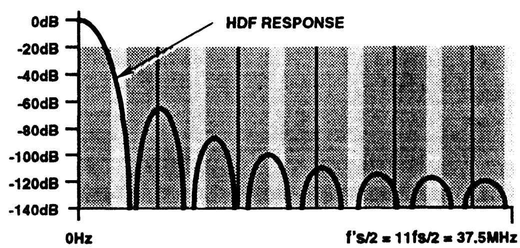

FIGURE 14. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 11 CASE

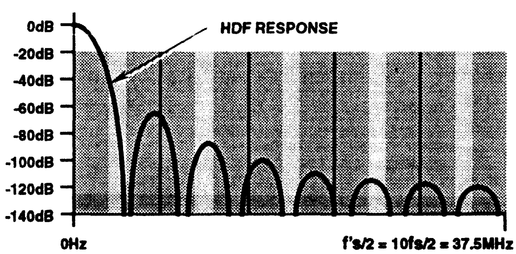

FIGURE 15. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 10 CASE

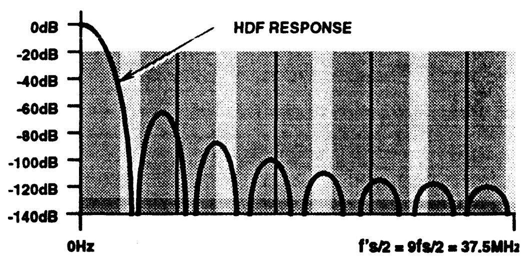

FIGURE 16. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 9 CASE

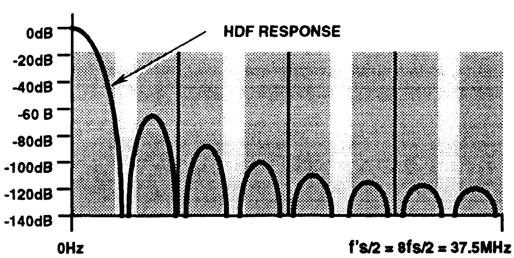

FIGURE 17. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 8 CASE

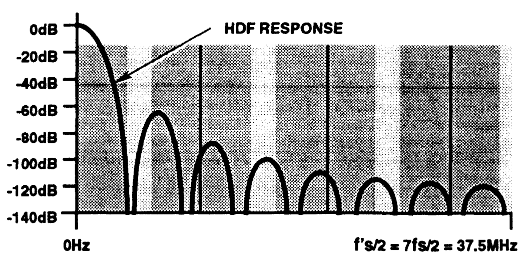

FIGURE 18. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 7 CASE

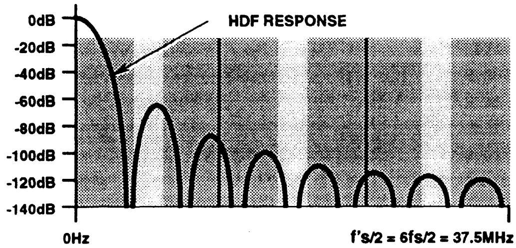

FIGURE 19. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 6 CASE

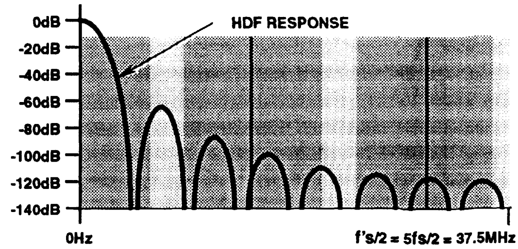

FIGURE 20. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 5 CASE

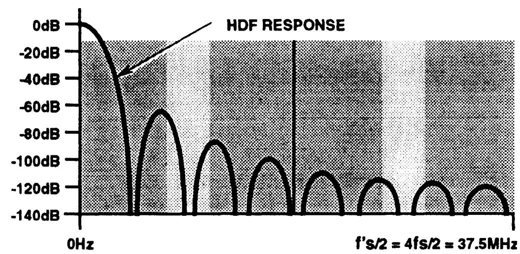

FIGURE 21. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 4 CASE

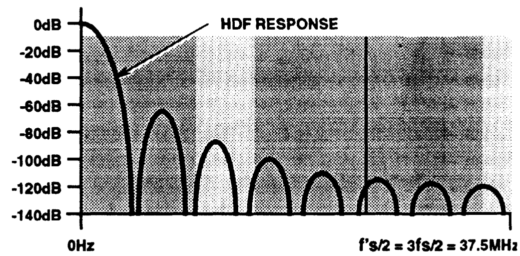

FIGURE 22. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 3 CASE

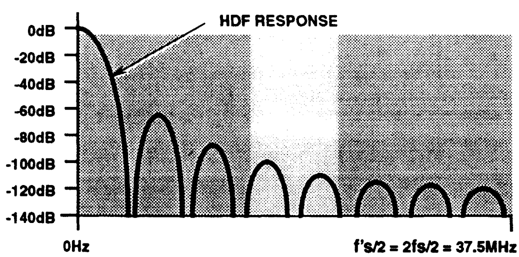

FIGURE 23. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 2 CASE

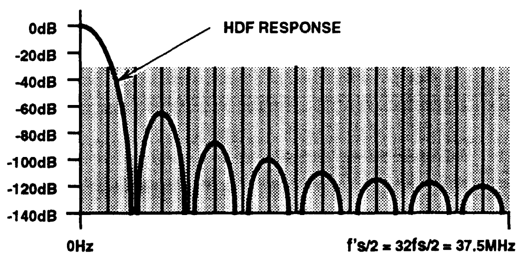

FIGURE 24. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 32 CASE

Center Frequency Calculation

Decreasing the minimum decimation rate of the DDC by interpolation impacts the calculation and resolution of the local oscillator control words with the exception of Phase Offset.

The Phase Generator in the DDC uses a 33 bit phase accumulator to generate an 18 bit phase word which controls the local oscillator [1]. In continuous carrier wave (CW) down convert mode the 32 bit Maximum Phase Increment is used to control the phase step between successive Phase Generator outputs. The Maximum Phase Increment represents phase increments from 0 to $\pi(1\text{-}2^{-32})$ relative to the DDC input sampling rate. When the DDC is proceeded by a sample rate expander the input sample rate is 1/L times the DDC input sample rate. Therefore, the maximum valid phase step relative to the input sample rate is 1/L that of the DDC. Likewise, the frequency resolution is reduced by L.

We now illustrate the afore stated points by way of example.

Assume a 4MSPS input and a desired decimation of 4. The DDC would be clocked at 64MHz and would be preceded by a sample rate expander which up samples by a factor of 16. The HDF decimation rate would be set to 16.

The Maximum Phase Increment can be programmed from 0_H to $FFFFFFFF_H$ representing an LO frequency from DC to just under 32MHz. However, the highest input frequency into

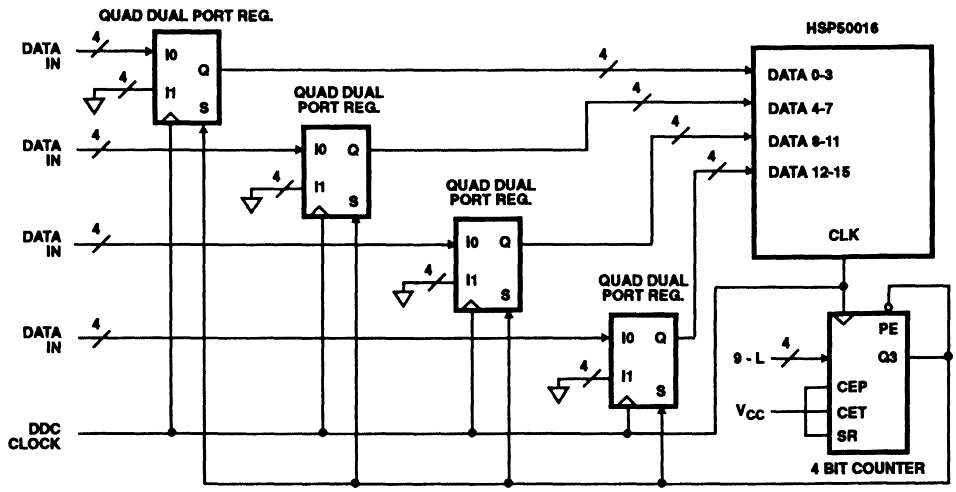

FIGURE 25. AN EXAMPLE SAMPLE RATE EXPANSION CIRCUIT WITH A MAXIMUM EXPANSION OF 8 AND A MAXIMUM CLOCK OF 65MHz

the sample rate expander is 2MHz which is in turn the highest valid LO frequency. This LO frequency corresponds to a Maximum Phase Increment value of $FFFFFFFF_H/16$ or $FFFFFFF_H$.

If the DDC sampling rate were 4 MHZ the frequency resolution would be $4MHz/2^{33}$. Since the DDC sampling rate is 64MHz the frequency resolution is $64MHz/2^{33}$, or 1/Lth that of $4MHz/2^{33}$.

In Chirp mode the Maximum Phase Increment, Minimum Phase Increment, and Delta Phase Increment must also be calculated for the input sample rate relative to the DDC sampling rate.

Example Sample Rate Expander Circuit

Figure 25 shows an example sample rate expander circuit built around a high speed CMOS synchronous counter and four high speed CMOS quad dual port registers.

The synchronous counter is preset with 9 minus L, the desired interpolation rate. The count enable parallel (CEP), count enable trickle (CET), and synchronous reset (SR) inputs are tied high. For L-1 counts of the DDC clock the counter's Q3 output line is low and is used to select the grounded I1 inputs into the quad dual port registers. On the Lth count Q3 goes high, initiating two actions. First it selects the input data on the I0 inputs to the quad dual port registers. Second, it presets the counter. The high rate outputs of the quad dual port registers are connected to the DDC's data inputs. This action results in sample rate expansion by L. This circuit can be used for DDC clock rates up to approximately 65MHz and interpolation rates of up to 8. Additional ANDing logic can be attached to the counter outputs to increase the possible interpolation rates to 16.

Figure 26 shows a similar circuit using two PAL's.

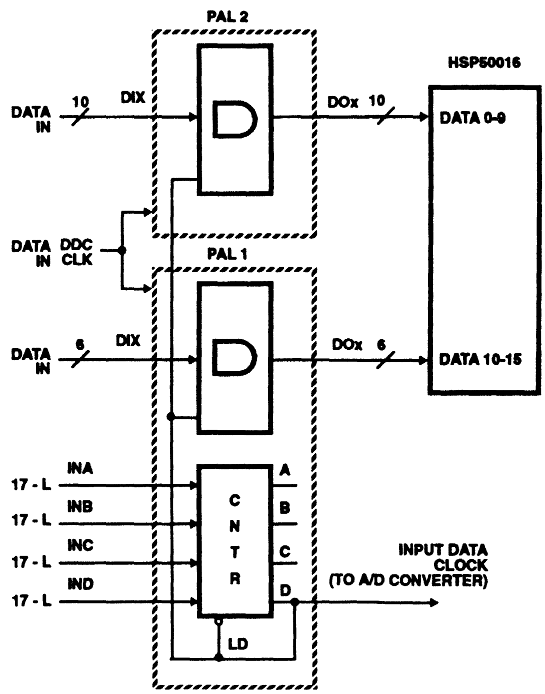

FIGURE 26. AN EXAMPLE SAMPLE RATE EXPANSION CIRCUIT USING TWO PALS WITH A MAXIMUM EXPANSION OF 8 AND A MAXIMUM CLOCK OF 75MHz

The first PAL is configured as a counter and six AND gates with one input of each AND gate tied to a common control line coming from the counter and the other input connected to an input data line. The logical configuration of the first PAL is as follows.

$DOx = DIx \text{ and } \overline{D}$

$A = (D \text{ and } \overline{A}) + (\overline{D} \text{ and } INA)$

$B = (D \text{ and } A \text{ and } \overline{B}) + (\overline{D} \text{ and } INB) + (D \text{ and } \overline{A} \text{ and } B)$

$C = (D \text{ and } A \text{ and } B \text{ and } \overline{C}) + (\overline{D} \text{ and } INC)$

$+ (D \text{ and } \overline{A \text{ and } B} \text{ and } C)$

$D = (\overline{A \text{ and } B \text{ and } C} \text{ and } D) + (\overline{D} \text{ and } IND)$

The other PAL is configured as ten AND gates with one input of each AND gate tied to a common control line coming from the counter via an input line and the other input connected to an input data line. Logically the second PAL is configured as follows.

$DOx = DIx \text{ and } \overline{D}$

All outputs are registered.

The operation of this circuit begins as the counter is preset with a value of 17 minus L, the interpolation factor L can be up to 8. On successive DDC clocks the counter counts up until it rolls over to zero. Until the roll over occurs D is in a high state and thus $\overline{D}$ is in a low state. Since $\overline{D}$ is in a low state all data outputs are in a low state. This stuffs zeros between the low rate data input to the PALs.

When the counter rolls over $\overline{D}$ goes high resulting in two actions. First the input data is passed through the AND gates and into the registered outputs to be passed to the DDC. Second, it reloads the counter to begin the count sequence anew.

This action results in sample rate expansion by L. This circuit can be used for DDC clock rates up to the maximum 75MHz and interpolation rates of up to 8. Additional logic can be incorporated in the counter to increase the possible interpolation rates.

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[3] Hogenauer, E.B., "An Economical Class of Digital Filters for Decimation and Interpolation," IEEE Trans. on ASSP, Vol. ASSP-29, No. 2, pp. 155-162, April 1981.

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EXTENDED DIGITAL FILTER CONFIGURATIONS

Introduction

Harris HSP43891, HSP43881and HSP43481 Digital Filters (DFs) perform high speed sum-of-products operations. These video speed devices operate at 30MHz, offering substantial improvement in processing speed over other available technology. Throughputs in excess of 30MHz are achieved using multiple devices.

The DF data sheet explains how multiple DFs can be easily cascaded to achieve long filters with 8 bit data and coefficients. This note presents extensions of the basic cascaded configuration for:

- Designing Extended Length Filters Using a Single Device (the Number of Taps Exceeds the Number of Cells).
- Implementing Higher Precision (Greater Than 8 or 9 Bits) Full Speed Designs Using Multiple Devices.
- Implementing Higher Precision Designs Using a Single Device.

It is assumed that the reader has a basic knowledge of filter design and some digital hardware experience. Readers who require more detailed information on the electrical characteristics of the DF family devices should refer to the Harris DF engineering data sheets. Harris also provides a comprehensive set of hardware and software development tools.

The Finite Impulse Response Filter

The finite impulse response (FIR) filter is simply a finite-length sum-of-products digital filter. Each output sample is a weighted sum of the new input value and the L-1 previous inputs, where L is the order of the filter. With the tapped delay line architecture (Figure 1) the filter coefficients remain fixed while the input data shifts from cell to cell on each clock cycle.

The DF's architecture (Figure 2) is different from the traditional tapped delay line filter. In the DF the filter coefficients shift from cell to cell with each clock cycle. As each new data sample becomes available it is distributed to all of the cells at the same time. In addition, every DF cell contains its own multiplier and accumulator. This allows each cell to maintain an independent sum-of-products in its accumulator. A new output value becomes available on each clock cycle by properly sequencing the filter coefficients through the cells.

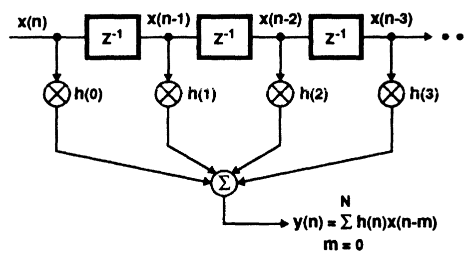


FIGURE 1. DIRECT FORM REPRESENTATION OF FIR FILTER

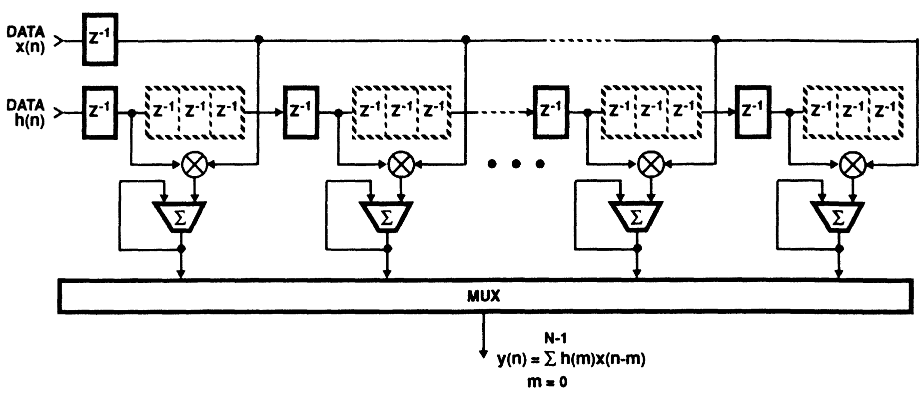


FIGURE 2. DF CELL DIAGRAM

Each cell's accumulator is cleared after its contents are output. This allows accumulation of the next sum-of-products to begin. Note that the filter coefficients enter from the left, shifting one cell to the right with each clock cycle.

A *single* device may be used to implement filters with a large number of coefficients. In this case the number of filter taps will exceed the number of DF cells. This requires manipulating the input data and filter coefficient sequences, maintaining the proper sum-of-products in each cell's accumulator. This implementation is described in greater detail in the following section.

Eight Tap Filter With a Four Cell Device

A simple example is the best way to demonstrate how data and coefficients are properly sequenced. Table 1 illustrates the situation when an eight tap filter is computed in a single 4 cell HSP43481. The table lists information in six columns. The first column shows the initial 21 clock cycles, which is enough to evaluate the example. The next four columns represent the actions taking place in each of the four DF cells as a function of the clock. The final column shows the output results, also a function of the clock.

Within the filter cell are internal pipeline delays. The result is a startup delay of three CLKs before the data and coefficients present at the input of the DF are processed and stored in the accumulator of the first cell. This delay is not relevant to the sequential operation of the DF and will be ignored in subsequent discussions (also ignored in Table 1).

The basic computational sequence is shown below:

CLK 0 - Initial data point X_0 is made available to all four cells. At the same time coefficient C_7 enters Cell 0.

- The First Product (C_7 x X_0) is Computed and Stored in Accumulator of Cell 0.

CLK 1 - X_1 is made available to all four cells. At the same time coefficient C_6 enters Cell 0, shifting C_7 to Cell 1.

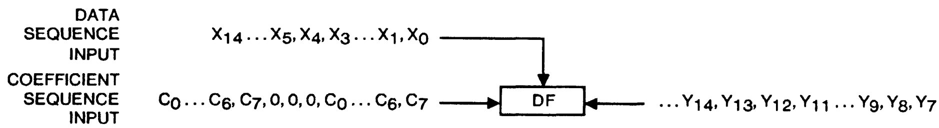
- The Accumulator of Cell 0 is Updated With the Additional Term C_6 x X_1.
- The Product C_7 x X_1 is Computed and Stored in Accumulator of Cell 1.

CLK 2 - X_2 is made available to all four cells. At the same time coefficient C_5 enters Cell 0, shifting C_7 to Cell 2 and C_6 to Cell 1.

- The Accumulator of Cell 0 is Updated With the Additional Term C_5 x X_2.
- The Accumulator of Cell 1 is Updated With the Additional Term C_6 x X_2.
- The Product C_7 x X_2 is Computed and Stored in Accumulator of Cell 2.

•
•
•
etc.

TABLE 1. HSP43481 8 TAP FIR FILTER SEQUENCE USING SINGLE 4 CELL DEVICE



CLK	CELL 0	CELL 1	CELL 2	CELL 3	SUM/CLR
0	$C_7 \times X_0$	0	0	0	-
1	$+C_6 \times X_1$	$C_7 \times X_1$	0	0	-
2	$+C_5 \times X_2$	$+C_6 \times X_2$	$C_7 \times X_2$	0	-
3	$+C_4 \times X_3$	$+C_5 \times X_3$	$+C_6 \times X_3$	$C_7 \times X_3$	-
4	$+C_3 \times X_4$	$+C_4 \times X_4$	$+C_5 \times X_4$	$+C_6 \times X_4$	-
5	$+C_2 \times X_5$	$+C_3 \times X_5$	$+C_4 \times X_5$	$+C_5 \times X_5$	-
6	$+C_1 \times X_6$	$+C_2 \times X_6$	$+C_3 \times X_6$	$+C_4 \times X_6$	-
7	$+C_0 \times X_7$	$+C_1 \times X_7$	$+C_2 \times X_7$	$+C_3 \times X_7$	Cell 0 (Y_7)
8	0	$+C_0 \times X_8$	$+C_1 \times X_8$	$+C_2 \times X_8$	Cell 1 (Y_8)
9	0	0	$+C_0 \times X_9$	$+C_1 \times X_9$	Cell 2 (Y_9)
10	0	0	0	$+C_0 \times X_{10}$	Cell 3 (Y_{10})
11	$C_7 \times X_4$	0	0	0	-
12	$+C_6 \times X_5$	$C_7 \times X_5$	0	0	-
13	$+C_5 \times X_6$	$+C_6 \times X_6$	$C_7 \times X_6$	0	-
14	$+C_4 \times X_7$	$+C_5 \times X_7$	$+C_6 \times X_7$	$C_7 \times X_7$	-
15	$+C_3 \times X_8$	$+C_4 \times X_8$	$+C_5 \times X_8$	$+C_6 \times X_8$	-
16	$+C_2 \times X_9$	$+C_3 \times X_9$	$+C_4 \times X_9$	$+C_5 \times X_9$	-
17	$+C_1 \times X_{10}$	$+C_2 \times X_{10}$	$+C_3 \times X_{10}$	$+C_4 \times X_{10}$	-
18	$+C_0 \times X_{11}$	$+C_1 \times X_{11}$	$+C_2 \times X_{11}$	$+C_3 \times X_{11}$	Cell 0 (Y_{11})
19	0	$+C_0 \times X_{12}$	$+C_1 \times X_{12}$	$+C_2 \times X_{12}$	Cell 1 (Y_{12})
20	0	0	$+C_0 \times X_{13}$	$+C_1 \times X_{13}$	Cell 2 (Y_{13})
21	0	0	0	$+C_0 \times X_{14}$	Cell 3 (Y_{14})

This process continues until eight taps have been computed and accumulated in each cell. This happens first in Cell 0, followed one CLK later by Cell 1, two CLKs later by Cell 2, and three CLKs later by Cell 3. Output points become available after each cell accumulates the sum of eight taps in the order given above.

After Cell 3's output becomes available, we are ready to begin work on the next four output points. We can cycle the eight filter coefficients in the same fashion as before but the input data is out of sequence. Before computing the fifth output point the DF requires X_4 to be available at the data input. Since X_4 passed by seven CLKs ago (during CLK 4) some method of storing the previous seven data points is necessary.

In order to access the previous seven data values they must have been originally stored in some form of sequential memory. FIFOs work very well and will be discussed in the next section. Starting with CLK 11 the taps once more begin to accumulate in each of the four cells.

The result of re-accessing data after every four output points is to lower the effective throughput. The output rate drops about fifty percent to a rate of four output points for every eleven CLKs.

L Tap Filter With an N Cell Device Where L>N

The example above leads to the more general case of implementing an L tap filter with an N cell device (L>N). When an L tap filter is implemented using an N cell DF (where L>N), the DF computes a block of N filter output samples at a time. Between these output blocks there are L-1 CLK cycles during which no valid output points are available. Therefore, generating a block of N output points requires L+N-1 CLKs. During these L+N-1 CLKs there are L+N-1 new input samples being clocked into the DIN (Data IN) port.

It can be seen from Table 1 that N outputs are read out of the DF during the last N CLKs of each L+N-1 CLK sequence. After inputting the first L data samples N-1 CLKs are required to flush the coefficients from the cells. The final L-1 of the previous L+N-1 input samples must be re-submitted at the input port. After the outputs are read out an additional L+N-1 samples are fed in and the process repeats itself until no more data is available.

In this paper, throughput is defined as the average rate at which outputs are computed by the DF. When the number of taps exceeds the number of filter cells, the necessity to re-access the data stream determines the maximum throughput. The generalized performance of an L tap, 8x8 FIR filter is shown below. Let:

L = Number of taps

N = Number of filter cells in DF

R = Maximum clock rate of DF (20, 25.6, or 30MHz)

F_S = Desired throughput (MHz) where $R>F_S$

If L, N, and R are known then:

$F_S = N \times R/(L+N-1)$

If L, R, and F_S are known then:

$N = F_S (L-1)/(R-F_S)$

Since there are either four (HSP43481) or eight (HSP43881) cells in each DF, the required number of DFs can be computed as:

# of 4 cell DFs = N/4 (round up to next integer value)

# of 8 cell DFs = N/8 (round up to next integer value)

An example design with L = 128 taps, F_S = 5MHz, and R = 20MHz would yield:

N = 5 x 127/15 = 43 cells

# of 4 cell DFs = 43/4 = 11

# of 8 cell DFs = 43/8 = 6

Optimum arrangement = 40/8 + 3/4 = Five 8 cell and one 4 cell DFs.

The sequencing of the input data can be realized in various ways, with the simplest design using FIFOs. Figure 3 shows the block diagram of a design using an eight cell DF. The input data buffered in two FIFOs (each must have three-state outputs).

An 8 bit counter is configured to count modulo L+N-1. To initialize the system, the first L-1 data samples are passed through FIFO #1 and written into FIFO #2. While this occurs N more samples are clocked into FIFO #1. Following that a repetitive steady state sequence begins as shown below:

1. Clock the first L-1 samples from FIFO #2 into the DF.
2. Clock N samples from FIFO #1 into the DF.
3. Clock the last L-1 samples of the sequence in steps 1 and 2 back into FIFO #2.
4. Clock the next N samples into FIFO #1 concurrently with steps 1-3.

This sequence of steps 1 through 4 can be repeated ad infinitum.

The output data is available in blocks of N points separated by L-1 CLK cycles. FIFO #3 acts as a rate buffer for the output and is optional. The coefficient memory contains the L coefficients followed by the necessary N-1 zeros.

A design example using the above technique might include a 57 tap filter with a sample rate of 2.5MHz. This can be done with a single 8 cell device operating at 20MHz.

Higher Precision Filters and Correlators

Several digital filtering applications require wider wordwidth calculations to maintain precision. The DFs are designed to be flexible in creating filters with input precision levels of 8, 16, 24, 32 bits or greater.

The first step is to restructure the data and/or coefficients into 8 bit quantities which can be processed by the DF.

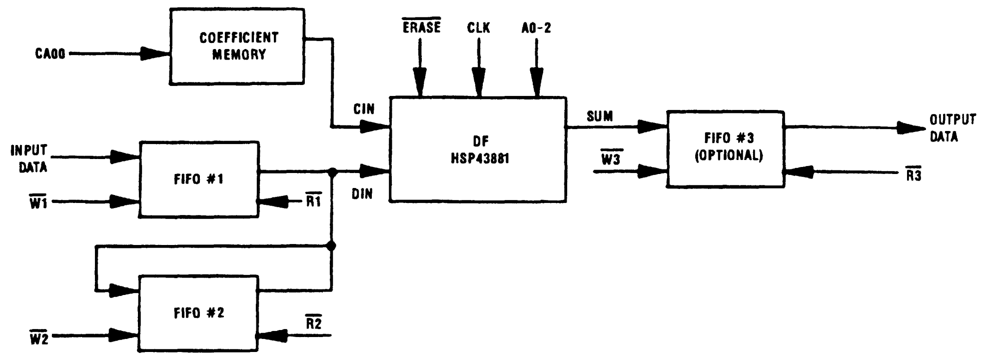


FIGURE 3. BLOCK DIAGRAM OF AN 8 CELL DF CONFIGURED TO IMPLEMENT EXTENDED FILTER LENGTHS (UP TO 249 TAPS)

These quantities are used to form the partial products of the larger multiplication involving the full precision data and coefficients. An example of segmenting the partial products of a 16x8 multiplication (16 bit coefficients and 8 bit data) would be:

$C(16\text{ bit}) = C_H \times 2^8 + C_L \times 2^0$ H = High Order Byte

$X(8\text{ bit}) = X \times 2^0$ L = Low Order Byte

Consequently,

$$C \times X = (C_H \times 2^8 + C_L \times 2^0)X \times 2^0$$
$$= C_HX \times 2^8 + C_LX \times 2^0$$

The process of convolution or correlation requires repeated multiply and accumulate operations. The resulting *partial* output word widths are a function of the number of MAC operations and of the coefficient scaling. Although each partial product is only 16 bits wide, the *sum* of the partial products in the output stage is allowed to accumulate up to a maximum width of 26 bits.

Care must be taken when combining the upper and lower partial sums-of-products into each complete output result. Figure 5 illustrates how the upper and lower sums of partial products for each output point must be re-combined. Sign extension must be used if more than 26 bits are required from the output stage representing the least significant sum of partial products.

Two separate techniques can be used in determining higher precision results:

1. Use separate DFs, combining the two partial products using external adders.
   - Throughput equals the clock rate of the DF.
2. Accumulate the two partial products in separate cells of a single DF.
   - The SHADD (SHift and ADD) feature of the output adder allows the data to be properly aligned and combined.
   - Throughput is determined by the number of taps, partial products, and DF cells, as well as the clock rate of the DF.

The equations describing the filtering operation are the same for either technique and can be given as:

$$y(n) = \sum_{i=0}^{N-1} C(i)X(n-i)$$

However: $(C_H \times 2^8 + C_L)X = C_HX \times 2^8 + C_LX$

Therefore: $$y(n) = \sum_{i=0}^{N-1} C_H(i)X(n-i) \times 2^8 + \sum_{i=0}^{N-1} C_L(i)X(n-1)$$

Assuming the coefficients are represented as two's complement numbers, the least significant byte has to be treated as a positive (unsigned) number. The TCCI input of the DF is used to take care of this.

Word-Size Extension at Full Speed

Full performance filters with extended precision data and/or coefficients are easily designed. This is achieved by computing the partial products in *separate* DFs and combining their results with external adders. When external adders are used the system performance is limited only by the throughput of the DF itself.

The filter equations listed directly above can be expanded into their partial products and grouped for processing. An expansion of the first four output points resulting from the convolution of 16 bit coefficient and 8 bit data is shown in Table 2.

In this case, for a 4 tap filter, each device accumulates four partial products at once, one in each cell. The output adder combines these partial products into the proper result. The sequence table (Table 2) shows the results of the multiply accumulate operations for one device (DF0).

Figure 4 is a block diagram that directly implements the grouping given above. DF0 is generating the C_LX partial products while DF1 is generating the partial products for C_HX. The two 8x8 partial products are generated in separate DFs and combined with an external adder. Notice that the lower and upper coefficients bytes are separated and used to supply different DFs. Using this design the throughput is limited only by the DF (up to 30MHz).

The adder stage of Figure 4 merits further discussion. Each 4 cell DF has 26 output lines (SUM0-25). Therefore, if all the available bits were preserved we would have a 34 bit sum as shown in Figure 5. However, many designs require only 16 output bits. Which 16 bits are selected depends on the coefficient scaling and the input signal level.

TABLE 2. HSP43481 4 TAP SINGLE PARTIAL PRODUCT FIR FILTER

$$\begin{aligned} y(0) = {} & C_H(0)X(0) \times 2^8 + C_L(0)X(0) \\ & + C_H(1)X(1) \times 2^8 + C_L(1)X(1) \\ & + C_H(2)X(2) \times 2^8 + C_L(2)X(2) \\ & + C_H(3)X(3) \times 2^8 + C_L(3)X(3) \end{aligned}$$

DF1 Cell 0 | DF0 Cell 0

$$\begin{aligned} y(1) = {} & C_H(0)X(1) \times 2^8 + C_L(0)X(1) \\ & + C_H(1)X(2) \times 2^8 + C_L(1)X(2) \\ & + C_H(2)X(3) \times 2^8 + C_L(2)X(3) \\ & + C_H(3)X(4) \times 2^8 + C_L(3)X(4) \end{aligned}$$

DF1 Cell 1 | DF0 Cell 1

$$\begin{aligned} y(2) = {} & C_H(0)X(2) \times 2^8 + C_L(0)X(2) \\ & + C_H(1)X(3) \times 2^8 + C_L(1)X(3) \\ & + C_H(2)X(4) \times 2^8 + C_L(2)X(4) \\ & + C_H(3)X(5) \times 2^8 + C_L(3)X(5) \end{aligned}$$

DF1 Cell 2 | DF0 Cell 2

$$\begin{aligned} y(3) = {} & C_H(0)X(3) \times 2^8 + C_L(0)X(3) \\ & + C_H(1)X(4) \times 2^8 + C_L(1)X(4) \\ & + C_H(2)X(5) \times 2^8 + C_L(2)X(5) \\ & + C_H(3)X(6) \times 2^8 + C_L(3)X(6) \end{aligned}$$

DF1 Cell 3 | DF0 Cell 3

•
•
etc.

CLK	CELL 0	CELL 1	CELL 2	CELL 3	OUTPUT
0	$C_{L3} \times X_{L0}$	0	0	0	
1	$+C_{L2} \times X_{L1}$	$C_{L3} \times X_{L1}$	0	0	
2	$+C_{L1} \times X_{L2}$	$+C_{L2} \times X_{L2}$	$C_{L3} \times X_{L3}$	0	
3	$+C_{L0} \times X_{L3}$	$+C_{L1} \times X_{L3}$	$+C_{L2} \times X_{L3}$	$C_{L3} \times X_{L3}$	Cell 0 (Y_L3)
4	$C_{L3} \times X_{L4}$	$+C_{L0} \times X_{L4}$	$+C_{L1} \times X_{L4}$	$+C_{L2} \times X_{L4}$	Cell 0 (Y_L4)
5	$+C_{L2} \times X_{L5}$	$C_{L3} \times X_{L5}$	$+C_{L0} \times X_{L5}$	$+C_{L1} \times X_{L5}$	Cell 0 (Y_L5)
6	$+C_{L1} \times X_{L6}$	$+C_{L2} \times X_{L6}$	$C_{L3} \times X_{L6}$	$+C_{L0} \times X_{L6}$	Cell 0 (Y_L6)
7	$+C_{L0} \times X_{L7}$	$+C_{L1} \times X_{L7}$	$+C_{L2} \times X_{L7}$	$C_{L3} \times X_{L7}$	Cell 0 (Y_L7)

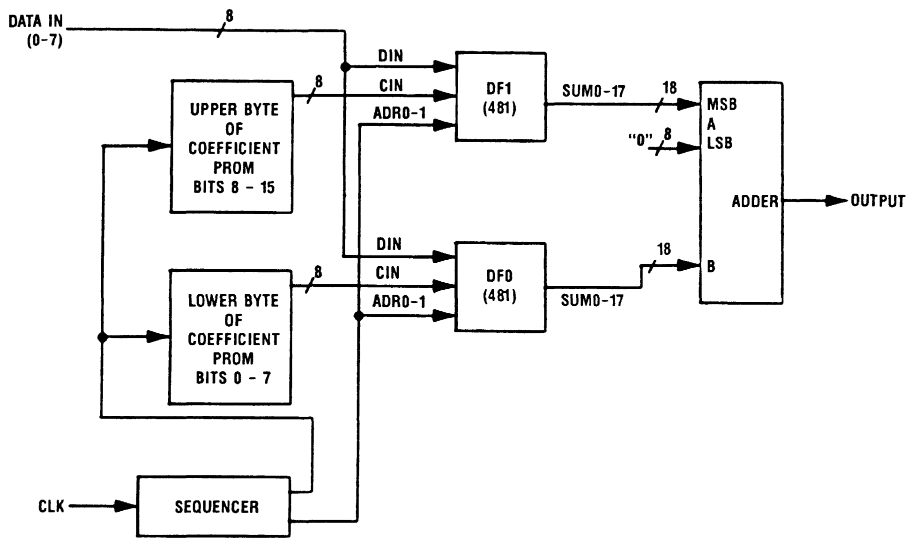


FIGURE 4. BLOCK DIAGRAM OF A 30MHz, 4 TAP, 16x8 FIR FILTER

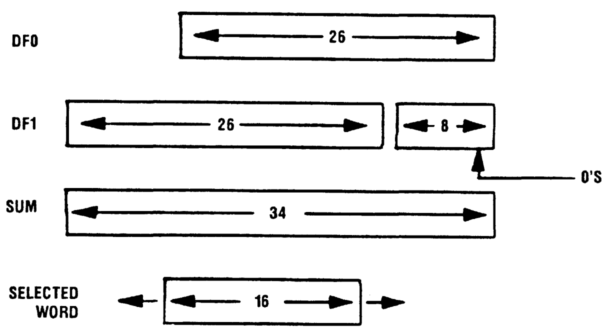


FIGURE 5. IDEAL OUTPUT STAGE ADDER

The results for the 16x8 example can be extended to the general case of more than four taps. Let:

L = Number of taps

N = Total number of filter cells required

R = Maximum clock rate of DF (20, 25.6, or 30MHz)

F_S = Desired throughput (MHz)

For a full speed (F_S = R) 16x8 design: N = 2L

There are either four (HSP43481) or eight (HSP43881) cells in each DF. Therefore, the number of DFs can be computed as:

# of 4 cell DFs = 2 x [L/4 (rounded up to next integer value)]

# of 8 cell DFs = 2 x [L/8 (rounded up to next integer value)]

An example design with L=15 taps and F_S = R = 25MHz would yield:

# of 4 cell DFs = 2 x [15/4] = 8

# of 8 cell DFs = 2 x [15/8] = 4

Word-Size Extension Using One Device

The second technique for extending the word width accumulates the partial products in separate cells of a *single* device. An expansion of the first four output points resulting from the convolution of 16 bit coefficient and 8 bit data is shown below.

The groupings are the same as in the earlier case using multiple DFs. However, in this case individual cells within *one* DF are responsible for generating the partial products. This method of processing eliminates the need for an external adder in exchange for lower throughput.

The sequence table (Table 3) shows the results of the multiply accumulate operation for the separate cells of a 4 tap 16x8 FIR filter. Cells 1 and 3 accumulate the partial products C_HX. Cells 0 and 2 accumulate the partial products C_LX.

After computing and outputting the first result Cell 0 is ready to accumulate the next partial products. At this point (CLK 11) Cell 0 needs to re-access X_2, which was last available during CLK 5. In order to accomplish this a temporary storage, sequential memory (such as a FIFO) is necessary. The design of Figure 6 shows such a FIFO based design.

$$\begin{aligned} y(0) = {} & C_H(0)X(0) \times 2^8 + C_L(0)X(0) \\ & + C_H(1)X(1) \times 2^8 + C_L(1)X(1) \\ & C_H(2)X(2) \times 2^8 + C_L(2)X(2) \\ & + C_H(3)X(3) \times 2^8 + C_L(3)X(3) \\ & \underbrace{\qquad\qquad\qquad}_{\text{Cell 1}} \underbrace{\qquad\qquad}_{\text{Cell 0}} \end{aligned}$$

$$\begin{aligned} y(1) = {} & C_H(0)X(1) \times 2^8 + C_L(0)X(1) \\ & + C_H(1)X(2) \times 2^8 + C_L(1)X(2) \\ & + C_H(2)X(3) \times 2^8 + C_L(2)X(3) \\ & + C_H(3)X(4) \times 2^8 + C_L(3)X(4) \\ & \underbrace{\qquad\qquad\qquad}_{\text{Cell 3}} \underbrace{\qquad\qquad}_{\text{Cell 2}} \end{aligned}$$

$$\begin{aligned} y(2) = {} & C_H(0)X(2) \times 2^8 + C_L(0)X(2) \\ & + C_H(1)X(3) \times 2^8 + C_L(1)X(3) \\ & + C_H(2)X(4) \times 2^8 + C_L(2)X(4) \\ & + C_H(3)X(5) \times 2^8 + C_L(3)X(5) \\ & \underbrace{\qquad\qquad\qquad}_{\text{Cell 1}} \underbrace{\qquad\qquad}_{\text{Cell 0}} \end{aligned}$$

$$\begin{aligned} y(3) = {} & C_H(0)X(3) \times 2^8 + C_L(0)X(3) \\ & + C_H(1)X(4) \times 2^8 + C_L(1)X(4) \\ & + C_H(2)X(5) \times 2^8 + C_L(2)X(5) \\ & + C_H(3)X(6) \times 2^8 + C_L(3)X(6) \\ & \underbrace{\qquad\qquad\qquad}_{\text{Cell 3}} \underbrace{\qquad\qquad}_{\text{Cell 2}} \end{aligned}$$

TABLE 3. HSP43481 4 TAP, 16x8 FIR FILTER SEQUENCE

INPUT DATA SEQUENCE $X_8, \ldots, X_4, X_6, \ldots, X_2, X_4, X_3, X_2, X_1, X_0$ → DF ($\overline{DIENB}$)

COEFFICIENT SEQUENCE $C_{L3}, C_{H3}, 0, 0, C_{L0}, C_{H0}, C_{L1}, C_{H1}, C_{L2}, C_{H2}, C_{L3}, C_{H3}$ → DF → Y(5) . . . Y(4) . . . Y(3)

CLK	CELL 0	CELL 1	CELL 2	CELL 3	OUTPUT
0	$C_{H3} \times 0$	-	-	-	-
1	$C_{L3} \times X_0$	$C_{H3} \times X_0$	-	-	-
2	$C_{H2} \times 0$	$C_{L3} \times 0$	$C_{H3} \times 0$	-	-
3	$+C_{L2} \times X_1$	$+C_{H2} \times X_1$	$C_{L3} \times X_1$	$C_{H3} \times X_1$	-
4	$C_{H1} \times 0$	$C_{L2} \times 0$	$C_{H2} \times 0$	$C_{L3} \times 0$	-
5	$+C_{L1} \times X_2$	$+C_{H1} \times X_2$	$+C_{L2} \times X_2$	$+C_{H2} \times X_2$	-
6	$C_{H0} \times 0$	$C_{L1} \times 0$	$C_{H1} \times 0$	$C_{L2} \times 0$	-
7	$+C_{L0} \times X_3$	$+C_{H0} \times X_3$	$+C_{L1} \times X_3$	$+C_{H1} \times X_3$	$Y_L(3)$
8	0×0	$C_{L0} \times 0$	$C_{H0} \times 0$	$C_{L1} \times 0$	-
9	$0 \times X_4$	$0 \times X_4$	$+C_{L0} \times X_4$	$+C_{H0} \times X_4$	$Y_H(3)$
10	$C_{H3} \times 0$	0×0	0×0	$C_{L0} \times 0$	-
11	$C_{L3} \times X_2$	$C_{H3} \times X_2$	$0 \times X_2$	$0 \times X_2$	$Y_L(4)$
12	$C_{H2} \times 0$	$C_{L3} \times 0$	$C_{H3} \times 0$	0×0	-
13	$+C_{L2} \times X_3$	$+C_{H2} \times X_3$	$C_{L3} \times X_3$	$C_{H3} \times X_3$	$Y_H(4)$
14	$C_{H1} \times 0$	$C_{L2} \times 0$	$C_{H2} \times 0$	$C_{L3} \times 0$	-
15	$+C_{L1} \times X_4$	$+C_{H1} \times X_4$	$+C_{L2} \times X_4$	$+C_{H2} \times X_4$	-
16	$C_{H0} \times 0$	$C_{L1} \times 0$	$C_{H1} \times 0$	$C_{L2} \times 0$	-
17	$+C_{L0} \times X_5$	$+C_{H0} \times X_5$	$+C_{L1} \times X_5$	$+C_{H1} \times X_5$	$Y_L(5)$
18	0×0	$C_{L0} \times 0$	$C_{H0} \times 0$	$C_{L1} \times 0$	-
19	$0 \times X_6$	$0 \times X_6$	$+C_{L0} \times X_6$	$+C_{H0} \times X_6$	$Y_H(5)$
20	$C_{H3} \times 0$	0×0	0×0	$C_{L0} \times 0$	-
21	$C_{L3} \times X_4$	$C_{H3} \times X_4$	$0 \times X_4$	$0 \times X_4$	$Y_L(6)$
22	$C_{H2} \times 0$	$C_{L3} \times 0$	$C_{H3} \times 0$	0×0	-
23	$+C_{L2} \times X_5$	$+C_{H2} \times X_5$	$C_{L3} \times X_5$	$C_{H3} \times X_5$	$Y_H(6)$
24	$C_{H1} \times 0$	$C_{L2} \times 0$	$C_{H2} \times 0$	$C_{L3} \times 0$	-
25	$+C_{L1} \times X_6$	$+C_{H1} \times X_6$	$+C_{L2} \times X_6$	$+C_{H2} \times X_6$	-

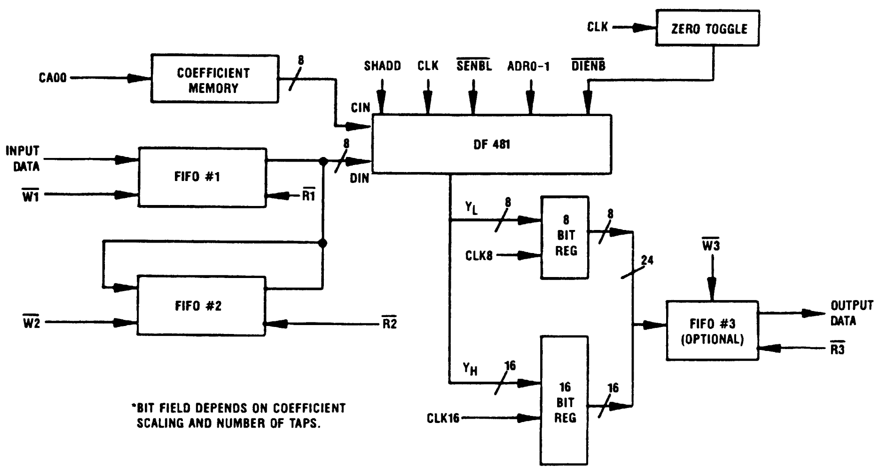


FIGURE 6. 16x8 4 TAP FIR FILTER BLOCK DIAGRAM

In order to interlace the necessary zeros between data samples we must toggle the DIENB control line. This line is driven low when passing a valid data sample to the X register and set high when loading the X register with zero. The sequencing of the input data through the FIFOs is similar to the example given in Figure 3.

The output stage (Figure 7) plays a key role in determining the final results. In the output stage there are several control signals. The most important signals controlling the output stage are SHADD (SHift and ADD), ADR0-1 (cell AdDRess), SENBL (Sum0-15 ENaBled), and SENBH (Sum16-25 ENaBled). SENBL and SENBH are always asserted in this example, enabling the three-state output buffer and allowing the external register to clock in data at the proper time. SHADD and ADR0-1 are used to control the flow of data through the output stage.

The contents of a selected cell (ADR0-1) are routed to two separate locations within the output stage; the 26 bit adder and the output mux. From the output mux the 26 bit cell contents are available to the outside world as either the 16 LSBs (SENBL), 10 MSBs (SENBH), or all 26 bits (SENBL+SENBH).

The 26 bit adder feeding the output buffer has two possible inputs. The first input represents the contents of the selected cell. The zero mux determines whether the other input to the adder is zero or the 18 MSBs of the output buffer. A high on the SHADD input selects the 18 MSBs of the output buffer and a low on the SHADD input selects zero. The results from the adder are immediately stored in the output buffer.

Data reaches the three-state buffer by one of two separate paths. The first path routes the data directly from the cell result multiplexer through the output multiplexer and onto the output bus. The second path is from the cell result multiplexer, through the adder, and finally onto the output bus. Both of these routes will be used in order to create the final result from the partial products.

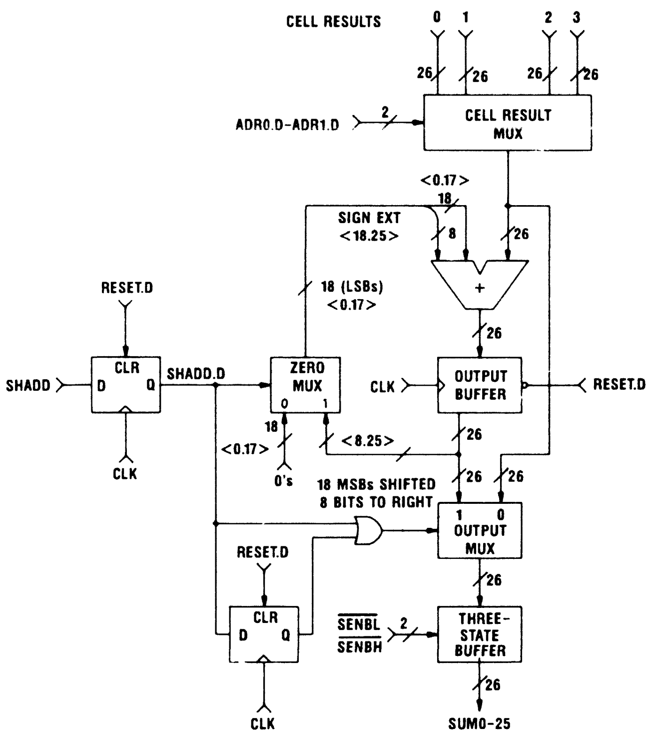


FIGURE 7. DF OUTPUT STAGE

After the partial products are made available to the output bus they are stored in temporary registers. This allows the two sections of the final result to be combined properly. Following this the full result may be stored directly into some form of memory. Figure 6 shows a block diagram illustrating the complete concept.

The following summary describes the sequence of events listed in Table 3 (also refer to Figures 6 and 7).

CLK 0-5
- Each Cell Is Accumulating Partial Product Data
- SHADD Not Asserted

CLK 6
- Cell 0 Selected (ADR0-1 = 0)
- Erase Accumulator of Cell 0 ($\overline{\text{ERASE}}$ = 0)
- SHADD Not Asserted

CLK 7
- Cell 0 Contents Added to Zero and Available at Input to Output Buffer
- Cell 0 Contents Available at SUM0-15
- Cell 1 Selected (ADR0-1 = 1)
- Erase Accumulator of Cell 1 ($\overline{\text{ERASE}}$ = 0)
- SHADD Not Asserted

CLK 8
- External 8 Bit Register Clock Asserted. Lower 8 Bits of SUM0-15 (Least Significant Byte of Y(3)) Entered Into External 8 Bit Register
- Cell 0 Contents Entered Into Output Buffer
- Cell 1 Contents Added to Zero and Available at Input to Output Buffer
- SHADD Asserted

CLK 9
- Shift Cell 0 Contents Down 8 Bits and Add to Contents of Cell 1 (Output Buffer). This 16 Bit Value Becomes Available at SUM0-15
- SHADD Not Asserted

CLK 10
- External 16 Bit Register Clock Asserted. All 16 Bits of SUM0-15 (Most Significant Word of Y(3)) Entered Into External 16 Bit Register
- Cell 2 Selected (ADR0-1 = 2)
- Erase Accumulator of Cell 2 ($\overline{\text{ERASE}}$ = 0)
- SHADD Not Asserted

CLK 11
- Cell 2 Contents Added to Zero and Available at Input to Output Buffer
- Cell 2 Contents Available at SUM0-15
- Cell 3 Selected (ADR0-1 = 3)
- Erase Accumulator of Cell 3 ($\overline{\text{ERASE}}$ = 0)
- Write Y(3) Into Output FIFO (Optional)
- SHADD Not Asserted

CLK 12
- External 8 Bit Register Clock Asserted. Lower 8 Bits of SUM0-15 (Least Significant Byte of Y(4)) Entered Into External 8 Bit Register
- Cell 2 Contents Entered Into Output Buffer
- Cell 3 Contents Added to Zero and Available at Input to Output Buffer
- SHADD Asserted

CLK 13
- Shift Cell 2 Contents Down 8 Bits and Add to Contents of Cell 3 (Output Buffer). This 16 Bit Value Becomes Available at SUM0-15
- SHADD Not Asserted

CLK 14
- External 16 Bit Register Clock Asserted. All 16 Bits of SUM0-15 (Most Significant Word of Y(4)) Entered Into External 16 Bit Register
- SHADD Not Asserted

This same pattern repeats until the input data is exhausted. Note that the value stored in the External Register must be stored elsewhere before the low byte of the next output value is sequenced.

The performance specifications for the 16x8 filter are listed below.

- 2 Outputs/10 CLKS = 1 Output/5.0 CLKS
  = 200ns/Output (25.6MHz Device)
  = 5MHz Throughput (25.6MHz Device)

The results for the 16x8 design used in this implementation can be extended to the general case. Let:

L = Number of taps

F_S = Sample rate (MHz)

N2 = Number of 2 cell groups

R = Maximum clock rate of DF (20, 25.6, or 30MHz)

($R > F_S$)

Then: $F_S = (N2 \times R)/(2L+2(N2-1))$

$N2 = 2F_S(L-1)/R-2F_S)$

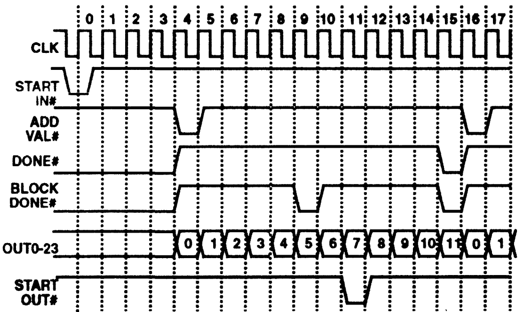
No. AN9205 January 1994

Harris Digital Signal Processing

TIMING RELATIONSHIPS FOR HSP45240

Author: Mike Petrowski

The timing diagram in Figure 1 shows the timing relationship between the various output signals of the HSP45240 when the sequence generator is programmed for **One-Shot Mode with Restart** (see Sequence Generator Section of Datasheet). In this example, the HSP45240 is configured to generate a sequence consisting of two address blocks. Each block is 6 addresses long, and the end of a block is denoted by the assertion of BLOCKDONE#. As the final address in the second block is generated, both DONE# and BLOCK-DONE# are asserted to signal the end of the address sequence. On the next clock, a new address sequence is started (see assertion of ADDVAL#) because the Sequencer was configured to restart. In this mode the STARTOUT# signal is asserted prior to the end of the address sequence for the synchronization of multiple HSP45240's.



NOTE: Asserting STARTIN# after an addressing sequence has been started will cause the sequencer to restart from the beginning of the sequence.

FIGURE 1. SIGNAL RELATIONSHIPS FOR ONE-SHOT MODE WITH RESTART

The timing diagram in Figure 2 shows the timing relationship between the various output signals of the HSP45240 when the sequence generator is programmed for **One-Shot Mode without Restart** (see Sequence Generator Section of Datasheet). As in the above example, the HSP45240 is configured to generate a sequence consisting of two address blocks. Each block is 6 addresses long, and the end of a block is denoted by the assertion of BLOCKDONE#. As the final address in the second block is generated, both DONE# and BLOCKDONE# are asserted and addressing is halted.

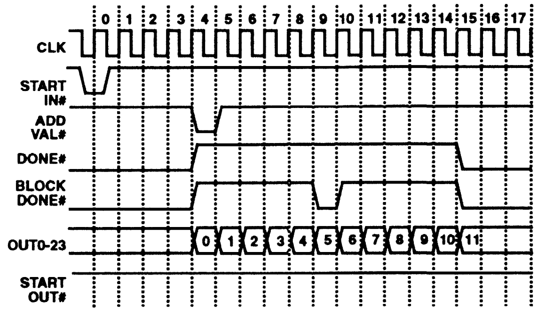


FIGURE 2. SIGNAL RELATIONSHIPS FOR ONE-SHOT MODE WITHOUT RESTART

The timing diagram in Figure 3 shows the timing relationship between the various output signals of the HSP45240 when the sequence generator is internally started by writing the Sequencer "START" address (see Table 1 of Datasheet). The output signals are shown with respect to the rising edge of WR# responsible for the internal START. The address generation parameters are as above.

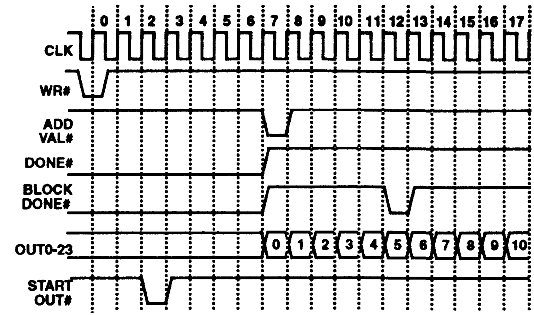


FIGURE 3. SIGNAL RELATIONSHIPS FOR INTERNALLY GENERATED START

DLYBLK Operation

Address generation can be halted by assertion of DLYBLK prior to the completion of an address block (Figure 4 & 5). Addressing will resume once DLYBLK is de-asserted. Since there is a pipeline delay between the assertion of DLYBLK at the pin and when it is internally active, DLYBLK must be asserted prior to the end of an address block. The pipeline delay associated with DLYBLK differs for halting address generation in mid-sequence and halting address generation after the final address block of a sequence.

For halting address generation in mid-sequence, DLYBLK must be asserted 3 clocks prior to the end of the addressing block as shown in Figure 4. In this example, DLYBLK is asserted for one clock cycle which delays the generation of the next address block by one clock. If addressing has been halted in mid-sequence, addressing will resume 4 clocks after de-asserting DLYBLK. Note: BLOCKDONE# will be asserted and OUT0-23 will be held until addressing resumes.

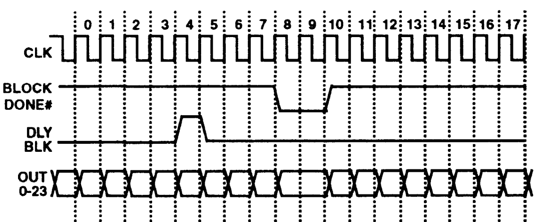


FIGURE 4. SIGNAL RELATIONSHIPS FOR A ONE CYCLE BLOCK DELAY IN MID-SEQUENCE

For halting address generation after the final block of addresses in a sequence, DLYBLK must be asserted 4 clocks prior to the end of the addressing block as shown in Figure 5. In this example, DLYBLK is asserted for one clock cycle which delays the start of a new address sequence by one clock. The part is assumed to be configured for One-Shot Mode with Restart. Addressing will resume 5 clocks after de-asserting DLYBLK. Note: BLOCKDONE# and DONE# will be asserted and OUT0-23 will be held until addressing resumes. Also, STARTOUT# will be asserted one clock after the assertion of DLYBLK.

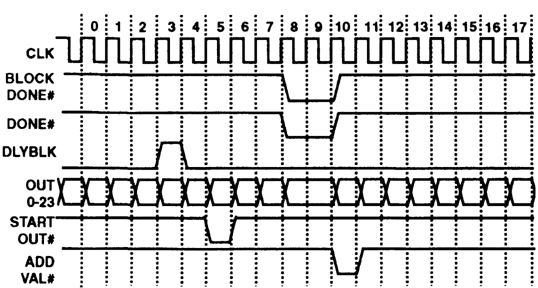


FIGURE 5. SIGNAL RELATIONSHIPS FOR A ONE CYCLE BLOCK DELAY AFTER FINAL BLOCK IN AN ADDRESSING SEQUENCE

STARTIN# Operation

The STARTIN# pin has two functions: first, it downloads the configuration data in the processor interface into the register bank that controls the operation of the part; second, it starts the address sequence using the updated configuration. When STARTIN# is deasserted, the part continues on with the new sequence. Note that there are four stages of pipeline delay between the sequence generator and the output of the part; all of the output signals will continue on using the original sequence for those four clock cycles.

After the assertion of STARTIN#, the first value in the sequence appears on the output after four pipeline delays. The part will remain in this state for the remainder of the time that STARTIN# is low, and for four clocks after STARTIN# returns high. This is shown in Figure 6, note that the old sequence ends at clock 3; the first address of the new sequence goes from clock 4 to clock 12; the second address of the new sequence appears on clock 13.

Asserting STARTIN# in the middle of a sequence demonstrates the sequence restart function as described above. The internal count of the HSP45240 returns to the starting point (the value in the Start Address Register - not the Current Block Start Address Register) on the first rising edge of CLK that STARTIN# is low. The first address of the sequence is output four clocks after the assertion of STARTIN#. The Sequencer goes to the second address in the sequence when STARTIN# goes away; this address appears on the output pins four clocks later. Sequencing continues based on the updated configuration. In Figure 7, the new sequence is started on clock 1; the old sequence will continue unaffected until clock 4, and the first address of the new sequence becomes valid on the outputs during clock 5.

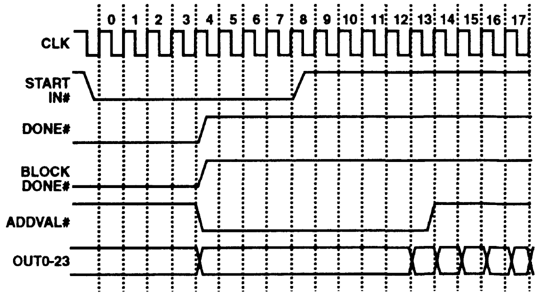


FIGURE 6. INPUT, OUTPUT SIGNALS WHEN STARTIN# IS LONGER THAN ONE CLOCK CYCLE.

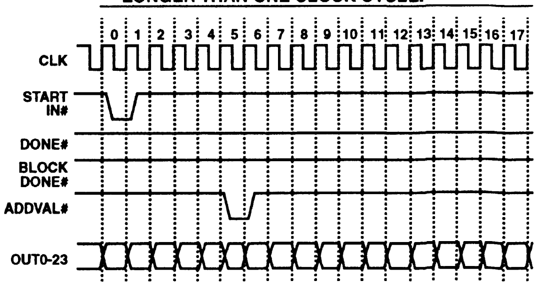


FIGURE 7. USING STARTIN# TO RESTART SEQUENCE DURING OPERATION

Harris Semiconductor

APP NOTE

No. AN9102 January 1994

Harris Digital Signal Processing

NOISE ASPECTS OF APPLYING ADVANCED CMOS SEMICONDUCTORS

By: R. Kenneth Keenan, Ph.D. and David F. Bennett

Introduction and Summary

This report is about noise aspects of high-speed logic, with a focus on Advanced CMOS semiconductor applications. The present report pertains to suppression of ringing for both short and long traces, with experimental evidence provided for long traces.

Although termination and decoupling techniques cited here minimize ringing for all semiconductor technologies (AC/ ACT, LSTTL, HCMOS, AS, etc.), external resistive termination is usually not required for slower semiconductor technologies. Decoupling is an important aspect of design for all semiconductor technologies.

The preferred termination technique is a resistor, R_T, equal in value to the trace's characteristic impedance, Z_O, in series with a trace at the driving end of that trace. For AC/ ACT, series termination results in a modest (1ns to 3ns) increase in propagation and transition times. The increase in transition times incurred with series termination helps to minimize interference generation.

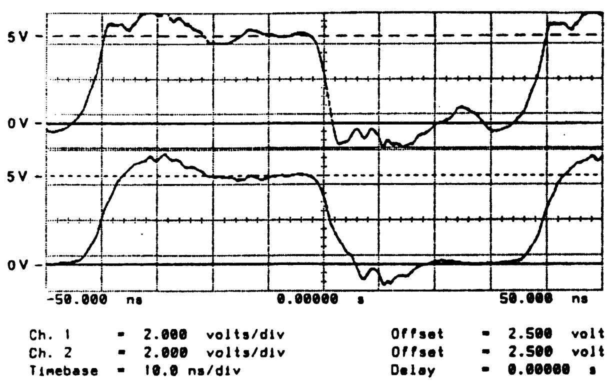
The length of traces with distributed loading to which series termination can be applied is limited by the increased transition times at intermediate points along those traces.

For long traces with distributed loading, AC shunt termination-a resistor in series with a small-value capacitor-is used from a trace to ground at the receiving end of a trace. The value of the capacitor depends on clock frequency, but it is typically 50pF to 200pF. Larger values result in improved pulse fidelity at the expense of increased power dissipation in the terminating resistor. At the expense of a capacitor, AC shunt termination consumes much less power than purely resistive shunt termination. AC shunt termination does not appear to materially effect propagation and transition times, except insofar as it removes the ringing contributing to shorter transition and propagation times.

Series Termination with a Single Receiver

Resistive Termination

Figure 1 illustrates the waveforms at the receiver for the case of no termination and for the case where the line is terminated at the driver end of the line. The termination resistor is 80Ω, approximately equal to the 78Ω characteristic impedance of the line on the board. In this and all succeeding Figures, the line is 12 inches long.



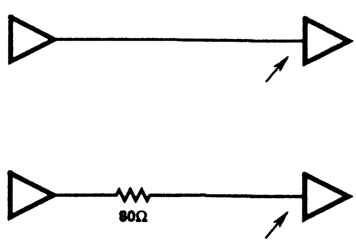


FIGURE 1. UNTERMINATED AND TERMINATED ($R_T \approx Z_O$) LINES

This work was supported by Harris Semiconductor (Harris) and The Keenan Corporation (TKC). The authors thank the external reviewers, Mr. Richard E. Funk, Manager, Applications Engineering, Harris Semiconductor, and Dr. Leonard Rosi, EMC Engineer, of Hewlett-Packard's Corvallis Workstation Operation, for their helpful comments.

9

AP NOTES AND TECH BRIEFS

Zero and five-volt reference lines are shown in each of the above oscillograms. It is clear from Figure 1 that termination assists in reducing both the undershoot for the low-to-high transition and the overshoot for the high-to-low transition. The noise immunity limits for CMOS are given in Table 1.

TABLE 1. NOISE IMMUNITIES AND MARGINS

D.C. SPECIFICATION	VOLTAGE LEVEL (V)
Maximum Low-Level Input Voltage (Max V_{IL})	0.8
Minimum High-Level Input Voltage (Min V_{IH})	2.0
Maximum Low-Level Output Voltage (Max V_{OL})	0.4
Minimum High-Level Output Voltage (Min V_{OH})	2.4
Low-Level Noise Margin ($V_{NML} = V_{IL} - V_{OL}$)	0.4
High-Level Noise Margin ($V_{NMH} = V_{OH} - V_{IH}$)	0.4

For the unterminated line in Figure 1, the maximum V_{IL} 0.8V is breached . Therefore, CMOS gates driven with the unterminated-line (upper) waveform in Figure 1 can mistake the "bump" between t = 20ns and t = 30ns for a "high". Thus, for the unterminated-line waveform, CMOS gates are subject to logic errors. The terminated line rings less and provides a signal which is well within the noise immunity limits for AC/ACT.

The relative sensitivity of the value of termination resistor was assesed. Figure 2 illustrates experimental results.

From Figure 2, the pulse waveform is marginally improved for termination resistance greater than the characteristic impedance, but it becomes more unterminated-like when a terminating resistance less than the characteristic impedance is used.

Table 1 summarizes the effects of terminating resistance on transition times and propagation delays. The propagation delay of the line, 1.8ns, has been subtracted from the experimentally-measured propagation delay in the data in Table 1. The propagation delay was measured as illustrated in Figure 3.

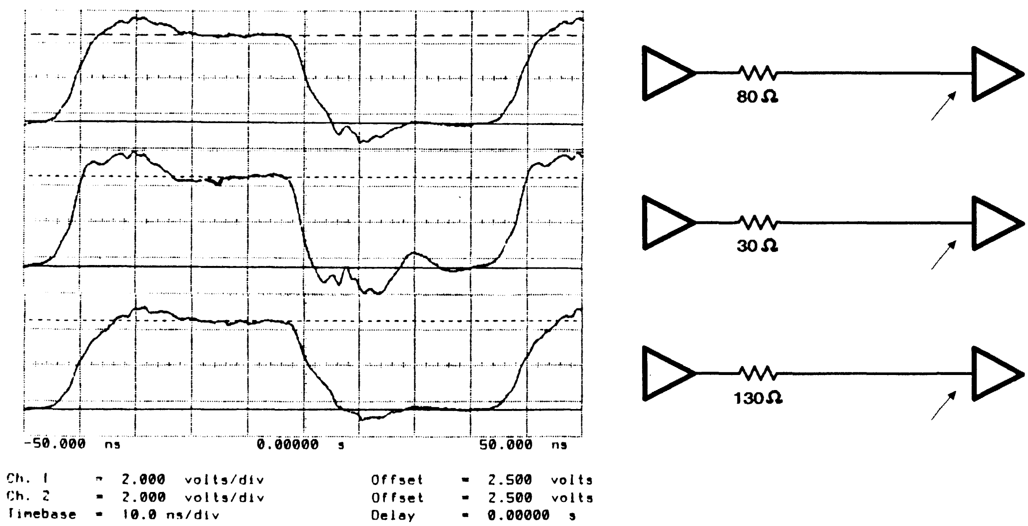


FIGURE 2. SENSITIVITY OF PULSE TO TERMINATING RESISTANCE

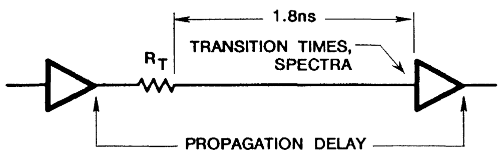


FIGURE 3. MEASUREMENTS

TABLE 2. SUMMARY OF TRANSITION TIMES AND PROPAGATION DELAYS

R_T (Ω)	TRANSISTION TIMES (ns)		PROPAGATION DELAYS (ns)	
	t_r	t_f	t_{plh}	t_{phl}
0	4.0	2.6	3.1	5.0
30	4.6	3.6	3.8	6.0
80 (= Z_O)	5.4	5.8	4.8	8.0
130	8.4	7.4	5.6	10.6

Transition times are measured in the conventions 10%/90% and 90%/10%, and, similarly, propagation delay is measured between the 50% points of the waveforms.

Termination with a resistor equal to the characteristic impedance of the line adds 1.7ns to 3.0ns to the propagation delays and increases the transition times. From the perspective of the emissions problems discussed in Section 9.0, an increase in transition times is good. However, increased propagation delays may be undesirable from a functional standpoint. With AC/ACT, some termination resistance must be used to prevent ringing which could exceed the noise immunity limits.

Shunt Termination with a Single Receiver

AC shunt termination is a means of approximating a resistive termination without incurring the power dissipation of resistive termination. In laptop computers, power drain is a battery life issue. In computers and other powerline-powered digital equipment, power drain causes heat dissipation and implies a diminution in reliability. CMOS, in spite of its speed, consumes relatively little power while operating and near zero power while in standby (or high-Z) states. Therefore, in a total power "budget", it is important to consider the power dissipation of termination resistors.

Figure 4 illustrates the effects of AC shunt termination for two different values of capacitors.

In designing an AC shunt termination, the value of the resistor is equal to the characteristic impedance of the line: $R_T = Z_O$. To allow for complete charging and discharging of the terminating capacitor (C_1) during one-half the clock period: $C_1 < 1/6Z_Of_C$. Then the power dissipated in R_T is $V_{CC}{}^2f_CC_1$ (see Table 7). For the present case of f_C = 12MHz, and $Z_O = 80\Omega$, $C_1 < 1/6Z_Of_C$ = 174pF. At the extreme, where $C_1 \rightarrow \infty$, the power dissipation approaches that of a resistive terminator: $V_{CC}{}^2/2Z_O$ for a 50% duty cycle clock.

For the case C_1 = 56pF, the power dissipation in the terminating resistor is relatively small: 16.8mW. For the case C_1 = 560pF, the power dissipation approaches that of a resistive terminator: 156mW (the power dissipation in the driver is approximately 30mW). However, the waveform with C_1 = 560pF is somewhat better than that with C_1 = 56pF. In shunt termination, one is always trading power dissipation in the terminating resistor for pulse fidelity.

Table 3 summarizes propagation and transition times for AC shunt termination.

TABLE 3. PROPAGATION AND TRANSITION TIMES

TERMINATION	TRANSISTION TIMES (ns)		PROPAGATION DELAYS (ns)	
	t_r	t_f	t_{plh}	t_{phl}
None	4.0	2.6	3.1	5.0
80Ω/56pF	5.0	4.2	4.6	7.2
80Ω/560pF	5.8	4.6	4.2	7.0

AC shunt termination at the sending end (only) was not tried. However, in the context of distributed loads with both ends of the bus AC shunt terminated, the driving-end termination did not improve the waveform.

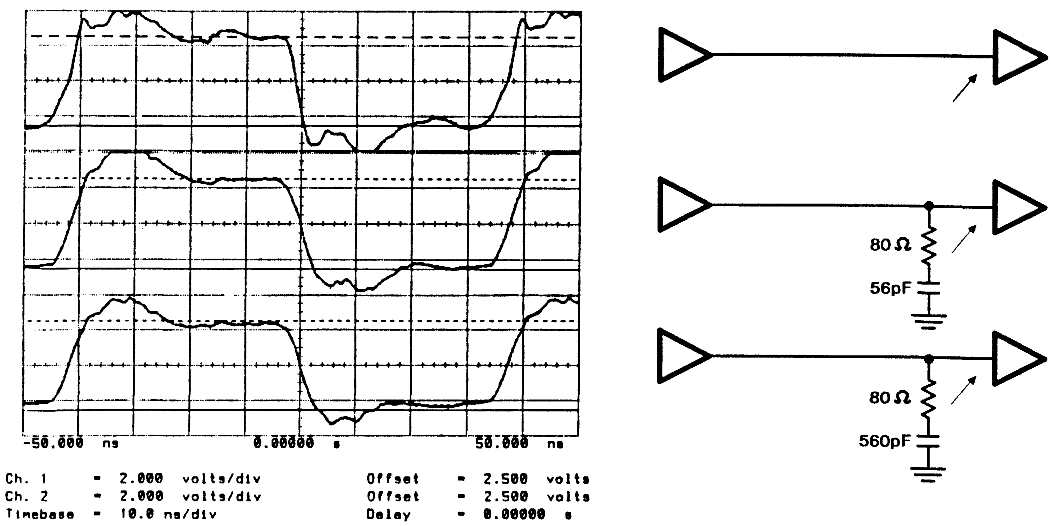


FIGURE 4. AC SHUNT TERMINATION AT RECEIVER

Since computer bus lines may be in the active high state for relatively long periods of time, the DC blocking capacitor, C_1 (56pF and 560pF in Figure 4), can be of considerable benefit when driving CMOS logic. However, when driving bipolar logic, the current required by the inputs of driven gates can total much more than that required by a terminating resistor without a DC blocking capacitor. Then, AC termination offers insignificant advantages over conventional resistive termination.

Terminations Applicable to Distributed Loads

Description of Board with Simulated Load

The circuit shown in Figure 5 is the simulated load used along the bus-like structure on the test board. It is patterned after the equivalent input curcuitry. The inductor was formed by a small loop of wire.

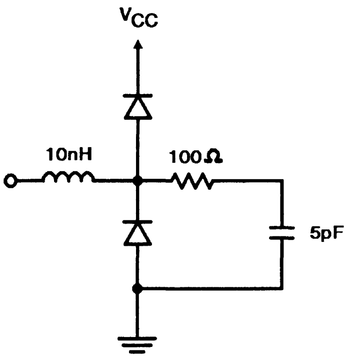


FIGURE 5. SIMULATED CMOS LOAD

The average value of the input capacitance of a CMOS gate is 7.5pF. That value was not available, so 5pF capacitors were used. The above load was distributed along one of the bus traces at points shown in Figure 6. The diodes are 1N914's, high-speed silicon types.

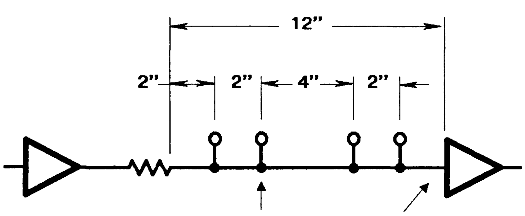


FIGURE 6. DISTRIBUTION OF SIMULATED LOADS ALONG BUS TRACE

The measurements and waveforms cited below were made at the gate four inches from the driver and at the gate at the end of the line. The points designated by arrows in the figure are referred to as the "intermediate gate" and "end gate" in the measurements to follow. In all cases, the waveform at the end gate was the worst case with respect to ringing.

When a load is distributed along a trace, the characteristic impedance of that trace is modified in accordance with [2, p. 148]

$Z_O = Z_\infty/[1 +$ distributed load capacitance on line/capacitance of line$]^{1/2}$ (1)

Z_∞ = Characteristic impedance of line without distributed loading.

In the case of the test board, the capacitance along the unloaded line of 0.72pF/in. x 12in. = 8.6pF, and the distributed load, including that at the last gate, was (4 x 5pF) + 7.5pF = 27.5pF. Then, $Z_O = 80/[1 + 27.5\text{pF}/8.6\text{pF}]^{1/2} \approx 40\Omega$.

Series Termination

Figure 7 illustrates waveforms along the line for unterminated lines, with and without distributed loading, and for the series-terminated line with $R_T = Z_O$. It is clear from a comparison of the top two oscillograms that the presence of distributed loading-even without termination-tends to smooth the waveforms. At least in part, this is probably due to the diodes in the simulated loads, which are also present in CMOS input gates.

Distributed loading increases line propagation delays by the same factor by which the characteristic impedance is decreased, which is a factor of approximately two in the present case. Propagation delay measurements were taken as indicated in Figure 2, with 2 x 1.8 = 3.6ns subtracted from the measured propagation delays to provide the "distributed load" propagation times in Tables 4 and 5.

The problem with using series termination with distributed loading is that the waveform along the line will tend to become a three-level waveform [2, p. 53]. This tendency is clear in the third oscillogram from the top in Figure 7. Thus, in Table 5 the transition times at the intermediate point on the line are greater than those at the end of the line given in Table 4. If the bus was longer, the "kink" at a line voltage of 2.5 volts would be more noticeable. However, in the present case, transition times are great enough to smooth the otherwise sharp three-level waveform. In some applications, an increase in transition times may be acceptable, and the extra component in the form of the capacitor necessary for AC shunt termination-which does not "three-level" the waveform along the bus-is not necessary. AC shunt termination is discussed in the next section.

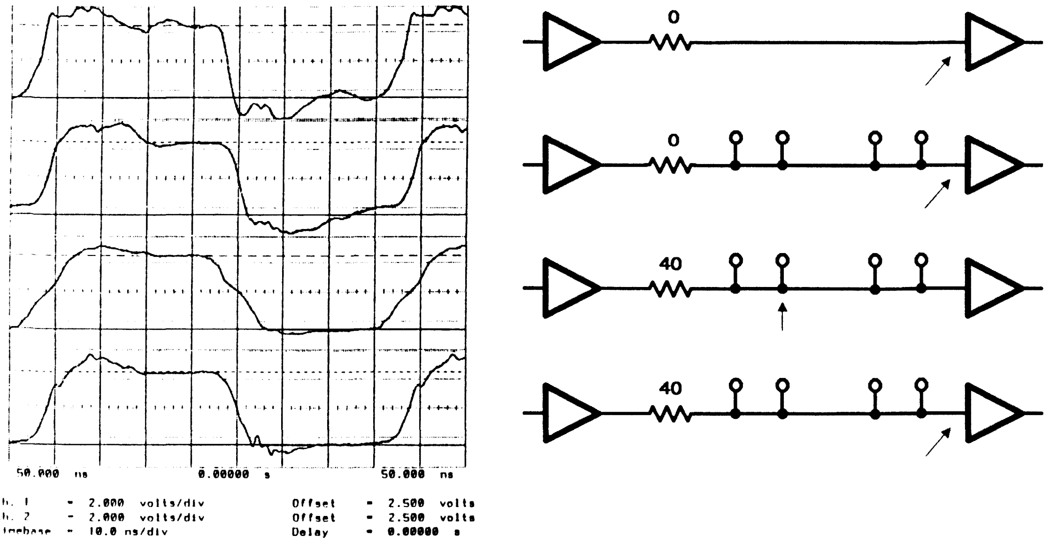


FIGURE 7. WAVEFORMS FOR DISTRIBUTED LOADING

TABLE 4. TRANSITION AND PROPAGATION TIMES-END GATE

R_T (Ω)	TRANSISTION TIMES (ns)		PROPAGATION DELAYS (ns)	
	t_r	t_f	t_{plh}	t_{phl}
0 (No Dist. load)	4.0	2.6	3.1	5.0
0 (Dist. load only)	4.4	3.6	4.4	6.4
40 (= Z_O) + Dist. load	4.8	5.2	5.2	7.8

TABLE 5. TRANSITION TIMES-INTERMEDIATE GATE

R_T (Ω)	TRANSISTION TIMES (ns)		PROPAGATION DELAYS (ns)	
	t_r	t_f	t_{plh}	t_{phl}
0 (Dist. load only)	6.6	5.6	Not measured	
40 (= Z_O) + Dist. load	8.0	7.8	Not measured	

AC Shunt Termination

This termination technique was previously explored in the context of a single load. For the case of loads distributed along a single line, the advantage of shunt termination is that the tendency toward a three-level waveform with series termination is absent. Figure 8 illustrates the waveforms obtained with AC shunt termination. As previously discussed, the corrected (for distributed loading) value of the characteristic impedance is 40Ω.

The discussion of trading off waveform integrity for power dissipation also applies here. The power consumed by the terminating resistor when C = 560pF is substantially greater than when C = 56pF.

Table 6 summarizes propagation and transition time data. As in the preceding section, gate propagation delay = measured delay -3.6ns.

TABLE 6. SUMMARY OF TRANSITION TIMES AND PROPAGATION DELAYS

R_T (Ω)	TRANSISTION TIMES (ns)		PROPAGATION DELAYS (ns)	
	T_R	T_F	T_{PLH}	T_{PHL}
40Ω/56pF				
End Gate	6.0	6.0	3.3	4.4
Int Gate	9.0	8.3	Not measured	
40Ω/560pF				
End Gate	8.0	8.3	3.7	8.0
Int Gate	8.8	9.0	Not measured	

As is evident from a comparison of Tables 5 and 6, shunt termination with a small capacitor (56pF) does not extract as much propagation delay "penalty" as does series termination-nor does a 56pF shunt termination cause a tendency toward a three-level waveform on the bus. With a 560pF capacitor, the waveform is better in the sense that there is less ringing, but, as indicated earlier, the power dissipation of the terminating resistor is substantially increased.

From a comparison of Figures 7 and 8, series termination appears to suppress ringing better than shunt termination-at least that shunt termination where, in order to reduce power consumed by termination resistors, the value of the capacitor is relatively small. Also, the increased transition times associated with series termination are very desirable from the standpoint of minimizing both ringing and ground bounce.

Termination Techniques

Table 7 illustrates termination techniques which can be used at the receiving end of a trace; C_I is the input capacitance of the driven semiconductor. The first three techniques require that the characteristic impedance of the trace structure be well-defined and constant along the trace run, which is complicated when a trace is to be run on both interior and exterior layers of a PCB.

Diode termination allows uncontrolled impedance-such as that obtained on a two-sided board where the trace-to-ground trace spacing is variable-but requires more expensive components than other techniques. In effect, CMOS input circuitry is a mixture of the series and diode termination techniques shown in Table 7.

In Table 7, the Termination Dissipation has been computed by assuming a (worst-case) 0Ω source resistance. The power dissipation expressions apply to use of the terminating networks at either end of the line. For example, the expression given for the dissipation of a series termination applies whether the termination is used on the sending (proper) end of the line or the receiving (improper) end of the line.

Series termination has been analyzed in some detail. For use at either the receiving or sending end, maximum clock frequency is determined by assuming that, after a high-to-low transition, the input capacitor, C_I, must discharge to a voltage below 5% of V_{CC} before the next clock low-to-high transition. This requires that three Z_OC_I time constants occur during one-half of the clock period, which leads to the clock-frequency limitation shown for series termination in Table 7.

The relatively large power consumed in termination resistors can be a problem. **AC shunt termination**, as defined in Table 7 and used in Figures 4 and 8, provides a worthwhile low-power alternative, to be applied at the receiving end of a trace. In AC shunt termination, pulse fidelity is traded off for power dissipation: the larger the value of the DC blocking capacitor, C1, the better the pulse, but the higher the power consumption of the terminating resistor.

In the limit as the value of C1 is made very large, the power dissipation of the terminating network approaches that of purely resistive termination. The improved pulse fidelity with larger values of C1 is apparent from Figure 8. The maximum value of C1 which still permits adequate charging/discharging of the shunt termination network over one-half of the clock cycle is $C_1 < 1/6f_CZ_O$; this inverse clock-frequency limitation is given in the "Max f_C" column of Table 7. However, for C1 >> $1/6f_C Z_O$, the network is slow enough that full charging never occurs, the network begins to approach a purely resistive shunt terminator, and clock frequencies are limited only by the driver.

AC shunt termination should be used whenever the DC drive capability of the driving device is approached via heavy TTL loading.

Decoupling CMOS

Clock-related noise on the V_{CC} bus can arise if too few decoupling capacitors are used [5, p.3.11-1]. It is recommended that all board layouts allow for one decoupling capacitor per semiconductor package. However, it is sometimes possible to remove some of the decoupling capacitors after a working prototype is developed. This is best done experimentally while carefully monitoring emissions, particularly at frequencies less than 200MHz. At those frequencies, cable radiation dominates radiated emissions spectra. Assuming good grounding, cable radiation is an accurate indicator of V_{CC} bus contamination.

On large (> 50-pin) devices with more than one V_{CC} pin, use one decoupling capacitor at each V_{CC} pin. In these cases, then, more than one decoupling capacitor per semiconductor package is recommended.

Choosing the Value of a Decoupling Capacitor

A simplified diagram of the equivalent circuit for the output of a Harris CMOS device is shown in Figure 10. When the circuit shown transitions from low to high, switch S1 connects to terminal A and current is drawn from the V_{CC} bus to charge the capacitor. On a high to low transition, the switch connects to B; current is sourced by the capacitor as it discharges into ground through S1. Note that the switch is, in the ideal case, a "break before make" circuit, so that no current is drawn from A to B as S1 changes state - a common source of current consumption in early CMOS logic.

Departures from ideality include the **totem-pole effect**: for time intervals which are smaller than the transition time, both the upper (PMOS) and lower (NMOS) transistors are partially "on". Then, during both the low-to-high and high-to-low transitions, there is a pulse of current drawn from the V_{CC} bus. This is in addition to the current pulse required-and predicted by the model-for the charging of C_S when making the low-to-high transition. Also, the internal gates-those which precede the output gate-require both totem-pole and charging currents (charging currents for internal gates are much smaller than that required for the output gate, as the source capacitance associated with those gates is on the order of tens of **femptofarads** [1 femptofarad = 10^{-15} farad]).

A decoupling capacitor is the V_{CC} bus for the purpose of supplying current during transitions. The inductance of a V_{CC} trace or plane precludes those sources from supplying all of the rapidly-changing current required during a transition. Between clock pulse transitions, a trace or plane supplies recharge current to decoupling capacitors. Recharging can take place over the much longer time of one-half of the clock period.

A value of 0.1µF will adequately decouple all known AC/ACT glue logic and VLSI circuits (even heavily loaded/fanned out), but the use of that relatively large value should be resisted in order to maintain the highest possible self-resonant frequency of the decoupling capacitor. Use 0.001µF and 0.01µF, not so much for reduced cost as for the purpose of increasing the self-resonant frequency of the decoupling capacitor.

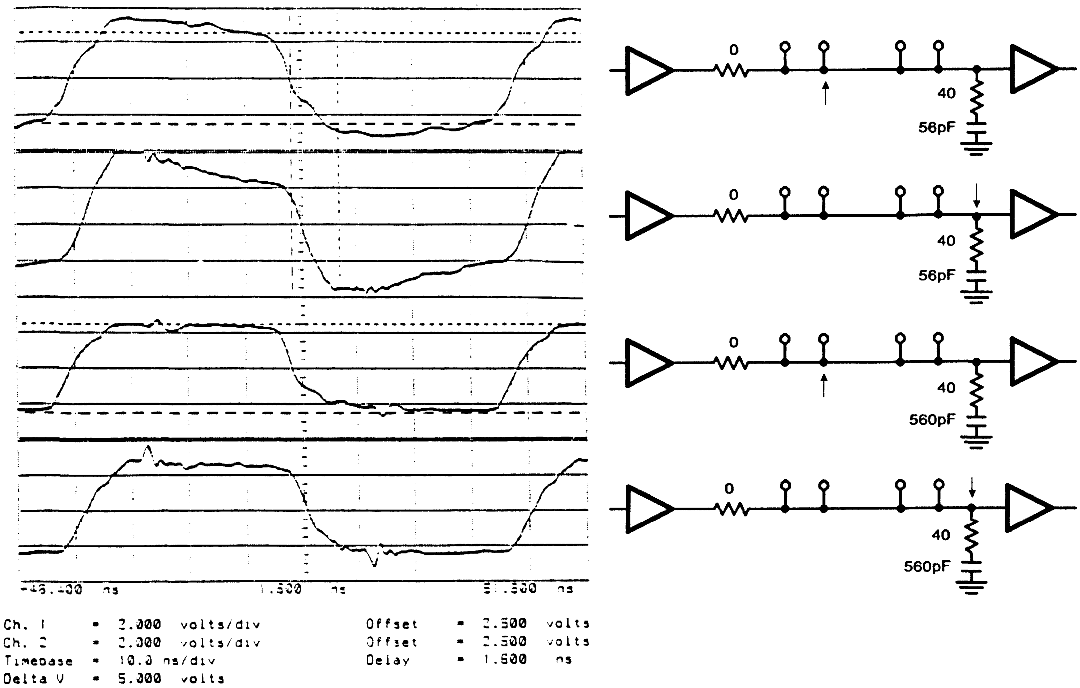
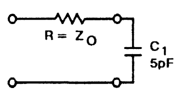
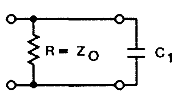
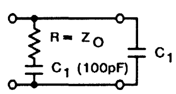
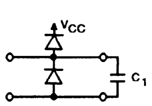


FIGURE 8. WAVEFORMS FOR AC SHUNT TERMINATION

TABLE 7. RECEIVING END TERMINATION TECHNIQUES

TERMINATION	MAX f_C	TERMINATION DISSIPATION	PULSE INTEGRITY	NOTES
 **Series** (Controlled Z_O)	$\frac{1}{6 Z_O C_1}$ (667MHz*)	Very Low: $p = V_{CC}^2 f_C C_1$ (3.8mW)	Improves with small Z_O, C_1	Transition times increased. **Want Low** Z_O
 **Shunt** (Controlled Z_O)	Driver-Limited	Very High: $\frac{V_{CC}^2}{2 Z_O}$ (250mW)	Good Reflected % $= \frac{4.4 Z_O C_1}{t_r - 4.4 Z_O C_1}$	Drive current $= \frac{V_{CC}}{Z_O}$ = (100mA)
 **AC Shunt** (Controlled Z_O)	$\frac{1}{6 Z_O C_1}$ (33.3MHz, see text)	Low to Moderate, increasing with C_1 $P = V_{CC}^2 f_C C_1$ (75mW, about same as device)	Best with largest possible value of $C_1 = 1/6 Z_O f_C$ Intergrity improves with C_1	Must use low-ESL C_1 with short leads Want **Low** Z_O
 **Diode** (Uncontrolled Z_O)	Driver-Limited	Low	Good with high-speed Schotky diodes or built-in protection diodes of some semiconductors	External diodes costly

* Examples are for Z_O = 50, C_1 = 5pF, V_{CC} = 5, f_C = 30MHz, Duty Cycle = 50%

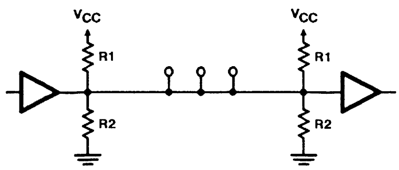


FIGURE 9. RESISTIVE TERMINATION IS USED IN MOST STANDARD BUSES

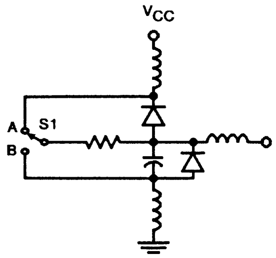


FIGURE 10. EQUIVALENT CIRCUIT FOR CMOS OUTPUT

The Equivalent Series Inductance (ESL) of a Decoupling Capacitor

The equivalent series inductance (ESL) of a decoupling capacitor and the inductance of the leads/planes used to connect the decoupling capacitor to a semiconductor package should be as small as economics and manufacturing practicalities permit. This decreases both ringing and emissions. It is shown in [5, pp. 3.9-7 through 3.9-10] that maximum attenuation of noise on the power bus occurs at the self-resonant frequency of the decoupling capacitor. To have that attenuation occur at frequencies where ringing and emissions suppression is otherwise difficult (generally 35MHz to 90MHz) using a capacitor value chosen according to the previous section requires ESL's less than 10nH. Surface-mount ("chip") capacitors on a multilayer board with both V_{CC} and ground planes are particularly desirable.

The ESL of a decoupling capacitor is at least as important as its capacitance. Above the self-resonant frequency of a decoupling capacitor which provides filtering; that inductance should be as small as manufacturing techniques and economy permit.

Placement of Decoupling Capacitor on a Board

A decoupling capacitor should always be placed on that end of the semiconductor package which points toward the power entry point on a board. One of the purposes of decoupling is to minimize V_{CC} noise at the power-entry point, and the filtration implied by a decoupling capacitor should be between the semiconductor package and the power entry point.

Conclusions and Recommendations

Use Multilayer Boards

The inductances associated with two-sided boards are often too large for successful application of high speed CMOS circuits. Two-sided boards designed from an RF standpoint could be used, but the low component density associated with such boards is inconsistent with most contemporary system design requirements.

The "Best" Termination Technique: Series Resistor at Driving End

When loads do not require much DC current, as with CMOS inputs, the preferred termination technique for a single load and large class of multiple distributed loads is a terminating resistor at the driving end of the trace. The value of the terminating resistor, R_T, is ideally equal to the characteristic impedance of the driven trace, Z_O, as modified by any distributed loading. The correction for distributed loading is given in equation 1.

Reduction of the value of a series terminating resistor from $R_T = Z_O$ leads to decreased propagation and transition times. However, for even zero-length traces, reduction of R_T eventually leads to ringing. Although the internal diodes in the input circuitry of Harris CMOS tend to limit ringing, noise immunity problems can still occur.

Increasing the value of the terminating resistor beyond Z_O tends to further enhance the smoothness of the pulse but can lead to undesirable increases in propagation delays. The resulting increased transition times tend to suppress emissions.

For driving-end series termination with distributed loading on lines 12 inches long, transition times at intermediate loads are doubled relative to those at the end of the bus. Longer buses lead to even greater increases in transition times at intermediate bus points. Should this not be tolerable, the alternative AC shunt termination discussed below should be used.

An Alternative Termination Technique

In the above case and/or when a resistively-terminated bus and/or heavy TTL loads are to be driven by CMOS gates, AC shunt termination should be considered as an alternative to putely resistive termination.

At least for the driven-end terminated case considered in this report, AC shunt termination does not appear quite as effictive as sending-end series termination in suppressing ringing.

When terminating high-speed traces, SIP resistors and capacitors should be avoided. The equivalent series inductance (ESL) is too large in many applications. Discrete SMD's are preferred to minimize ESL.

Minimize Power Bus Ringing to Minimize Interference

To minimize ringing on the power bus, it is recommended that CMOS devices which handle high-frequency periodic signals be carefully decoupled from the power bus. Specific decoupling recommendations have been provided in this report.

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Harris Digital Signal Processing

TEMPERATURE CONSIDERATIONS

Author: Clay Olmstead

Junction Temperature

The energy expended by an integrated circuit is dissipated as heat. In a CMOS system, current (and hence power) increase proportionally with switching frequency. With the advent of fast CMOS circuits, the attendant rise in temperature causes a variety of problems. In some cases, the current and/or temperature constraints placed on the device by its operating environment are the limiting factors on the clock rate. The increased die temperature due to the switching speed produces a number of secondary effects. The propagation delay time of a CMOS gate increases, causing a decline in the overall performance of the system. In addition, the effects of various failure mechanisms are accelerated (see Reliability Fundamentals). Depending on the failure mechanism, the lifetime of the product can be decreased by a factor of two for every 10°C rise in junction temperature.

The internal temperature of a semiconductor device is defined as junction temperature, T_J. Harris products are designed to operate with a 10 year lifetime under the stated operating conditions. For parts in ceramic packages, these include a maximum junction temperature of 175°C. For plastic packages, the maximum T_J is 150°C - this is to maintain the integrity of the package, not the device inside. Note that the 175°C limit is set according to military standards; many users in specific industries set this limit higher or lower, depending on their individual requirements.

Determination Of Junction Temperature

Once the designer has selected an IC and calculated the clock frequency that meets the needs of the application, the operating temperature of the die (junction temperature) must be calculated to determine whether it exceeds reliability guidelines. This involves the concept of thermal resistance: the temperature differential across a body that is dissipating a given amount of energy. There are two common sets of reference points for thermal resistance: θ_{JC} is the temperature differential between the p-n junction of a semiconductor device and the outside surface of the package (case); θ_{JA} is measured from the junction to ambient conditions. Other reference points for measuring thermal resistance are defined depending on specific requirements.

To calculate whether a device will exceed its maximum junction temperature, the first step is to multiply the clock rate by the frequency coefficient (given in mA/MHz) for that product. This is listed in the D.C. Electrical Specifications section of the data sheet under I_{CCOP}. The total package power dissipation is calculated by multiplying that current by the maximum V_{CC}. If this figure is less than the Maximum Package Power Dissipation listed in the data sheet, then the operating conditions meet Harris specifications. In some applications, it is necessary to operate the part using a higher junction temperature (for applications that can absorb the penalty in expected lifetime) or lower temperature (for high reliability applications). Users with these requirements calculate their actual junction temperature using one of the following equations. Given the maximum ambient temperature, the proper equation is:

$T_J = (\theta_{JA} \times P) + T_A$ Equation 1

Where:

T_J = Junction Temperature of the Part In °C
θ_{JA} = Thermal Resistance from Junction to Ambient In °C/W
$P = I_{CCOP} \times V_{CC}$
T_A = Ambient Temperature

The junction temperature for a given case temperature is:

$T_J = (\theta_{JC} \times P) + T_C$ Equation 2

Where:

T_J = Junction Temperature of the Part In °C
θ_{JC} = Thermal Resistance from Junction to Case In °C/W
$P = I_{CCOP} \times V_{CC}$
T_C = Case Temperature

Reducing Junction Temperature

If, after going through the above equations, the junction temperature exceeds the allowable limit, there are several possible solutions. With some types of parts, such as digital filters, the user can replace a single part running at a high data rate with multiple parts, each operating at a reduced clock rate. Using this method, the junction temperature of each IC is reduced but the throughput of the entire circuit is unaffected. In most cases, the optimum solution is to improve the heat flow out of the package by adding a heat sink and/or forcing airflow across the package. Moving air lowers the effective θ_{JA} of the part as shown in Figure 1. The required value for the effective thermal resistance is calculated by solving equation 1 for θ_{JA}:

$\theta_{JA} = (T_J - T_A) / P$ Equation 3

Once the necessary value for θ_{JA} is known, Figure 1 is used to locate the corresponding air flow for the package of interest. Note that the improvement in thermal impedance is a function of the airflow measured in linear feet per minute (lfm), but fan manufacturers measure airflow in cubic feet per minute (cfm). Assuming 100% efficiency, lfm is converted to cfm by multiplying the required lfm by the cross sectional area of the path of moving air. In reality, obstructions in the airflow cause back pressure, which diminish the fan output to between 60% and 80% of its free air capacity; divide the lfm figure derived from Figure 1 by this compensation factor to obtain the required fan output.

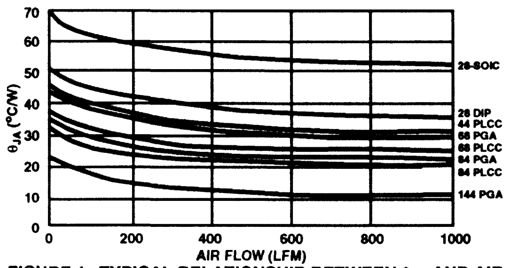

FIGURE 1. TYPICAL RELATIONSHIP BETWEEN θ_{JA} AND AIR FLOW FOR VARIOUS PACKAGES

Another viable solution is to use a heat sink, either by itself (natural convection) or with moving air (forced convection). There is a wide range of heat sinks available for virtually any package type. Note, however, that a heat sink is much more effective when used in combination with a ceramic package. This is due to the greater thermal efficiency of the ceramic material: most of the flow of thermal energy is from the die directly into the package, where the entire surface of the part acts as a radiating surface to let the heat escape. Some energy flows from the die through the bond wires and pins and out through the copper traces in the board, but this effect is negligible due to the fact that the bond wires are only 1 mil in diameter and thus their thermal impedance is relatively high. In a plastic package, the main path for the heat flow is from the die through the paddle and the plastic molding compound and on to the outside world. Since plastic is a relatively poor thermal conductor, other paths, such as the bond wires, take on a greater proportion of the total heat transfer so that their contribution is no longer negligible. For this reason, a heat sink mounted to a plastic package dissipates less heat than Equation 2 would indicate. Harris recommends the use of a ceramic package for operating conditions that require a heat sink.

Addition of a heat sink puts two additional elements in path of thermal transfer: the heat sink and the thermal joint compound that attaches it to the package. The total value for θ_{JA} is divided into its component parts: the thermal resistance from the junction to the surface of the package, from the package to the heat sink, and from the heat sink to ambient:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \qquad \text{Equation 4}$$

Where CS is the thermal resistance from the IC package to the heat sink, which is controlled by the mounting technique and thermal joint compound used. θSA is the thermal resistance from the heat sink to ambient.

Under natural convection, heat sink dissipation is a function of the power dissipation of the chip. The heat sink manufacturer's catalog will specify the performance for their products using a chart similar to that shown in Figure 2. Starting with the power dissipated by the device on the x axis, find the corresponding temperature rise of the package on the y axis. Add this value to the ambient temperature, T_A, to find the elevated case temperature. Use Equation 2 to find the new junction temperature.

If a fan is to be used, then the following procedure is recommended. Use Equation 3 to calculate the required total thermal resistance. Solving Equation 4 for θ_{SA}, calculate the maximum thermal resistance allowable for the heat sink. The literature from the maker of the heat sink will have a chart similar to Figure 3; find θ_{SA} on the right axis and find the air flow that corresponds to that value on the top axis. (The placement of the axes is to allow Figures 2 and 3 to be combined into one graph.) Convert lfm to cfm and divide that value by the compensation factor for back pressure mentioned above; use that figure to select a fan.

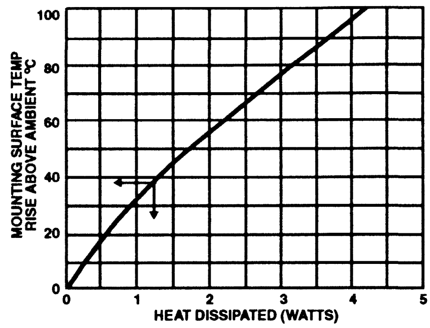

FIGURE 2. PACKAGE TEMPERATURE INCREASE AS A FUNCTION OF POWER FOR A TYPICAL HEAT SINK UNDER NATURAL CONVECTION

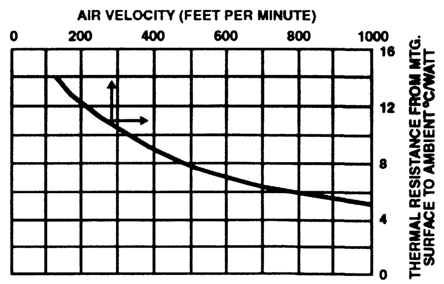

FIGURE 3. THERMAL RESISTANCE VERSUS AIR VELOCITY FOR TYPICAL HEAT SINK UNDER FORCED CONVECTION

For Further Reading

The discussion above outlines the overall method for calculating the thermal parameters of a circuit. the interested reader may refer to the following references for further information.

MIL STD 883 Method 1012.1; JEDEC ENG. Bulletin No. 20, January 1975; 1992 Semi Std. Vol. 4, Methods G30-86, G32-86, G42-88, G43-87

No. TB310 January 1994

COMMON ABUSES OF THE HSP43220

1. Loads too many coefficients. Only "half" the coefficients (including center tap) are needed. Loading more or less coefficients will cause incorrect operation.
2. Improper reset of part. Both clocks must be active during reset. Both start pins high during reset and remain high until programming complete.
3. Starting part too soon. Under software control, the start pins may float momentarily before programming is complete. Once started, any writes of coefficients are ignored.
4. In DECIMATE, customer tries to bypass the HDF by setting Hdec = 1 and Stages = 1. The correct settings are HDec = 1 and Stages = 0.
5. Customer is violating the CK_IN duty cycle requirements when HDF is bypassed. See A.C. Specifications in data sheet.
6. Customer confuses even/odd symmetry bit with even/odd length filters.
7. Customer tries to run HDF bypassed with CK_IN = FIR_CK.
8. Customer thinks that taking the start pin inactive will stop the part. Only reset can stop the HDF section once it has been started.
9. Has intermittent or poor results from cheap socket or poor part insertion.
10. General - input rise/fall time to slow (>10ns), input setup/ hold violations, noise.
11. System board problems are causing incorrect acquisition of outputs from DDF. i.e. in a multiplexed bus structure there is bus contention.
12. Customer does not realize data is held at outputs until next DATA_RDY.
13. Customer does not relax passband attenuation as much as possible and valuable taps are wasted.

Debug Ideas

1. Bypass the FIR or HDF sections individually or together. If the clocks are tied together the HDF section can be pseudo bypassed by setting HDRATE as usual but set GROWTH = 50 and STAGES = 0. The HDF will output every Nth input sample. This will verify correct wiring of the DATA_IN bus and some of the C_BUS bits.
2. Read out coefficients as per memo.
3. Try writing F_DIS =0 then F_DIS = 1 before loading coefficients. If this helps then poor reset procedure or floating start pins are likely.
4. Input a DC value, it should pass through a low pass filter.
5. Are DATA_RDY's at correct frequency? (CK_IN/(H_{dec}+F_{dec}).

HSP43220 - DESIGN OF FILTERS WITH OUTPUT RATES <2(Passband + Transition)

One of the design rule checks in DECI•MATE is that the output rate must be greater than 2 times the sum of passband + transition band. For the informed user, violation of this rule is a valid design choice. Suppression of this rule check in DECI•MATE is not possible, but design of such a filter using DECI•MATE is possible.

The general solution is to use DECI•MATE to design a filter with an output rate that is twice the desired rate, or a integer multiple of the desired rate that is >2(pass + trans). Outside of the Design Module the FIR decimation rate is increase by the factor needed to achieve the desired output rate. The new filter response is obtained graphically.

Consider a filter with a passband of 70KHz and a transition band of 60KHz. The desired output rate is 200KHz. DECI•MATE requires an output rate of >260KHz, an output rate of 400KHz is chosen (see Figure 1 below and FILTER 1 page 2).

By increasing the FIR decimation by a factor of 2 the folding point ($F_S/2$) is moved and the desired output rate is obtained. The filter response can be generated graphically. The aliasing component is represented by the dotted line (see Figure 2 below).

Notice in FILTER 1 the stopband attenuation was limited to 40dB (FIR_CK=CK_IN). Because the FIR decimation was increased from 5 to 10, there are more taps available with FIR_CK=20MHz. Using equation 2.0 from the 43220 data sheet, we see how many taps are available.

$$\#\text{Taps} = \left(\frac{2 \times 20(10)10}{20} - 10 - 4\right) = 172$$

We can therefore use FILTER 2 which uses 151 taps and has 96dB stopband. The part will of course be programmed for FIR decimation rate of 10 and an FIR_CK of 20MHz is used.

To correctly simulate or generate PROM files for the "new filter" the *.DAR file must be edited. The corrected value for FDRATE on line 1 column 4 is entered. The correct output rate and FIR_CK rate are entered on the next to the last and the last line of the *.DAR file.

The above procedure works for standard or Precomp FIR. Remember the maximum FIR decimation rate is 16.

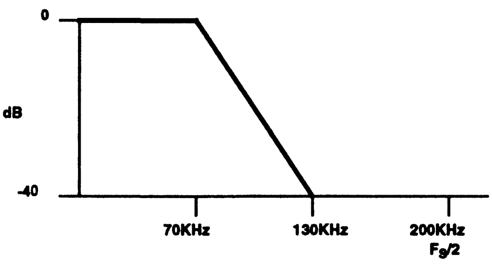

FIGURE 1

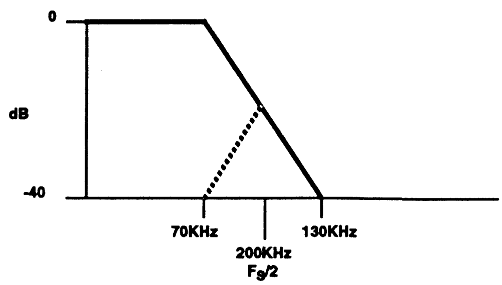

FIGURE 2

```
DESIGN MODULE                 SIMULATOR MODULE                PROM MODULE

                        HSP43220 DDF FILTER SPECIFICATION
D
     Filter File        : filter1.DDF
E    Input Sample Rate:          20 MHz   Design Mode          :  AUTO
     Output Rate        :       400 kHz   Generate Report      :  YES
C    Passband           :        70 kHz   Display Response     :  LOG
     Transition Band    :        60 kHz   Save Freq Responses:    NO
I    Passband Atten     :       0.1 dB    Save FIR Response    :  NO
     Stopband Atten     :        40 dB
•
     FIR Type           :  STANDARD
M

A
     HDF Order          :          2    FIR Input Rate  :     2 MHz
T    HDF Decimation     :         10    FIR Clock (min) :    20 MHz
     HDF Scale Factor :      0.78125    FIR Order       :    81
E                                       FIR Decimation  :     5
```

FIGURE 3. FILTER DESIGN USING STANDARD TECHNIQUE.

```
DESIGN MODULE                 SIMULATOR MODULE                PROM MODULE

                        HSP43220 DDF FILTER SPECIFICATION
D
     Filter File        : filter2.DDF
E    Input Sample Rate:          20 MHz   Design Mode          :  AUTO
     Output Rate        :       400 kHz   Generate Report      :  YES
C    Passband           :        70 kHz   Display Response     :  LOG
     Transition Band    :        60 kHz   Save Freq Responses:    NO
I    Passband Atten     :       0.1 dB    Save FIR Response    :  NO
     Stopband Atten     :        96 dB
•
     FIR Type           :  STANDARD
M

A
     HDF Order          :          4    FIR Input Rate  :     2 MHz
T    HDF Decimation     :         10    FIR Clock (min) :    40 MHz
     HDF Scale Factor :      0.61035    FIR Order       :   151
E                                       FIR Decimation  :     5
```

FIGURE 4. FILTER DESIGN DISREGARDING FIR CLOCK (MIN).

HSP43220
DECI•MATE DESIGN RULE CHECKS

In order to maximize effectiveness of DECI•MATE software there are two design rule checks that need some in depth discussion. Once these crosschecks are understood the usefulness of DECI•MATE and the DDF will improve because filters that were previously thought unrealizable are in fact achievable. Consider the following normalized HDF response (to first null).

In Figure 1 the dotted line represents aliasing. The point defined by stopband attenuation (50dB) and the sum of the passband and transitionband frequencies, must not cross the dotted line. Sometimes in MANUAL design mode you will come upon a filter in which you can vary either the transition-band or passband frequencies or attenuation by just a few Hz or a few dB, and find the filter jumps from unrealizable due to many taps to a viable filter that only needs a few taps. This may be due to crossing the aliasing curve. This in effect, renders the HDF ineffective and DECI•MATE is trying to accomplish everything in the FIR. You may also get the error message "HDF unrealizable".

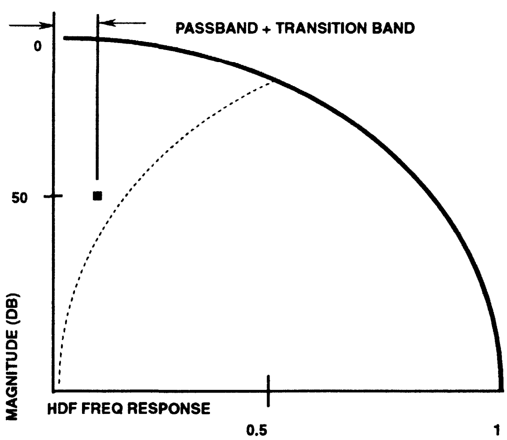

FIGURE 1.

Violation of the second rule exhibits similar symptoms.

Figure 2 illustrates the design rule check that the HDF rolloff should not violate the passband attenuation spec. This condition can occur in a variety of ways, if the passband is a large percentage of the output rate, if the passband attenuation is very small, if most of the decimation is being done in the HDF (which brings the first null of the HDF response in close to the passband region). The number of stages in the HDF also determines the rolloff of the HDF response. This design rule check is done with no knowledge of the type of FIR being used, STANDARD, IMPORTED, or PRECOMP. Therefore switching to a PRECOMP, or IMPORTED FIR will not alleviate a violation of this rule. The PRECOMP FIR can in fact reduce the HDF rolloff effect when the rolloff is within the limits stated above.

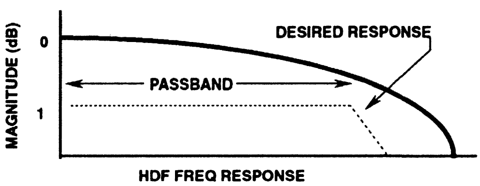

FIGURE 2.

It is important the user understand which rule is being violated because the first one is hard and fast, must not be violated. The second is correctable with additional work (manual design of FIR on other software). It is of course possible that both rules are being broken. There are two simple tests that can be done to identify what the problem is. If the difficulty is with HDF rolloff in the passband (rule 2), then relaxing the passband attenuation will allow the software to generate a filter.

If the problem is intrusion of stopband attenuation past the dotted line (rule 1), then changing the passband attenuation will not solve anything. Try reducing the stopband attenuation, a little, then a lot, if this results in a filter design then the problem is rule 1.

Solutions

If DECI•MATE was in design mode MANUAL when the problem occurred then the user can adjust the design parameters (input rate, output rate, passband, transition band, passband attenuation, stopband), or the HDF filter parameters to achieve a filter. For problems with rule 1 try any of the following: higher input rate, narrower passband, less stopband attenuation, less HDF decimation, more HDF stages. For problems with rule 2 try any of the following: higher input rate, higher output rate, narrower passband, looser passband attenuation, less HDF decimation, fewer HDF stages.

In general, if DECI•MATE was in design mode AUTO when the problem occurred, then going to manual design mode and playing with HDF stages, or HDF decimation will not produce any better results (with the one exception noted below as "Special Case"). The user then must decide if the system can tolerate the relaxed design parameters (input rate, output rate, passband, transition band, passband attenuation, stopband attenuation) needed to achieve a realizable filter. If not, the user will need to perform a manual design of the HDF and FIR filter parameters.

Special Case

For those users who have the option of low system decimation rates there are some alternatives. For those with system decimation rates of less than 10, trying varying combinations of HDF decimation and HDF stages may prove worth while. Also, for those that can have system decimation of 16 or less, bypassing the HDF (setting HDF decimation to 1 and HDF stages to 0) and using only the FIR may be beneficial.

NOTES ON USING THE HSP43220

Operation And Programming

Typical operation of the part using DECI•MATE software is as follows. RESET# is held low long enough to satisfy the specification of 4 clocks for the slowest clock. Coming out of reset both start inputs must be high. After waiting the specified reset recovery time the registers are then loaded. H_Register1: H_DRATE register will accept values from 0 to 1023. H_BYP is set as desired. F_CLA is typically set to a zero, F_DIS is set to a zero. H_Register2: H_STAGES is set as desired, a six or seven may be entered and will be interpreted as a five. H_GROWTH is entered as specified in the data sheet or DECI•MATE with acceptable values from 0 to 63, with values above 50, the most significant bits of the input data will be dropped. F_Register: F_TAPS will accept values from 2 to 511. DECI•MATE always generates odd tap filters, therefore the value N to be entered will typically be even. F_DRATE, enter value between 0 and 15 as desired. F_ESYM, as with most filter design software, DECI•MATE always generates even symmetric filters, enter a one. F_BYP, enter as desired. F_0AD, typically set to a zero, used only for non-symmetric filters and for verifying filter coefficients. FC_Register, for a the value N loaded in the F_TAPS register there will be (N/2)+1 coefficients to be entered for odd length filters and N/2 coefficients for even length filters. It takes two writes to load each coefficient. Internally the number of coefficients loaded is recorded and used to determine the length of the filter, NOT F_TAPS. F_TAPS is used to offset a read pointer in the data RAM and to determine if an odd or even number of taps is being done to properly handle the center tap.

With programming of the HSP43220, the part must be started as described in the data sheet. If STARTIN# is used, it will be the third rising edge of CK_IN (from STARTIN# active) that the DATA_IN pins will start accepting data. If ASTARTIN# is used it will be the fifth rising edge of CK_IN.

If at any time RESET# goes active, or glitches low, the above procedure must be repeated (except for reloading coefficients). Also see reprogramming.

Implementing Non-symmetric Filters

The HSP43220 can implement up to a 256 tap non-symmetric filter. Correct programming procedures are as follows. By definition the number of coefficients loaded is equal to the number of taps (N). The F_TAPS is set equal to 2N-1, and F_0AD and F_SYM are set to a one. The remaining registers are loaded normally.

Data_in Bus

In many cases the source of information to be fed into the DATA_IN pins will be less than 16 bits wide. The recommended configuration is to connect the input bus to the most significant bits of DATA_IN and to tie unused DATA_IN pins to GND. In some systems there will be available a 16 bit bus to connect to the DATA_IN pins but the full range of the bus is not being used. For example the upper 4 bits are always sign bits. This can be adjusted for in software by setting the growth for three more than normal. Even if the HDF is to be bypassed this can be accomplished by manually putting the HDF in bypass. This is done by setting H_STAGES and H_DRATE to 0. For the case described above, H_GROWTH would be set to 50+3, or 53. This pushes the 3 extra sign bits off the top of the data shifter.

Output Format

As stated on page 4-5 of the DECI•MATE manual, the FIR coefficients are computed using the Parks-McClellan (Remez) method and then scaled by the inverse of the HDF scale factor as well as an additional factor which accounts for the maximal ripple gain of the derived FIR. As a result, the output format is as follows. DATA_OUT bits 0-15 are the most significant bits. If OUT_SELH is held high, then DATA_OUT bits 16-23 are simply sign extension, if held low they are the LSB extension, for a total of 24 bits of resolution. For those that wish more bits of resolution the sign extension bits can be used. This may be accomplished through the users own software or the coefficients from DECI•MATE may be scaled. This is accomplished by determining the magnitude of the largest coefficient, and then multiplying all coefficients by the factor 0.999999/mag. The coefficients must then be quantized to 20 bits. This results in the magnitude of the largest coefficient being about 0.999999, the largest representable value. This procedure also allows the realization of filters of greater than 96dB attenuation since it reduces quantization effects. The new position of the decimal point in the output will be moved into the sign extension bits with its exact position being dependent on the coefficients.

Bypass Modes Of The HDF And FIR

When the H_BYP bit is set, H_Register2 bits are affected as follows. H_GROWTH is set to 50, H_STAGES is set to zero. The clock divider is disabled so CK_DEC=CK_IN. The H_Register1 value H_DRATE is not altered by setting the H_BYP bit. H_Register2 must be reloaded after H_BYP has been returned to a zero.

With H_BYP set to a one, the feedback paths in the integrators and the holding registers in the comb are zeroed. The 16 bits of chip input data pass through the HDF section unaltered. As always, the first data sample out of the HDF (after reset/startup) is a zero due to resetting of the data paths. Because the FIR section has several operations to complete between rising edges of CK_DEC it is necessary for FIR_CK to be faster than CK_IN as described in the data sheet. The duty cycle of CK_IN must meet the conditions described Tech Brief TB312. DECIMATE can be used to determine the necessary frequency of FIR_CK or equation 1.0 in the data sheet can be solved for the case of HDF in bypass by setting Hdec=1.

When the F_BYP bit is set the FIR filter is configured as a 3 tap, even symmetric filter, no decimation with one input to the pre-adder set to zero (same side as if F_0AD was set). The output of the coefficient ram is forced to 00004H to aid in positioning the result in the accumulator. The output multiplexes are set by the F_BYP bit to output data from the bottom of the accumulator. For a 3 tap filter there are two multiply/accumulate (MAC) cycles. The data flow is as follows. A new piece of data becomes available at the HDF output as signaled by a rising edge of CK_DEC. The FIR is signaled and the data is written into the data ram. The first MAC cycle begins. From the data ram the new data and some old data are read. The new data is added to zero in the pre-adder, then multiplied by the coefficient, and then accumulated with a zero (because start of new FIR cycle). The second MAC cycle starts one FIR_CK cycle after the first. Two old pieces of data are read from ram. But two zeros are input to the pre-adder because of zeroing the other side of the pre-adder at the center of odd length tap filters. The resulting zero is multiplied by the coefficient and accumulated. The accumulator results are sent to the output pins along with a DATA_RDY.

Reprogramming

After initial startup of the HSP43220 the FIR section can be reprogrammed using the F_DIS bit of H_Register1. When writing H_Register1 be sure to maintain the same values in bits 0-10, H_DRATE and H_BYP. When the F_DIS bit is written the FIR section will terminate a FIR cycle if one is in progress, no DATA_RDY is issued. The FIR section is disabled from performing multiply/accumulate cycles. The FIR_CK must continue to run. The HDF section continues to operate and its output continues to be written into the data ram. By letting the HDF section continue to run the synchronous operation of multiple DDFs is maintained. By continuing to load the data ram a transient response is avoided when the FIR section is restarted. Writing the F_DIS bit also resets the coefficient ram address pointer to zero (to allow for reloading coefficients) and enables writing of the coefficient ram (writing is disabled when FIR section is enabled). Once the bit is set and at least two rising edges of FIR_CK have occurred, the user may then reconfigure the FIR section as desired. The FIR section can be re-enabled either by writing F_DIS to a zero or by generating a high to low transition on either of the start inputs, which automatically clears F_DIS.

For those users that wish to clear the HDF data paths before bringing in a new signal, or for those that wish to change HDF programming and have multiple DDFs running synchronously, activating the RESET# input is recommended. Re-programming the DDF and restarting will be necessary. The coefficient ram is not corrupted by reset and will not need to be reloaded unless new coefficients are needed. It is also possible to reconfigure the HDF without losing synchronization between DDFs if CK_IN is stopped (high or low) during writing of the registers. For single chip applications or where synchronization is not a concern, the HDF registers can be written on the fly. This will result in a transient response and changing HDF registers at regular intervals in an attempt to achieve fractional decimation rates with the chip is not recommended.

Internal Decimation

The total decimation in the DDF, also called the system decimation, is equal to the product of Hdec and Fdec. The output rate of the DDF will be equal to CK_IN divided by system decimation, regardless of FIR_CK speed. The time from the start of the DDF to the first DATA_RDY may not be the same as time between DATA_RDYs. To the user the FIR decimation appears at the FIR output. That means the output of the DDF is equivalent to using a standard FIR filter and only looking at every Nth output for FIR decimation of N.

In the HDF the counter used for decimation is initialized to Hdec. The first CK_DEC (internal to chip) will occur about Hdec CK_INs after the part is started. The FIR decimation counter is initialized to zero and the first CK_DEC will always cause an FIR cycle which generates a DATA_RDY about taps/2 FIR_CKs later. Thus the time delay from start of the DDF to the first DATA_RDY is about CK_IN period times Hdec plus FIR_CK period times taps/2.

Transient Response

After reset, after changing the source of input data, or after re-programming the HDF, the output of the DDF will have a transient response until the data ram is sufficiently full of "valid" data. There is no transient response when only the FIR is reprogrammed using the FIR disable bit in the control register. It is impossible to predict exactly when the transient is complete as the answer depends on the FIR filter coefficients as well as new data values relative to old data values in both the FIR and HDF.

First the integrator stage(s) must be flushed of old data (except when reset is used). The number of stages and growth will influence this. But in general the flushing of the integrator stages is small compared to the remainder of the chip. For N stages it will take N CK_DEC cycles to flush all the holding registers in the comb. The number of taps determines how many locations of the data ram needs to be written with new data. The equation for the number of input samples needed to complete the transient response is:

number of input samples = Hdec(taps + N)

The number of output samples that are part of the transient response is:

number of output samples = taps/Fdec + N/Fdec

Because the center coefficients are usually much larger than outer coefficients the transient response is done before all the ram locations are filled. In some cases in half the time described above.

The simulator in DECI•MATE assumes all unwritten ram locations are zero and may not necessarily reflect the startup transient of the DDF. This can be overcome by making sure leading zeros are input ahead of the signal for both the simulator and the chip. For the case of the data input changing (one signal followed by another) the simulator will match the DDFs transient response. You cannot simulate reprogramming the DDF.

Clock Inputs

The requirement that the two input clocks be synchronous is driven by the handshake circuitry between the HDF and FIR section. In this circuitry there is a flip/flop which has CK_DEC as the data input and FIR_CK as the clock input. Based on the theory that it is impossible to design a synchronizer that is 100% immune to metastable conditions it was needed to specify the FIR_CK and CK_IN inputs as synchronous inputs. Metastable condition refers to when the flop output oscillates due to the data and clock changing simultaneously. For the user that finds it very inconvenient to use synchronous clocks, or for one that does not wish to use clocks that are integer multiples (which is by definition not synchronous), the use of a local synchronizer can be of benefit. This option puts the risks and control of metastability at the board level under user control. One example of this might be a user that has designed the needed filter in DECI•MATE and the required FIR_CK is 35Mhz with a CK_IN rate of 5Mhz. Through the use of equation 1.0 in the data sheet the minimum FIR_CK is 32Mhz. The software chose 35Mhz because it is smallest integer multiple (30Mhz would have been to slow). Assume the fastest available speed grade of HSP43220 is 33Mhz. The user may then use a local synchronizer to make the filter realizable. The following is just one example of a local synchronizer that re-aligns the system clock edges to create a synchronous CK_IN.

The following restrictions are needed to insure maximum performance.

1. System clock must have high and low times greater than oscillator period.
2. Have to still meet DATA_IN setup and hold times at DDF pins. Use of Q bar output makes this easier.
3. Realistically the maximum system clock rate is one sixth of oscillator.

Node A can still become metastable but it has one oscillator period to become stable. The user has access to node A and can make his own evaluation as to if the circuit performance is acceptable. In general the higher the speed capabilities of the flip/flops used makes for faster resolution of the metastable condition if it should occur.

Harris Semiconductor

TechBrief

No. TB312 January 1994

Harris Digital Signal Processing

HDF BYPASS IN THE HSP43220

When HDF bypass is selected special timing restrictions exist for signal CK_IN.

When no decimation is selected for the HDF section either by setting the H_BYP bit to 1 or by setting H_DRATE = 0, the timing requirements for CK_IN require special consideration. The FIR section of the chip is signaled that there is new data from the HDF when a transition is detected on the signal CK_DEC (see Figure 1). Failure to meet the timing requirements on CK_IN when H_d = 1 results in no or erratic DATA_RDY pulses being issued.

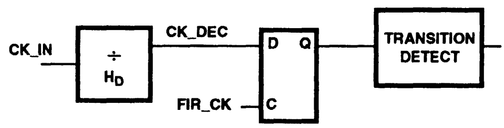

FIGURE 1. CK_DEC GENERATION AND DETECTION

When H_d > 1, the internal divider sets the high or low time of CK_DEC equal to the period of CK_IN, guaranteeing that CK_DEC will be detected by FIR_CK (Figure 2). When H_d = 1, the duty cycle of CK_DEC is the same as CK_IN as shown in Figure 3.

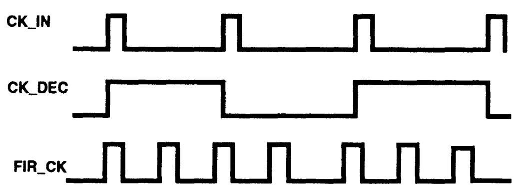

FIGURE 2. CIRCUIT TIMING WHEN H_D = 2

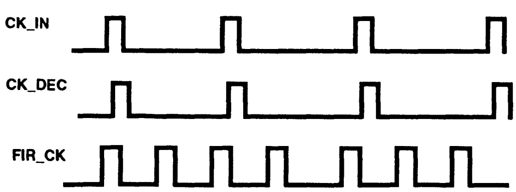

FIGURE 3. CIRCUIT TIMING WHEN H_D = 1

By definition of valid part operation, any time H_d = 1 the FIR_CK will be at least 2 times the frequency of CK_IN.

In the example shown in Figure 3, the state of CK_DEC is always a zero when sampled by the rising edge of FIR_CK. To insure that signal CK_DEC is sampled in both its high and low state by the flipflop requires careful control of CK_IN. The most obvious solution is for the high or low time of CK_IN to be a minimum of one period of FIR_CK. This guarantees sampling both a 1 and a 0 no matter what the phase relation of FIR_CK and CK_IN is.

There is a specified range of allowed phase offset between FIR_CK and CK_IN as given in the AC specifications by spec TSK. Using this spec with 2ns of margin yields the following minimum CK_IN high or low time with setup and hold as specified.

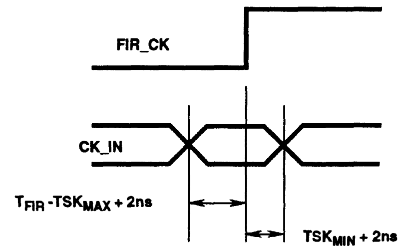

FIGURE 4.

For a 25Mhz part the minimum high or low time requirement for CK_IN is 19ns (when H_d = 1) given the above timing (independent of clock frequencies).

For the typical user, guaranteeing the CK_IN high and low times greater than or equal to the period of FIR_CK will be the most desirable solution in terms of hardware. For the user with additional system constraints, such as those that vary the frequency of CK_IN but hold a high or low time constant, the above timing yields the most flexible solution.

READING OUT FIR COEFFICIENTS FROM THE HSP43220

There are two methods of reading out the FIR coefficients. With method 1, a single coefficient is output with every DATA_RDY. With method 2, a coefficient is output every rising edge of FIR_CK.

Method 1

The premise is to configure the 43220 to look like a FIR filter, input an impulse, and observe the coefficients at the output.

First, the FIR section of the chip is programmed for no decimation ($F_{dec} = 1$). This may require changing H_DRATE from the original setup (see BYPASSING THE HDF). The F_REG is written for the original value of F_TAPS, F_BYP = 0, F_0AD = 0, F_ESYM = 1, F_DRATE = 0, and F_CLA = 0 (H_REG1). The FC_REG is loaded normally. The FIR data ram must be sufficiently filled with zeros before the impulse. The minimum number of zeros to clock into the 43220 is Hdec*taps. The pin OUTSELH should be set to a zero. An impulse, value 0800H, is input and the coefficients will be output in the order, outer coeff through center coeff and back to outer coeff. The 20 bit coefficients are output on the 24 DATA_OUT pins with the format shown below.

Method 2

This method allows for reading out the FIR coefficients in less time than method 1 but requires the system to have the ability to capture the value on the DATA_OUT pins every FIR_CK. DATA_RDY has no meaning in this mode. The HDF section must be configured as described in the BYPASSING THE HDF portion of this memo. For an NTAP filter, the value for F_TAPS is either NTAPS or NTAPS-1, which ever is odd. For example, for either a 67 or 68 tap filter, F_TAPS = 67. Set other FIR parameters as follows: F_BYP = 0, F_0AD = 1, F_ESYM = 1, F_DRATE = 0, and F_CLA = 1

Instead of an impulse, the DATA_IN pins are held at the value 0800H. After (taps/2)(Hdec+10) CK_IN cycles, all the coefficients will be output on consecutive FIR_CKs in the order in which they were written.

Bypassing The HDF

Use the following equation to determine the H_{dec} required with $F_{dec} = 1$ (if F_{dec} was equal to 1 in the original filter then the correct H_{dec} is already known).

$$H_{DEC} = \frac{CK\_IN\ [\ (taps/2) + 5]}{FIR\_CK}$$

Round the resultant value for H_{dec} up to the next integer value.

For $H_{dec} = 1$, set H_BYP = 1, in this case an impulse is defined as the DATA_IN pins having the value 0800H for one rising edge of CK_IN.

For H_{dec} = N, N>1, set HBYP = 0, H_DRATE = N-1, H_GROWTH = 50, H_STAGES = 0. In this case an impulse is defined as the DATA_IN pins having the value 0800H for N rising edges of CK_IN (see Figure 1).

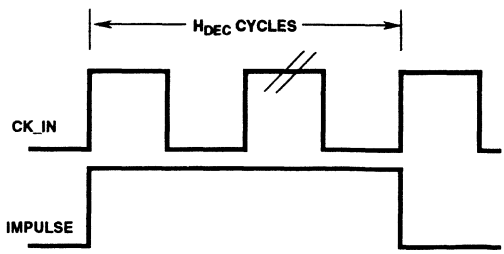

FIGURE 1

OUTPUT FORMAT

DATA_OUT	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	c7	c6	c5	c4	c3	c2	c1	c0	SE	SE	SE	SE	c19	c18	c17	c16	c15	c14	c13	c12	c11	c10	c9	c8

SE - SIGN EXTENSION

QUADRATURE DOWN CONVERSION WITH THE HSP45116, HSP43168 AND HSP43220

The Harris HSP45116 Numerically Controlled Oscillator/ Modulator (NCOM) can be combined with a low pass filter to perform down conversion on a digital signal. The NCOM rotates the spectrum of a real or complex signal and outputs a complex data stream. The signal of interest is now at base band, so that the output can be low pass filtered to eliminate unwanted signals (Figure 1).

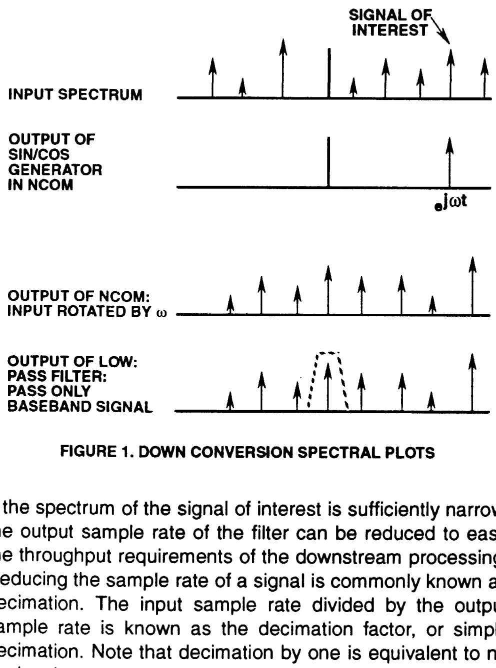

FIGURE 1. DOWN CONVERSION SPECTRAL PLOTS

If the spectrum of the signal of interest is sufficiently narrow, the output sample rate of the filter can be reduced to ease the throughput requirements of the downstream processing. Reducing the sample rate of a signal is commonly known as decimation. The input sample rate divided by the output sample rate is known as the decimation factor, or simply decimation. Note that decimation by one is equivalent to no decimation, and decimation by less than one is undefined. For the purposes of this discussion, base band signals will be divided into two categories: wide band signals, where the decimation factor is 16 or less, and narrow band signals, where the decimation is greater than 16.

Narrow Band Down Conversion

For narrow band output signals, Harris has a three chip set with a filter that is capable of decimation by up to 16,384. Figure 2 shows how the NCOM and HSP43220 Decimating Digital Filter (DDF) are connected to perform down conversion and real to quadrature conversion of an input signal. This is a generalized block diagram which can be used as the basis for a specific design.

Several assumptions were made in defining this block diagram. Among these assumptions are:

- Input and output data are sixteen bits. Users requiring less than that should keep bit 15 as the most significant bit, grounding the unused bits on the input of the NCOM. In all cases, bits 0 through 15 on the output of the NCOM should be connected to the sixteen input bits of the DDF. To select the output bits of the DDF, note that if the input is a cosine at frequency A and the NCOM is tuned to frequency B and the phase offset is 0, then the real and imaginary outputs of the NCOM at sample n are:
- Real Output: cos(An)cos(Bn) = [cos(An-Bn) + cos(An+Bn)]
- Imaginary Output: cos(An)sin(Bn) = [sin(An+Bn) - sin(An-Bn)]
- Note that the factor of $^1/_2$ has been omitted. The output of the Complex Multiplier is shifted left by one bit internally. For this reason, both the real and imaginary outputs have the same magnitude as the input.
- The Phase Register is selected to control the phase of the NCOM (as opposed to MOD0-1) and is initialized along with the center frequency. In this example, the LOAD# signal is not exercised, so the initial phase of the NCOM is unknown.
- To shift the positive component of a real input signal to base band, the Center Frequency Register of the NCOM is set to a negative number.
- The Offset Frequency Register, Timer Accumulator and Complex Accumulator of the NCOM are not used.
- The filter clocks of the two DDFs are driven at a higher rate than the input data clocks. For many applications the FIR_CK, CK_IN and CLK signals can all be connected together. In this case the divide by N block is not needed.
- The DDFs are reset and started asynchronously with a pulse generator that receives asynchronous commands from an outside source and drives the two DDFs simultaneously. The DDF receiving the asynchronous start pulse performs the synchronization and starts the other part at the proper time.

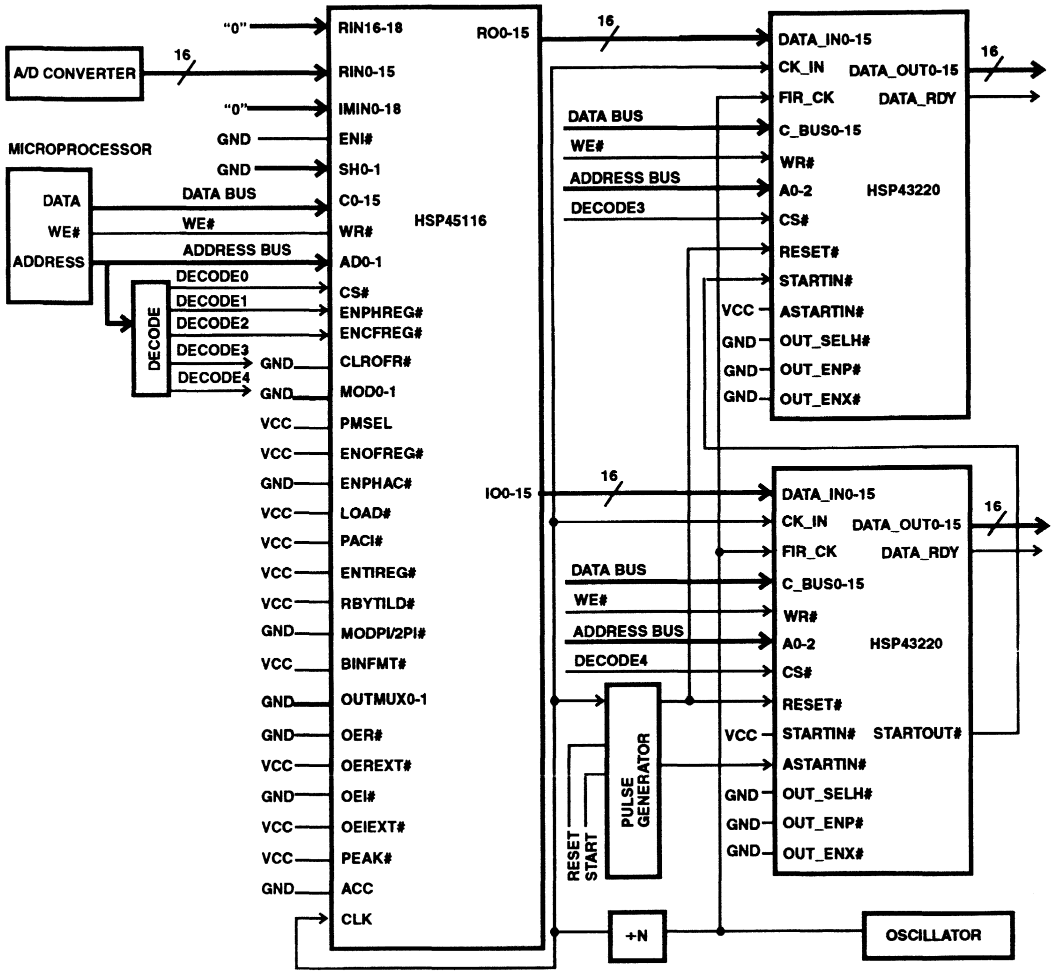

FIGURE 2. BLOCK DIAGRAM FOR QUADRATURE DOWN CONVERSION WITH HSP45116 AND HSP43220.

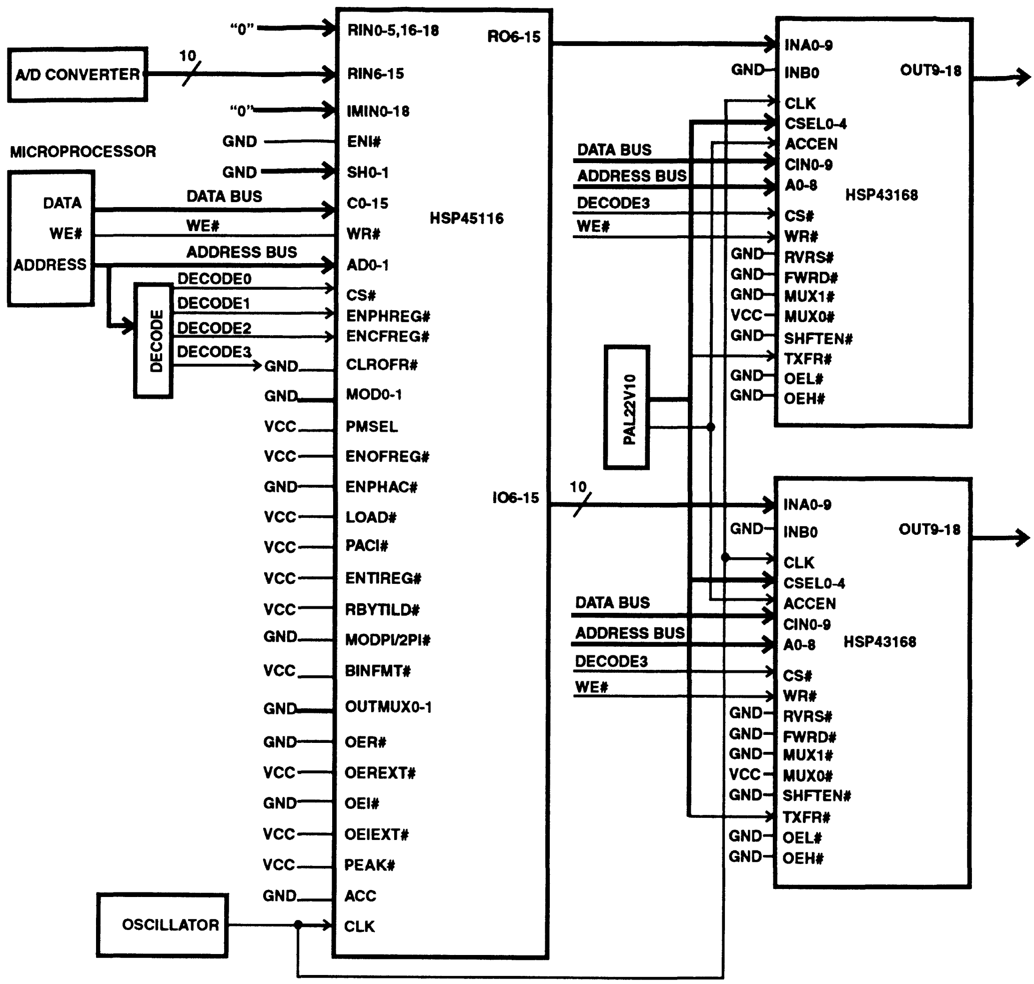

FIGURE 3. BLOCK DIAGRAM FOR WIDE BAND QUADRATURE DOWN CONVERSION WITH HSP45116 AND HSP43168.

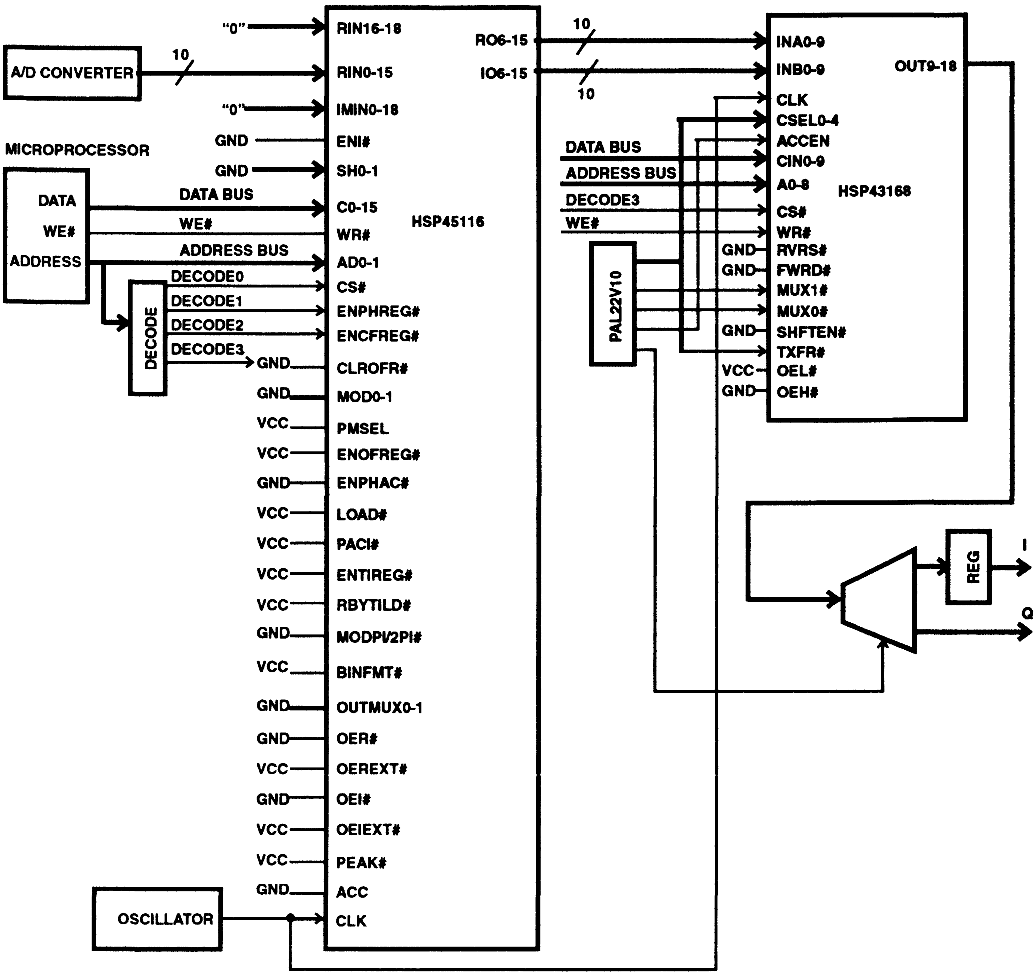

FIGURE 4. BLOCK DIAGRAM FOR WIDE BAND DOWN CONVERSION WITH HSP45116 AND HSP43168.

Wide Band Down Conversion

Figures 3 and 4 show how the NCOM and HSP43168 Dual FIR Filter (Dual FIR) are connected to perform down conversion and real to quadrature conversion of an input signal. Because the Dual FIR can implement either one or two filters, two block diagrams are shown. Figure 3 shows the case where each 43168 is implementing a single filter. The maximum number of coefficients in this case is 16 times the decimation factor for each filter. Figure 4 shows the same configuration with the exception that the Dual FIR is now configured as two independent filters, each with a maximum length of 8 times the decimation factor.

These are generalized block diagrams which can be used as the basis for a specific design. Note that they do not represent detailed schematics with all gates represented. For instance, the control signals are driven with a single PAL22V10 operating as a self contained state machine; it reality, the 22V10 may not have enough gates to generate all the necessary output sequences; in that case, it would be necessary to have a counter generate the states and use the PAL to decode the counter output, generate the control signals to the 43168, and reset the counter when the sequence is completed.

The design parameters of these circuits are:

- Input data is 10 bits. Users requiring less than that should keep bit 15 as the most significant bit of the NCOM, grounding the unused bits on the input. In all cases, bits 6 through 15 on the output of the NCOM should be connected to the input bits of the Dual. To select the output bits of the Dual, note that if the input is a cosine at frequency A and the NCOM is tuned to frequency B and the phase offset is 0, then the real and imaginary outputs of the NCOM at sample n are:
- Real Output: cos(An)cos(Bn) = [cos(An-Bn) + cos(An+Bn)]
- Imaginary Output: cos(An)sin(Bn) = [sin(An+Bn) - sin(An-Bn)]
- Note that the factor of $^1/_2$ has been omitted. The output of the Complex Multiplier is shifted left by one bit internally. For this reason, both the real and imaginary outputs have the same magnitude as the input.
- The Phase Register is selected to control the phase of the NCOM (as opposed to MOD0-1) and is initialized along with the center frequency. In this example, the LOAD# signal is not exercised, so the initial phase of the NCOM is unknown.
- To shift the positive component of a real input signal to base band, the Center Frequency Register of the NCOM is set to a negative number.
- The Offset Frequency Register, Timer Accumulator and Complex Accumulator of the NCOM are not used.
- The decimation rate in the Dual FIRs is greater than one. For no decimation, TXFR# should be grounded. Note that the maximum number of coefficients in the 43168 is eight or sixteen times the decimation rate, depending on the mode (see above).

Combined Narrow And Wide Band

In some applications, it is necessary to pass both wide and narrow band signals. In this case, both the HSP43220 and HSP43168 can be used in parallel, with the user selecting the output of either set of chips, depending on the characteristics of the signal of interest. Figure 5 shows this application, with most of the control signals eliminated for clarity. (These signals can be derived from the previous block diagrams.) In addition, note that the input data clock (CK_IN) and the FIR clock (FIR_CK) of the DDF have been connected together. This configuration is applicable when the input data rate is sufficiently high to allow the filter to operate at this rate also. If this is not the case, the divide by N circuit used in Figure 2 could be used, with the high speed clock driving the FIR_CK pins and the divided down clock used for all other clocks in the circuit.

New Products

Now available from Harris are the HSP50016 Digital Down Converter, which is a single chip quadrature down converter and low pass filter (Figure 6). In addition, the HSP43216 Half Band Filter allows the user to double the input sample rate of the NCOM for real signals (Figure 7). Contact your local Harris sales office or representative for more details on these and other new products from Harris.

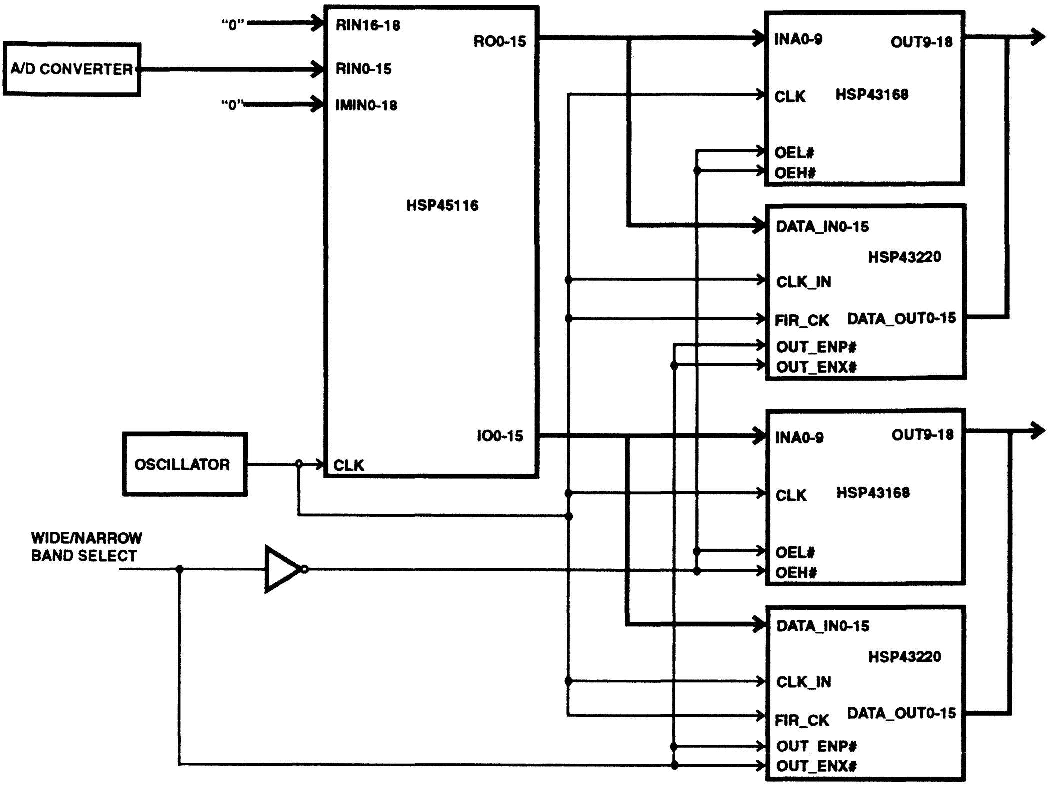

FIGURE 5. BLOCK DIAGRAM FOR QUADRATURE DOWN CONVERSION WITH HSP45116, HSP43220 AND HSP43168

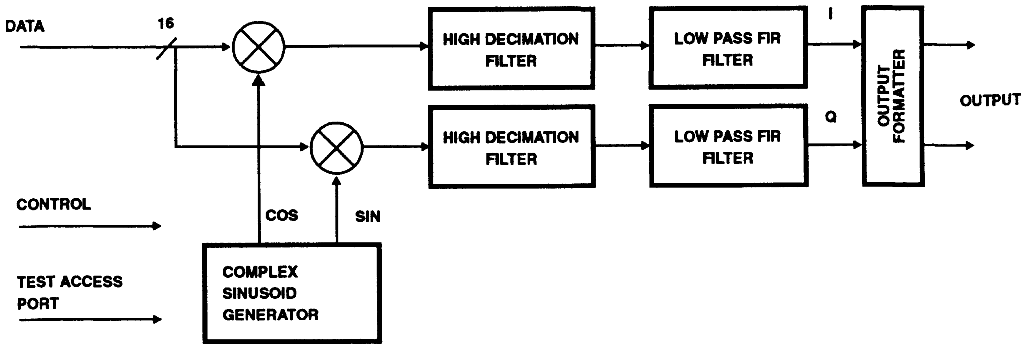

FIGURE 6. BLOCK DIAGRAM OF HSP50016 DIGITAL DOWN CONVERTER

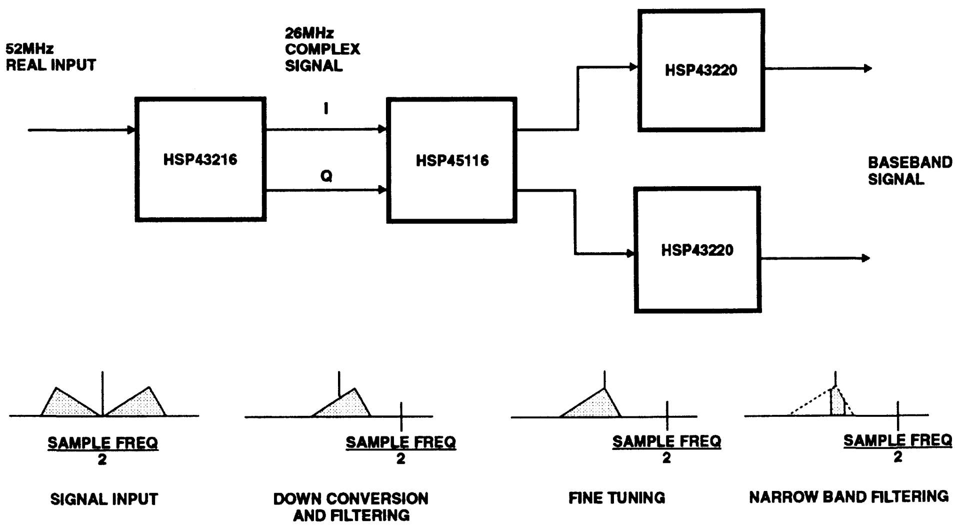

FIGURE 7. HALF BAND FILTER IN QUADRATURE DOWN CONVERSION

No. TB316 January 1994

PIPELINE DELAY THROUGH THE HSP45116

The following timing diagrams show the pipeline delays through the HSP45116 NCOM from the time that data is applied to the inputs until the outputs are affected by the change. The delay is shown as a number of clock cycles, with no attempt made to accurately represent the setup and hold times or the clock to output delays.

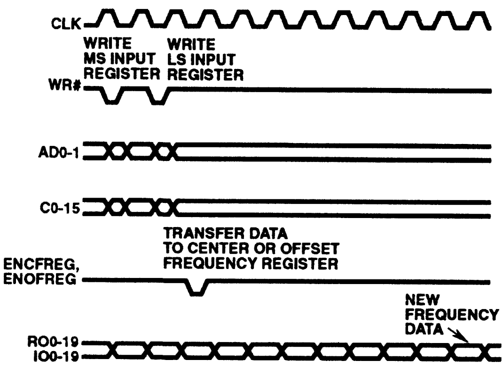

FIGURE 1. FREQUENCY TO OUTPUT DELAY

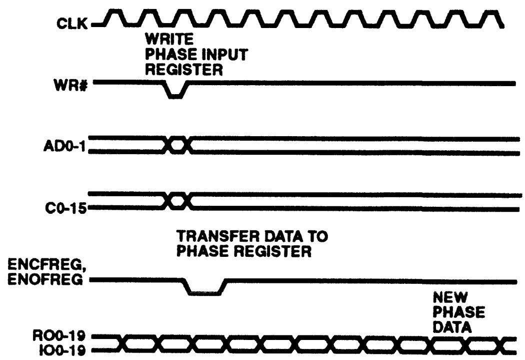

FIGURE 2. PHASE TO OUTPUT DELAY

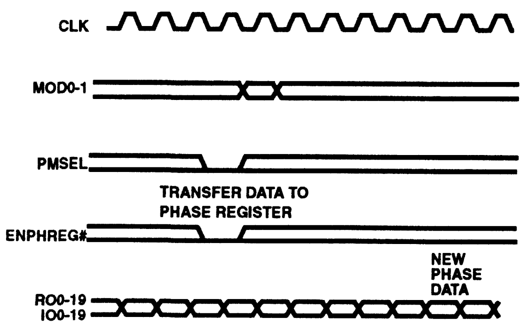

FIGURE 3. PHASE MODULATION TO OUTPUT DELAY

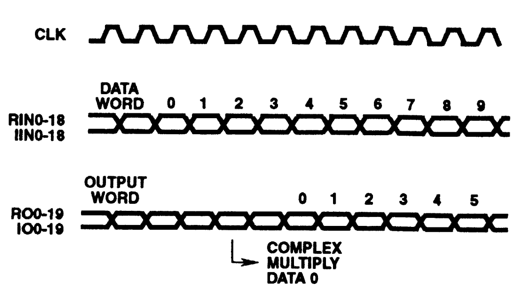

FIGURE 4. VECTOR INPUT TO OUTPUT DELAY

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No. TB319 January 1994

Harris Digital Signal Processing

READING THE PHASE ACCUMULATOR OF THE HSP45106

The block diagram shown below illustrates the method of reading the phase accumulator of the NCO16 from a microprocessor. The setup shown is very similar to that used when the part is used for generating a complex sinusoid, except that the internal SIN/COS lookup is bypassed by putting a logic 1 on the TEST pin. While the TEST pin is high, the phase accumulator continues to drive the inputs of the SIN/COS Generator while the most significant 28 bits of the phase accumulator are multiplexed out onto the output pins. Because of this, the part can be operated in two modes, one where the SIN/COS Generator is permanently bypassed, and one where the phase accumulator output is brought out to the outputs as a check.

Figure 1 shows the circuit for reading out the phase accumulator all the time. In this case, a microprocessor loads the frequency and phase registers of the NCO16. This is fairly straightforward, except the Start Logic block, which needs to be synchronous to the oscillator clock and the microprocessor interface. This has been left as an undefined function, since it is dependent on the implementation. Also note that COS0-15 are connected up, although only COS4-15 are valid in this application. The microprocessor reads the sine and cosine data busses as if they were RAMs, using the decoded address bus to select one or the other.

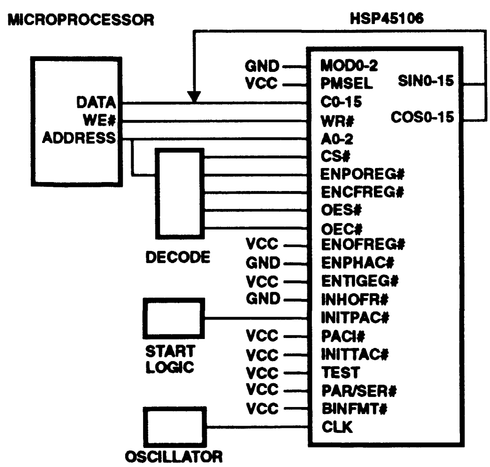


FIGURE 1. CIRCUIT FOR READING PHASE ACCUMULATOR OF NCO16

The timing for loading the center frequency register and seeing the output on COS0-15 and SIN0-15 is shown in Figure 2. This timing is independent of whether the output data represents the phase accumulator data or the SIN/COS Generator output.

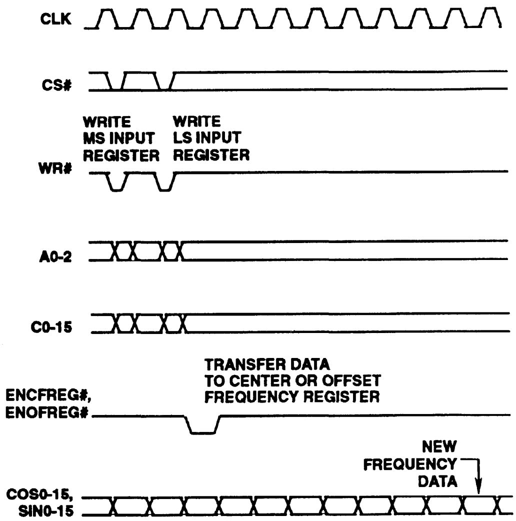


FIGURE 2. NCO16 PIPELINE DELAY

When the output of the NCO16 is to be switched back and forth between sine/cosine and the phase accumulator, a circuit such as the one shown in Figure 3 could be used. In this case, the sinusoidal output cannot be interrupted, so the phase accumulator must be read out between samples. This is possible due to the fact that the TEST signal is simply the control line for a multiplexer on the output of the SIN/COS Generator, but carries with it a limitation on the maximum possible clock rate. Since TEST is a synchronous input, the output of the NCO16 must be either driven by the SIN/COS Generator or the phase accumulator for an entire clock cycle. Therefore, the part must be driven at twice the desired speed at all times so there is a clock cycle available for TEST when necessary. Note that the processor must be driven from the same clock that generates the NCO clock in order to maintain synchronous operation. The timing is identical to that shown in Figure 2 with CLK replaced with CLK/2.

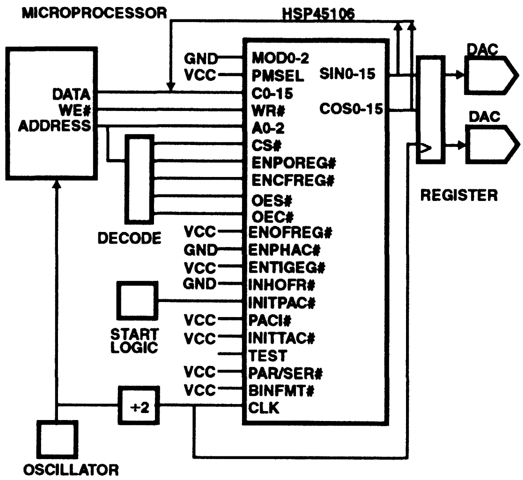


FIGURE 3. CIRCUIT FOR READING PHASE ACCUMULATOR OF NCO16 WHILE GENERATING SINUSOID

Harris Semiconductor

TechBrief

No. TB317 January 1994 *Harris Digital Signal Processing*

PIPELINE DELAY THROUGH THE HSP45106

The following timing diagrams show the pipeline delays through the HSP45106 NCO16 from the time that data is applied to the inputs until the outputs are affected by the change. The delay is shown as a number of clock cycles, with no attempt made to accurately represent the setup and hold times or the clock to output delays.

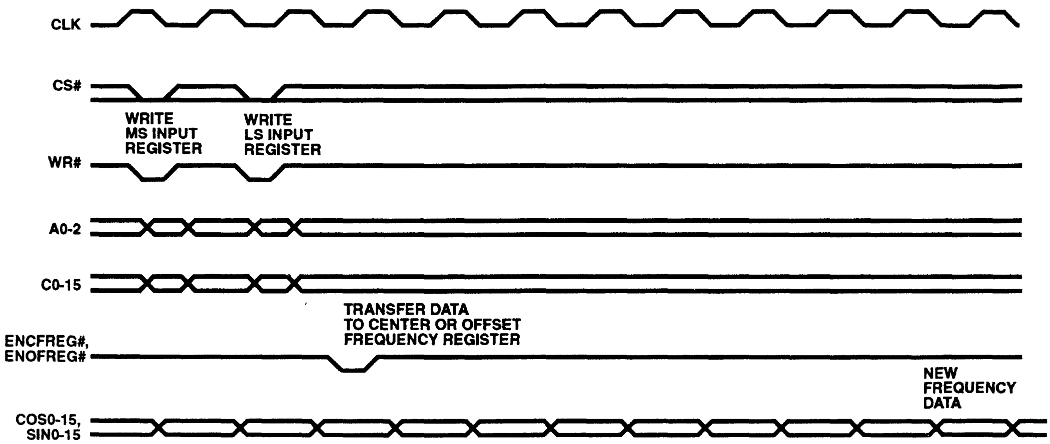


FIGURE 1. FREQUENCY TO OUTPUT DELAY

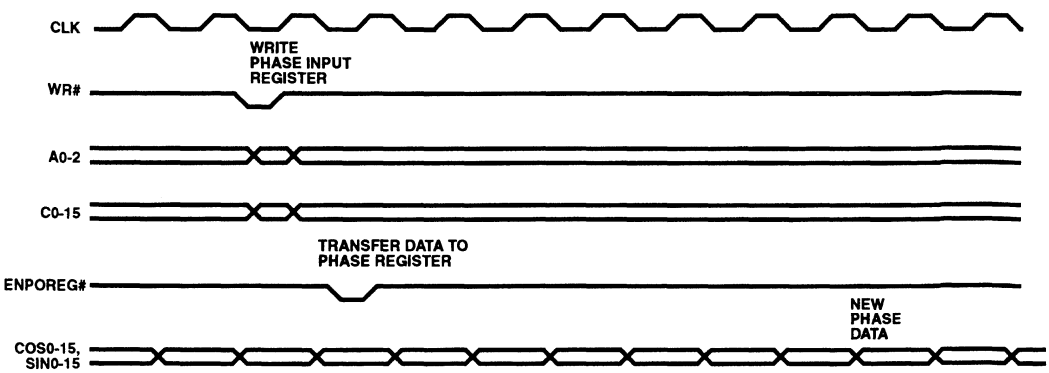


FIGURE 2. PHASE TO OUTPUT DELAY

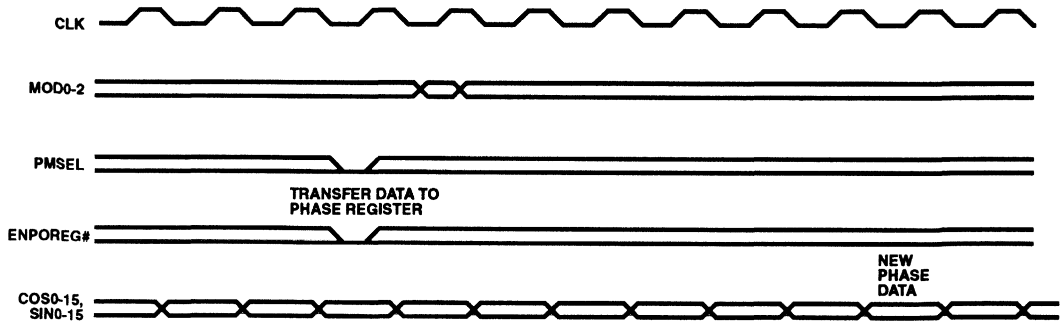


FIGURE 3. PHASE MODULATION TO OUTPUT DELAY

THE NCO AS A STABLE, ACCURATE SYNTHESIZER

Low Jitter Frequency Reference

In communication and other circuits, it is often necessary to produce an accurate reference signal whose frequency and phase can be precisely controlled in real time. The Numerically Controlled Oscillator (NCO) is ideally suited for this purpose. For some applications, the output reference signal is a square wave, so the temptation is to use only the MSB of the NCO output. This is useful in low frequency applications such as motor controllers, but is inadequate for most communications tasks. This is because the zero crossings of this signal can vary by one period of the input clock from one pulse to the next, which creates an unacceptable amount of jitter in the output. For example, if the NCO is clocked at 30MHz, the jitter is 33nsec. For a 1MHz square wave, this results in 12° of phase jitter. The straightforward solution is to use an NCO with a much higher clock rate. This is not cost effective for applications requiring phase jitter of less than 5nsec, however, since it requires a sample rate of 200 Mega Samples Per Second, (MSPS), which drives the user to an ECL NCO.

A much less costly circuit which solves this problem is shown in Figure 1. The output of the comparator is a square wave with much less jitter than the NCO alone. The basic idea is that the sampled sine wave output of the NCO is converted to a smooth sine wave, which is converted back to a square wave with a comparator. In the circuit shown, the comparator drives a filter, which attenuates the odd order harmonics so that the final output of the circuit is a sine wave. The upper limit on the purity of the sine wave is also much better than that of the NCO, as will be seen below.

The primary sources of error in this circuit are:

In the NCO, spurs are classified as either AM or PM. PM spurs are due to truncation of the phase in calculating the sine and cosine. If M = number of bits into the input of the Sine/Cosine Generator, the PM spur level is -6M + 5.17dB[1]. The AM spurs are due to amplitude quantization on the output of the NCO. If the number of NCO output bits is N, the AM spur level is approximately equal to -6.02N - 1.76dB. [1] There will also be jitter due to the clock oscillator driving the

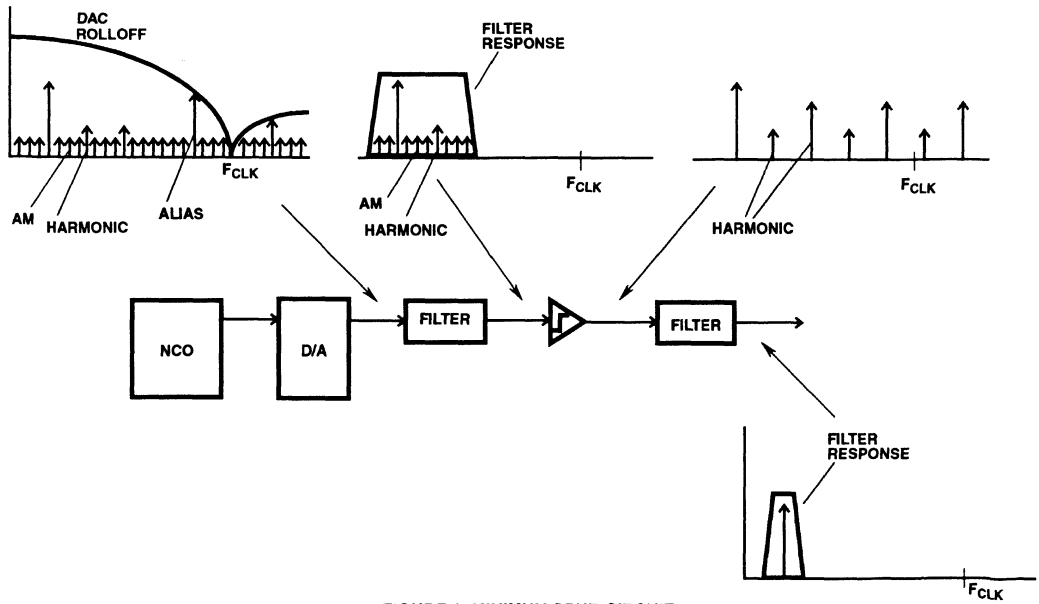


FIGURE 1. MINIMUM SPUR CIRCUIT

NCO, but since it is only the short term jitter, not the long term stability of the oscillator that contributes to phase noise, this will be negligible if a reasonably good oscillator is used.

The DAC introduces additional spurs, which come from three sources: intermodulation spurs due to non-linearities in the DAC; a spur at the clock oscillator frequency due to clock feed-through; and power supply noise. The DAC also faithfully reproduces the aliases and harmonics that are unavoidable products of the NCO due to the digital nature of the output.

The filter on the output of the DAC eliminates the clock feed through, aliases due to the sampled nature of the NCO output and most of the AM spurs are eliminated with the bandpass. Spurs within the pass band are unchanged. The spectrum of the DAC output is a tone surrounded by spurs and noise in the frequency band corresponding to the pass band of the filter with negligible noise elsewhere. The area comprised of the tone, spurs and noise is known as the pedestal.

The input of the comparator is a relatively clean sine wave which the comparator converts into a square wave. This limiting action eliminates the AM spurs but has no effect on the PM spurs. For this reason, the number of bits used on the output of the NCO and the input of the DAC has little measurable effect on the output. The primary contributions to errors on the output of the comparator are the PM spurs on its input, which are passed through relatively unaffected, and power supply noise, which is attenuated by the power supply rejection of the comparator. If the filter on the input of the comparator did not remove the aliases and clock feed through, then the comparator will generate intermodulation components. This makes a good filter and a careful frequency pian essentiai.

If the desired output of the circuit is a sine wave rather than a square wave, the output of the comparator is filtered to extract the fundamental - that is, to suppress the odd order harmonics of the square wave signal. Note that this signal is much cleaner than the output of the first filter, since the comparator has removed the AM spurs.

The circuit shown here is often used to generate the reference tone for an indirect loop PLL synthesizer. In this case, the output of this circuit is fed into one input of a mixer, with the other input of the mixer driven by a high frequency VCO. The output of the mixer is a high frequency tone. The phase noise at the output of the mixer due to the noise in the reference circuit will be equal to the spur level of the reference circuit plus 20*log10(output frequency/NCO frequency). For example, using the 45106 as a 5MHz reference for a 1GHz synthesizer, the spurs on the output of the reference would increase by 20log10(200), so the output spur level would be -114 + 46 = -68dBc at 1GHz. The NCO frequency resolution is 0.008Hz at 33 MSPS, so the tuning resolution of the synthesizer is 200(0.008) = 1.6Hz. Finer resolution can be obtained by cascading the Time Accumulator with the Phase Accumulator. (See below.)

Extended Frequency Resolution

The phase accumulator of the HSP45106 (NCO16) is 32bits wide. This corresponds to a frequency resolution of (Sample Frequency)/2^{32}. For a 25 MSPS sample rate, this results in an output frequency resolution of 0.006Hz. In certain applications, there is a requirement for much greater resolution. The NCO16 can address these applications using the Time Accumulator as an extension of the Phase Accumulator. Frequency resolutions of up to 64bits can be obtained in this configuration. Using the previous example of a 25MHz clock, the frequency resolution is 25MHz/2^{64} = 1.35picoHertz. Using the parts in this configuration requires a small change to the external control logic: the Timer Accumulator register must be loaded over the control bus interface. This mode of operation has no effect on any of the other performance parameters, such as spurious free dynamic range, phase resolution, etc.

To configure the HSP45106 for this application, the setup shown in Figure 2. Note that the Timer Accumulator output, TICO#, is connected to the Phase Accumulator input, PACI#. To set the output frequency of the part, the Center Frequency Register and the Timer Accumulator must be loaded. Assuming that the Offset Register is not used, the equation for calculating the output frequency is now:

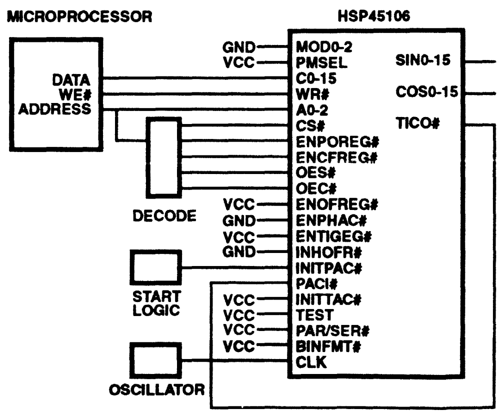


FIGURE 2. EXTENDED FREQUENCY RESOLUTION CIRCUIT

Center Frequency =

CLK Frequency x ((Center Frequency Register / 2^{32})

+ (Timer Accumulator Register / 2^{64})

In this equation, the contents of the value in the Center Frequency Register is a two's complement number, i.e., the part tunes from -(CLK Frequency) / 2 to +(CLK Frequency) / 2. The value in the Timer Accumulator is an unsigned number.

It is unsigned because it provides the carry in to the Phase Accumulator, which is always added to the LSB of the current phase value.

The user should note that there is a flip flop between the Time Accumulator carry out and the TICO# pin, and another flip flop between the PACI# pin and the Phase Accumulator carry input. This will cause a two clock cycle delay between the carry out of the timer into the carry in of the accumulator. This will only have an effect on the output when the frequency register is updated; in effect, the Time Accumulator lags the Phase Accumulator by two clock cycles. If this is a concern, this can be compensated for by loading the input registers for both accumulators, then toggling ENTIREG# two clock cycles before ENCFREG#.

While the internal architecture of the HSP45116 NCOM and the HSP45106 NCO16 are very similar, this application works better with the NCO16 for two reasons. The first is that on the NCO16, the timer is loaded using a unique pin, rather than sharing this function with the ROM bypass line. This means that the output of the NCO16 is always valid, instead of having erroneous results on the output whenever the timer is updated. The second is that with the NCO16, the data for the various registers is downloaded into separate input registers, which can be downloaded into the operating registers with the ENXXREG# pulses. With the NCOM, there is only one 32bit input register, which must be downloaded into the appropriate operating register before the next value can be input into the part. In this application, it means that the user can adjust the phase between the register updates with the NCO16 but not with the NCOM.

Example

The circuit used to verify this equation is shown in Figure 2. The clock oscillator frequency was measured at 25.24102MHz. In order to achieve an output frequency of 1.000000Hz, the center frequency was set to hexadecimal AA, the offset frequency set to 0, and the Timer Accumulator set to hexadecimal 28880000. A frequency counter was attached to bit 15 of the cosine output. The actual frequency out varied from 0.9999999 to 1.0000003 as the oscillator drifted with time. A more stable oscillator would yield more predictable results. Note that going through the calculations results in an output frequency of 1.0000006Hz. The difference is due to the fact that the oscillator frequency measurement was only carried out to 7 digits, but the counter used in this example had 8 digits.

References

[1] Cercas, Francisco A. B., Tomlinson, M and Albuquerque, A. A. Designing with Digital Frequency Synthesizers, Proceedings of RF Expo East, 1990

Harris Semiconductor

Tech Brief

No. TB305 January 1994

Harris Digital Signal Processing

HISTOGRAMMING WITH A VARIABLE PIXEL INCREMENT

The HSP48410 Histogrammer/Accumulating Buffer has several modes; two of these are Histogram mode, in which the part computes the histogram of an input data stream, and bin accumulate mode, in which it computes the totals of a set of rank-ordered data. These operations work on generalized digital data, but for the purposes of this tech brief, image data will be used as an example.

In Histogram mode (Figure 1),the HSP48410 accepts pixel data on the PIN0-9 bus. It uses this information as the address of its internal RAM to compute the number of pixels in an image that are at each gray level. The contents of the RAM at the given address is fed into an adder; the other input of the adder is set to all zeroes except for a one in the LSB. The output of the adder is written back into the RAM in the same location. When all pixels have been processed by the chip, the RAM contains the histogram of the image.

When placed in Bin Accumulate mode (Figure 2), the HSP48410 operates in a similar manner, except that the inputs to the adder come from the RAM and the DIN0-23 input bus. In this mode, the user loads the DIN bus with the desired increment value. Since this is a synchronous input, it can be changed on a pixel by pixel basis. When the operation is finished, the completed histogram will be stored in the RAM as before.

Figure 3 shows an implementation of the latter function using a TMS320 for the system microprocessor. The circuit diagram and timing were derived from the TMS320C25 data sheet and the 1989 Second Generation TMS 320 User's Guide. This circuit has not yet been verified with a physical implementation.

Initially, the part is set to Bin Accumulate mode (FCT = 100). The memory is reset with FC# (Flash Clear) prior to data processing. The input image data is latched into PIN0-9, the histogram increment for that pixel is simultaneously loaded into DIN0-23. The internal pipeline delays align the two sets of data internally so that the proper bit in the histogram is incremented with the right number. The SYNC signal is used to flag the beginning of the new frame of data, and stays low while image data is being fed into the part.

When one frame of image data has been processed, the histogram can be read out of the memory over the microprocessor interface. After the START# pin is brought high, the TMS320 uses the FCT0-2 lines to configure the part for 16 bit Asynchronous mode (FCT = 111). The contents of the bins can now be read out asynchronously to the pixel clock and in random order. START# remains high during this operation.

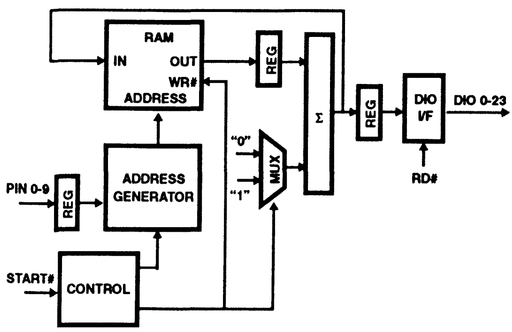


FIGURE 1. HISTOGRAMMER MODE BLOCK DIAGRAM

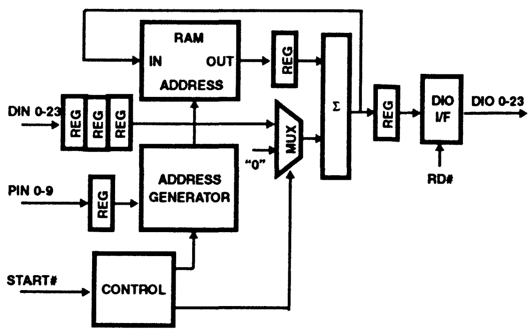


FIGURE 2. BIN ACCUMULATE MODE BLOCK DIAGRAM

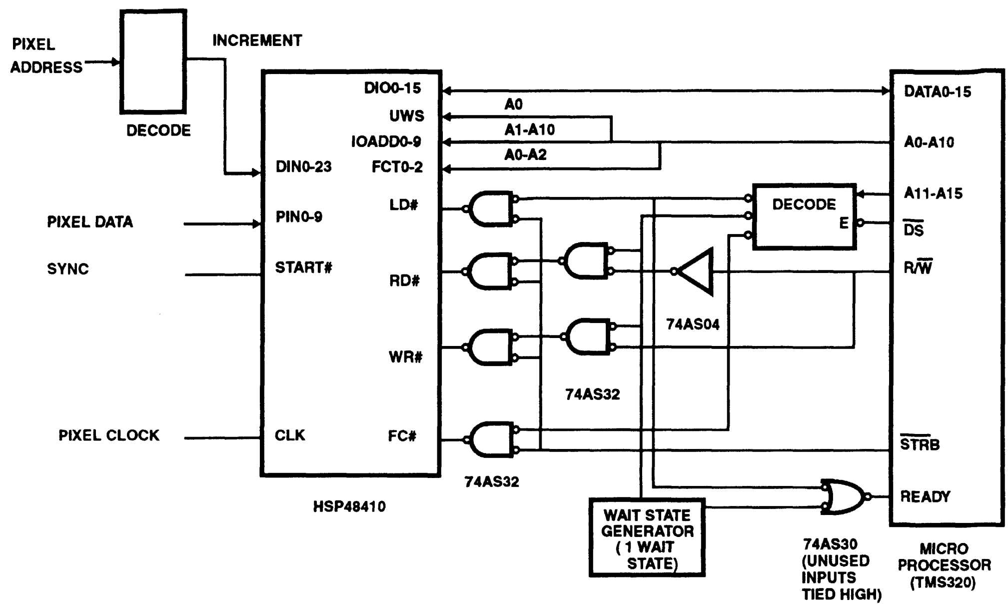


FIGURE 3. HSP48410 CIRCUIT SHOWING INTERFACE TO TMS 320 AND DYNAMIC PIXEL INCREMENT

CASCADING MULTIPLE HSP45256 CORRELATORS

When multiple correlators are cascaded for longer reference data sets, the Programmable Delay is used to adjust the timing between chips so that they can be connected with no external hardware. Figure 1 shows the portions of two correlators that would be active when two 45256's are set up to perform a 1 bit, 512 tap correlation. In this case, DOUT7 of one correlator is connected to DIN7 of the next one; CASOUT0- 12 of the first part are connected to CASIN0-12 of the second one. (See the HSP45256 data sheet.) Figure 2 shows the relevant portions of two Correlators which are cascaded together; in this example, each is configured as 1x256. In the interest of clarity, the only portions shown are the final stage of the first correlator and the first stage of the second one. The data sample number at each stage for a given clock cycle is shown in the boxed in numbers. Note that the Programmable Delay of the first part is set to a delay of one (the minimum possible) and the second part is set to a delay of two. This assures that the proper samples are added in the Cascade Summer.

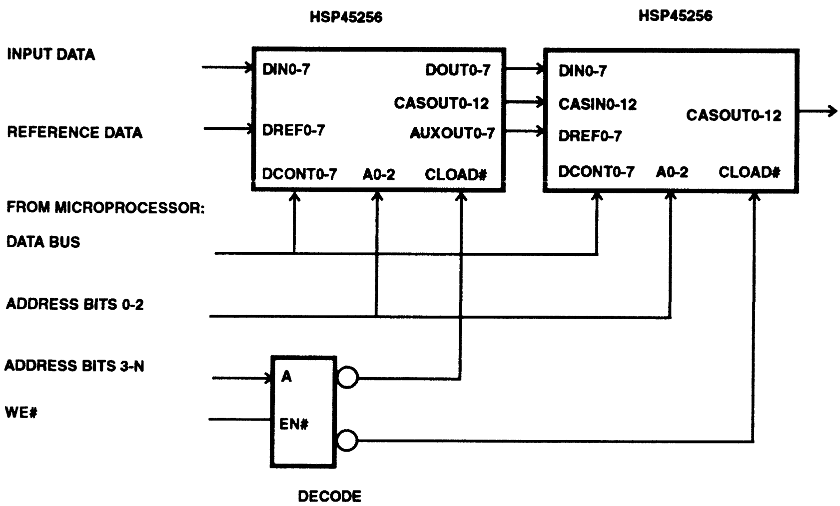


FIGURE 1. CIRCUIT BLOCK DIAGRAM

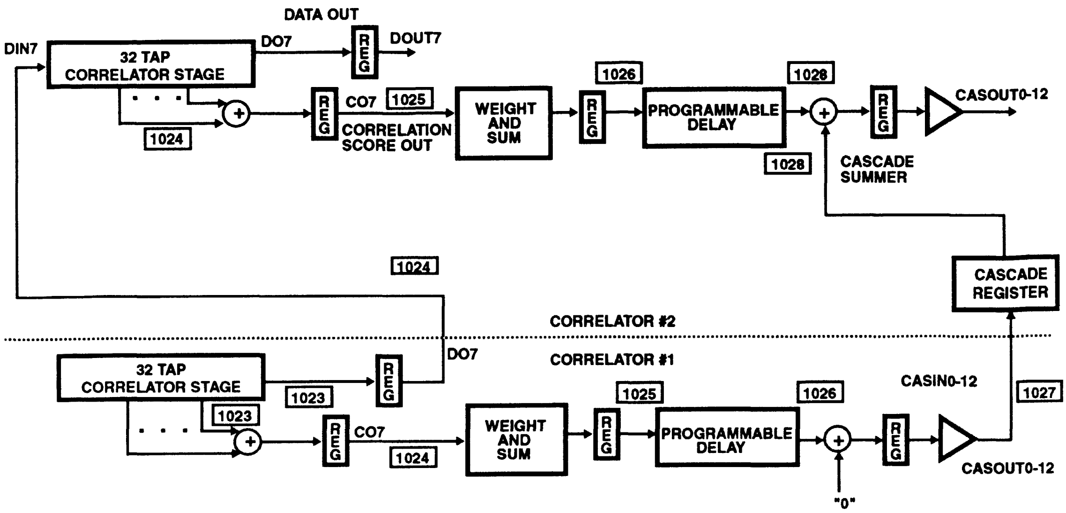


FIGURE 2. CASCADED CORRELATORS SHOWING RELATIVE CLOCK CYCLES.

Harris Semiconductor

TechBrief

No. TB307 January 1994 *Harris Digital Signal Processing*

CORRELATION WITH MULTIBIT DATA USING THE HSP45256

For single bit data, the output of the correlator, that is, the correlation score, represents the total number of data bits that match the reference at time n. At time n+1, the data slides past the reference by one sample, a new data sample is input into the device, and the new sum is calculated. When the data matches the reference most closely, a correlation peak is obtained. Figure 1 shows a stream of data being correlated with a reference and the corresponding peak in the output score.

The maximum possible correlation score (corresponding to a perfect match) equals the number of bits in the data stream. Assuming that the reference pattern occurs only once in the data, the correlation score will build slowly until it reaches the peak. Assuming random input data, most of the time about half of the data samples will match the reference. The minimum correlation score for a given configuration will then be one half of the peak score.

This example is ideal; the received pulse is not corrupted by noise, so correlation is perfect. In the real world, noise on the input data will lower the correlation peak, making it more difficult to determine its position in the data. Quantizing the data using more than one bit helps to alleviate this problem. In the example shown in Figure 2, two bit quantization is used to illustrate this point. In this case, calculation of the maximum possible score must take into account the bit weighting. The output scores are shown normalized to their respective maximums so that a fair comparison is achieved. Note that using more data bits sharpens the peak of the score.

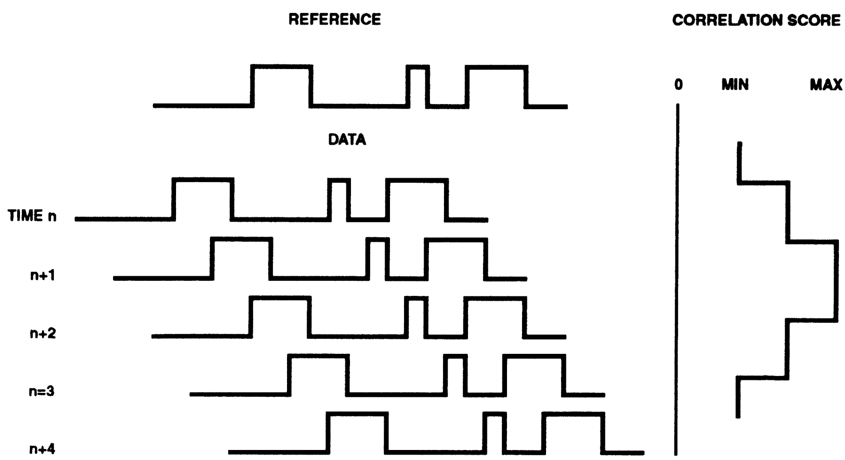
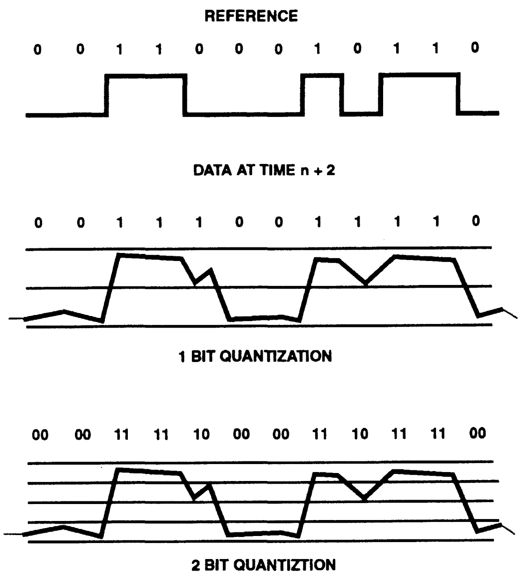


FIGURE 1. CONCEPTUAL DIAGRAM OF CORRELATION OF SINGLE BIT DATA AND REFERENCE

9

AP NOTES AND TECH BRIEFS



CORRELATION SCORE:

1+1+1+1+0 +1+1+1+0+1+1+1 = 10

TOTAL POSSIBLE = 12

10/12 = 0.83

SCORE AT n + 1 = 8/12 = 0.75
SCORE AT n + 3 = 6/12 = 0.50

2 (1+1+1+1+0+1+1+1+0+1+1+1)
+ (1+1+1+1+1+1+1+1+1+1+1+1) = 32

TOTAL POSSIBLE = 36

32/36 = 0.89

SCORE AT n + 1 = 21/36 = 0.58
SCORE AT n + 3 = 18/36 = 0.50

FIGURE 2. COMPARISON OF CORRELATION USING ONE BIT AND TWO BIT DATA

DSP 10

HARRIS QUALITY AND RELIABILITY

Harris Quality

Introduction

Success in the integrated circuit industry means more than simply meeting or exceeding the demands of today's market. It also includes anticipating and accepting the challenges of the future. It results from a process of continuing improvement and evolution, with perfection as the constant goal.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force – from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added on or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of the Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. In addition to facilitating the development of SPC and DOX, Quality professionals support other continuous improvement tools such as control charts, measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs – with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress.

The Improvement Process

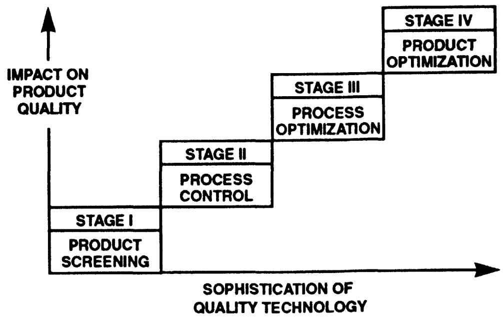


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage III to Stage IV, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

Designing for Manufacturability

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment.

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Wafer Fab	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Junction Depth	X	
	- Sheet Resistivities	X	
	- Defect Density	X	X
	- Critical Dimensions	X	X
	- Visual Inspection	X	X
	- Lot Acceptance	X	
	• Process		
	- Film Thickness	X	X
	- Implant Dosages	X	
	- Capacitance Voltage Changes	X	X
	- Conformance to Specification	X	X
	• Equipment		
	- Repeatability	X	X
	- Profiles	X	X
	- Calibration		X
	- Preventive Maintenance	X	X
Assembly	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Documentation Check		X
	- Dice Inspection	X	X
	- Wire Bond Pull Strength/Controls	X	X
	- Ball Bond Shear/Controls		X
	- Die Shear Controls		X
	- Post-Bond/Pre-Seal Visual	X	X
	- Fine/Gross Leak	X	X
	- PIND Test	X	
	- Lead Finish Visuals, Thickness	X	X
	- Solderability		X
	• Process		
	- Operator Quality Performance	X	X
	- Saw Controls	X	
	- Die Attach Temperatures	X	X
	- Seal Parameters	X	
	- Seal Temperature Profile	X	X
	- Sta-Bake Profile	X	
	- Temp Cycle Chamber Temperature	X	X
	- ESD Protection	X	X
	- Plating Bath Controls	X	X
	- Mold Parameters	X	X

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (Continued)

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Test	• JAN Self-Audit		X
	• Temperature/Humidity	X	
	• ESD Controls	X	
	• Temperature Test Calibration	X	
	• Test System Calibration	X	
	• Test Procedures		X
	• Control Unit Compliance	X	
	• Lot Acceptance Conformance	X	
	• Group A Lot Acceptance		X
Probe	• JAN Self-Audit		X
	• Wafer Repeat Correlation	X	
	• Visual Requirements	X	X
	• Documentation	X	X
	• Process Performance	X	X
Burn-In	• JAN Self-Audit		X
	• Functionality Board Check	X	
	• Oven Temperature Controls	X	
	• Procedural Conformance		X
Brand	• JAN Self-Audit		X
	• ESD Controls	X	X
	• Brand Permanency	X	X
	• Temperature/Humidity	X	
	• Procedural Conformance		X
QCI Inspection	• JAN Self-Audit		X
	• Group B Conformance		X
	• Group C and D Conformance		X

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 2).

TABLE 2. HARRIS I.C. DESIGN TOOLS

DESIGN STEP	PRODUCTS	
	ANALOG	DIGITAL
Functional Simulation	Cds Spice	Cds Spice Verilog
Parametric Simulation	Cds Spice Monte Carlo	Cds Spice
Schematic Capture	Cadence	Cadence
Functional Checking	Cadence	Cadence
Rules Checking	Cadence	Cadence
Parasitic Extraction	Cadence	Cadence

Special Testing

Harris Semiconductor offers several standard screen flows to support a customer's need for additional testing and reliability assurance. These flows include environmental stress testing, burn-in, and electrical testing at temperatures other than +25°C. The flows shown on pages 9-6 and 9-7 indicate the Harris standard processing flows for a Commercial Linear part in PDIP Package. In addition, Harris can supply products tested to customer specifications both for electrical requirements and for nonstandard environmental stress screening. Consult your field sales representative for details.

Harris Semiconductor Standard Processing Flows

Control	Step	COMMERCIAL
HIGH/ROOM TEMP PROBE TEST	PROBE/DICE PREPARATION	VISUAL INSPECTION MODIFIED MIL-STD-883 METHOD 2010 CONDITION B WITH QC MONITOR
	ASSEMBLY (1)	
	■ OPERATION	
	★ QUALITY MONITOR	
DIE ATTACH CONTROL	■ DIE MOUNT	YES
	■ MOUNT CURE CONTROL	YES
	★ QUALITY DIE ATTACH CONTROL (SPC)	YES
WIRE BOND CONTROL	■ WIRE BOND	YES
	★ QUALITY WIRE BOND CONTROL (SPC)	YES
POST BOND VISUAL	■ POST BOND INSPECTION (RTPC)	YES
	★ QUALITY POST BOND INSPECTION	AS APPLICABLE
MOLD CONTROL	■ MOLDING	YES
	■ MOLD CONTROL (SPC)	YES
	■ BOTTOM CODE	YES
	■ POST MOLD CURE	YES
LEAD FINISH CONTROL	■ TRIM/FORM/DERAIL	YES
	■ SINGULATED SOLDER DIP	YES
	■ 100% VISUAL INSPECTION	YES
	■ LOAD SHIPPING TUBES	YES
	★ QA LOT ACCEPTANCE	YES
	★ QA DOCUMENTATION INSPECTION	YES

(1) Example for a PDIP Package Part

Harris Semiconductor Standard Processing Flow (Continued)

TEST (2)

■ OPERATION
★ QUALITY MONITOR

	TEST (2)	COMMERCIAL
AC/DC SINGLE INSERTION TEST CAPABILITY; HIGH/LOW TEMP	■ 100% ELECTRICAL TEST	YES
	■ TOP BRAND	YES
	■ PRE-BURN-IN ELECTRICAL TEST	IF APPLICABLE
BURN-IN	■ BURN-IN	IF APPLICABLE
	■ POST BURN-IN ELECTRICAL TESTS	IF APPLICABLE
	■ APPLY BURN-IN PDA	IF APPLICABLE
QUALITY LOT ACCEPTANCE	★ QC PRESHIP LOT ACCEPTANCE TEST	YES
PDIP LEAD SCANNING	■ 100% LEAD SCANNING	YES
	■ PACKING	YES
	★ QC PRESHIP LOT ACCEPTANCE INSPECTION	YES
	■ FINAL DATA REVIEW	YES

(2) Example for a Linear Part in PDIP Package

TABLE 3. SUMMARIZING CONTROL APPLICATIONS

FAB			
• Diffusion - Junction Depth - Sheet Resistivities - Oxide Thickness - Implant Dose Calibration - Uniformity	• Thin Film - Film Thickness - Uniformity - Refractive Index - Film Composition	• Photo Resist - Critical Dimension - Resist Thickness - Etch Rates	• Measurement Equipment - Critical Dimension - Film Thickness - 4 Point Probe - Ellipsometer
ASSEMBLY			
• Pre-Seal - Die Prep Visuals - Yields - Die Attach Heater Block - Die Shear - Wire Pull - Ball Bond Shear - Saw Blade Wear - Pre-Cap Visuals	• Post-Seal - Internal Package Moisture - Tin Plate Thickness - PIND Defect Rate - Solder Thickness - Leak Tests - Module Rm. Solder Pot Temp. - Seal - Temperature Cycle	• Measurement - XRF - Radiation Counter - Thermocouples - GM-Force Measurement	
TEST			
	- Handlers/Test System - Defect Pareto Charts - Lot % Defective - ESD Failures per Month	- Monitor Failures - Lead Strengthening Quality - After Burn-In PDA	
OTHER			
• IQC - Vendor Performance - Material Criteria - Quality Levels	• Environment - Water Quality - Clean Room Control - Temperature - Humidity	• IQC Measurement/Analysis - XRF - ADE - 4 Point Probe - Chemical Analysis Equipment	

Controlling and Improving the Manufacturing Process - SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use control charts to determine the normal variabilities in processes, materials, and products. Critical process variables and performance characteristics are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that an operation is outside the process control limits or indicates a nonrandom pattern inside the limits. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 3 lists some typical manufacturing applications of control charts at Harris Semiconductor.

SPC is important, but still considered only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost. (See Table 4).

TABLE 4. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

STAGE		APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at reducing the number of defects by studying the key variables controlling the process, and optimizing the procedures or design to yield the best result. This approach is a more time-consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in JEDEC STD 16, MIL-STD-883 and MIL-I-38535 are used by our quality inspectors.

The focus on this quality parameter has resulted in a continuous improvement to less than 100 PPM, and the goal is to continue improvement toward 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of Harris statisticians, private consultants, and internally developed programs, training of engineers, supervisors, and operators/technicians has been an ongoing activity in Harris Semiconductor.

Over the past years, Harris has also deployed a comprehensive training program for hourly operators and supervisors in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

Incoming Materials

Improving the quality and reducing the variability of critical incoming materials is essential to product quality enhancement, yield improvement, and cost control. With the use of statistical techniques, the influence of silicon, chemicals, gases and other materials on manufacturing is highly measurable. Current measurements indicate that results are best achieved when materials feeding a statistically controlled manufacturing line have also been produced by statistically controlled vendor processes.

To assure optimum quality of all incoming materials, Harris has initiated an aggressive program, linking key suppliers with our manufacturing lines. This user-supplier network is the Harris Vendor Certification process by which strategic vendors, who have performance histories of the highest quality, participate with Harris in a lined network; the vendor's factory acts as if it were a beginning of the Harris production line.

SPC seminars, development of open working relationships, understanding of Harris' manufacturing needs and vendor capabilities, and continual improvement programs are all part of the certification process. The sole use of engineering limits no longer is the only quantitative requirement of incoming materials.

TABLE 5. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	TOPICS COVERED
SPC, Basic	Manufacturing Operators, Non-Manufacturing Personnel	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts
SPC, Intermediate	Manufacturing Supervisors, Technicians	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Introduction to Capability
SPC, Advanced	Manufacturing Engineers, Manufacturing Managers	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Advanced Control Charts, Variance Component Analysis, Capability Analysis
Design of Experiments (DOX)	Engineers, Managers	Factorial and Fractional Designs, Blocking Designs, Nested Models, Analysis of Variance, Normal Probability Plots, Statistical Intervals, Variance Component Analysis, Multiple Comparison Procedures, Hypothesis Testing, Model Assumptions/Diagnostics
Regression	Engineers, Managers	Simple Linear Regression, Multiple Regression, Coefficient Interval Estimation, Diagnostic Tools, Variable Selection Techniques
Response Surface Methods (RSM)	Engineers, Managers	Steepest Ascent Methods, Second Order Models, Central Composite Designs, Contour Plots, Box-Behnken Designs

Specified requirements include centered means, statistical control limits, and the requirement that vendors deliver their products from their own statistically evaluated, in-control manufacturing processes.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Taper • Thickness • Total Thickness Variation • Backside Criteria • Oxygen • Carbon	• Equipment Capability Control Charts - Oxygen - Resistivity • Control Charts Related to - Enhanced Gettering - Total Thickness Variation - Total Indicated Reading - Particulates • Certificated of Analysis for all Critical Parameters • Control Charts from On-Line Processing • Certificate of Conformance
Chemicals/Photoresists/ Gases	• Chemicals - Assay - Major Contaminants • Molding Compounds - Spiral Flow - Thermal Characteristics • Gases - Impurities • Photoresists - Viscosity - Film Thickness - Solids - Pinholes	• Certificate of Analysis on all Critical Parameters • Certificate of Conformance • Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Water - Selected Parameters • Control Charts - Assay - Contaminants • Control Charts on - Photospeed - Thickness - UV Absorbance - Filterability - Water - Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Dimensional Characteristics • Certificate of Analysis for all Critical Parameters • Certificate of Conformance
Assembly Materials	• Visual Inspection • Physical Dimension Checks • Glass Composition • Bondability • Intermetallic Layer Adhesion • Ionic Contaminants • Thermal Characteristics • Lead Coplanarity • Plating Thickness • Hermeticity	• Certificate of Analysis • Certificate of Conformance • Process Control Charts on Outgoing Product Checks and In-Line Process Controls

Calibration Laboratory

Another important resource in the product assurance system is a calibration lab in each Harris Semiconductor operation site. These labs are responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both production and engineering areas. The accuracy of instruments used at Harris is traceable to a national standards. Each lab maintains a system which conforms to the current revision of MIL-STD-45662, "Calibration System Requirements."

Each instrument requiring calibration is assigned a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Manufacturing Science - CAM, JIT, TPM

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened - in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Just In Time (JIT)

The major focus of JIT is cycle time reduction and linear production. Significant improvements in these areas result in large benefits to the customer. JIT is a part of the Total Quality Management philosophy at Harris and includes Employee Involvement, Total Quality Control, and the total elimination of waste.

Some key JIT methods used for improvement are sequence of events analysis for the elimination of non-value added activities, demand/pull to improve production flow, TQC check points and Employee Involvement Teams using root cause analysis for problem solving.

JIT implementations at Harris Semiconductor have resulted in significant improvements in cycle time and linearity. The benefits from these improvements are better on time delivery, improved yield, and a more cost effective operation.

JIT, SPC, and TPM are complementary methodologies and used in conjunction with each other create a very powerful force for manufacturing improvement.

Total Productive Maintenance (TPM)

TPM or Total Productive Maintenance is a specific methodology which utilizes a definite set of principles and tools focusing on the improvement of equipment utilization. It focuses on the total elimination of the six major losses which are equipment failures, setup and adjustment, idling and minor stoppages, reduced speed, process defects, and reduced yield. A key measure of progress within TPM is the overall equipment effectiveness which indicates what percentage of the time is a particular equipment producing good parts. The basic TPM principles focus on maximum equipment utilization, autonomous maintenance, cross functional team involvement, and zero defects. There are some key tools within the TPM technical set which have proven to be very powerful to solve long standing problems. They are initial clean, P-M analysis, condition based maintenance, and quality maintenance.

Utilization of TPM has shown significant increases in utilization on many tools across the Sector and is rapidly becoming widespread and recognized as a very valuable tool to improve manufacturing competitiveness.

The major benefits of TPM are capital avoidance, reduced costs, increased capability, and increased quality. It is also very compatible with SPC techniques since SPC is a good stepping stone to TPM implementation and it is in turn a good stepping stone to JIT because a high overall equipment effectiveness guarantees the equipment to be available and operational at the right time as demanded by JIT.

Harris Reliability

The reliability operations for Harris Semiconductor are consolidated into three locations; in Palm Bay, Florida, and Research Triangle Park, North Carolina, for integrated circuits products, and Mountaintop, Pennsylvania for Power Discrete Products. This consolidation brought the reliability organizations together to form a team that possesses a broad cross section of expertise in:

- Custom Military
- Automotive ASICs
- Harsh Environment Plastic Packaging
- Advanced Methods for Design for Reliability (DFR)
- Strength in Power Semiconductor
- Chemical/Surface Analysis Capabilities

The reliability focus is customer satisfaction (external and internal) and is accomplished through the development of standards, performance metrics and service systems. These major systems are summarized below:

- A process and product development system which emphasizes getting new products to market over product design. Uses empowered cross functional development teams.
- Standard test vehicles (96 in all) for process characterization of wearout failure mechanisms using conventional stresses (for modeling FITs/MTTF) and wafer level reliability characterization during development.
- Common qualification standards and philosophy for all sites and developments.
- Matrix monitor standard - a reliability monitoring system for products in production to insure ongoing reliability and verification of continuous improvement.
- Field return failure analysis system deployed world wide to track and expedite root cause analysis and irreversible corrective actions in a timely manner for our customers. The system is called by the team name PFAST, Product Failure Analysis Solution Team. Failure analysis sites are located in Brussels, Mountaintop, Palm Bay, Singapore, Kuala Lumpur, and Tokyo. In order to optimize our response time to the customer all locations are networked for optimum communication, trend analysis, and performance tracking.

Integrated circuits reliability home base is in Palm Bay, Florida. This new facility has consolidated the reliability organization of the standard products divisions reliability group from Palm Bay, Florida; Somerville, New Jersey; Santa Clara, California, and the Military and Aerospace Division in Palm Bay, Florida. This facility contains

- A 9,000 square foot reliability analysis laboratory,
- An 8,000 square foot reliability stress testing facility,
- A 5,000 square foot analytical (chemistry/surface analysis) laboratory,
- A 3,000 square foot of engineering office space.

The facilities are well equipped and manned with highly trained and disciplined analysts. The reliability facilities are JAN certified and certified by a host of customers including major automotive and telecommunications companies.

Process/Product/Package Qualifications

Qualification activities at Harris begin with the in-depth qualification of new wafer processes. These process qualifications focus on the use of test vehicles to characterize wearout mechanisms for each process. These data are used to establish design ground rules for each process to eliminate wearout failure during the useful life of the product. Products designed within the established ground rules are qualified individually prior to introduction. New package configurations are qualified individually prior to being available for new products. Harris qualification procedures are specified via controlled documentation.

Product/Package Reliability Monitors

Many of the accelerated stress-tests used during initial reliability qualification are also employed during the routine monitoring of standard production product. Harris' continuing reliability monitoring program consists of three groups of stress tests, labeled Matrix I, II and III. As an example, Table 7 outlines the Matrix tests used to monitor plastic packaged CMOS Logic ICs in Harris' Malaysia assembly plant, where each wafer fab technology is sampled weekly for both Matrix I and II. Matrix I consists of highly accelerated, short duration (48 hours or less) tests, which provide real-time feedback on product reliability. Matrix II consists of the more traditional, longer term stress-tests, which are similar to those used for product qualification. Finally, Matrix III, performed monthly on each package style, monitors the mechanical reliability aspects of the package. Any failures occurring on the Matrix monitors are fully analyzed and the failure mechanisms identified, with corrective actions obtained from Manufacturing and Engineering. This information along with all of the test results are routinely transmitted to a central data base in Reliability Engineering, where failure rate trends are analyzed and tracked on an ongoing basis. These data are used to drive product improvements, so as to ensure that failure rates are continuously being reduced over time.

TABLE 7. PLASTIC PACKAGED CMOS LOGIC ICS MALAYSIA RELIABILITY MONITORING TESTS.

MATRIX I

TEST	CONDITIONS	DURATION	SAMPLE
Bias Life	+175°C	48 Hours	40
HAST	+145°C, 85% RH	20 Hours	40

TABLE 7. PLASTIC PACKAGED CMOS LOGIC ICS MALAYSIA RELIABILITY MONITORING TESTS (Continued)

MATRIX II

TEST	CONDITIONS	DURATION	SAMPLE
Bias Life	+125°C	1000 Hours	50
Dynamic Life	+125°C	1000 Hours	50
Biased Humidity	+85°C, 85% RH	1000 Hours	50
Autoclave	15 PSIG, +121°C, 100% RH	192 Hours	50
Storage Life	+150°C	1000 Hours	50
Temp. Cycle	-65°C to +150°C	1000 Cycles	50
Thermal Shock	-65°C to +150°C	1000 Cycles	50

MATRIX III

TEST	CONDITIONS	SAMPLE
Solderability	MIL-STD 883/2003	15
Lead Fatigue	MIL-STD 883/2004	15
Brand Adhesion	MIL-STD 883/2015	20
Flammability	(UL-94 Vertical Burn)	5

Field Return Product Analysis System

The purpose of this system is to enable Harris' Field Sales and Quality operations to properly route, track and respond to our customers' needs as they relate to product analysis.

The Product Failure Analysis Solution Team (PFAST) consists of the group of people who must act together to provide timely, accurate and meaningful results to customers on units returned for analysis. This team includes the salesman or applications engineer who gets the parts from the customer, the PFAST controller who coordinates the response, the Product or Test Engineering people who obtain characterization and/or test data, the analysts who failure analyze the units, and the people who provide the ultimate corrective action. It is the coordinated effort of this team, through the system described in this document that will drive the Customer responsiveness and continuous improvement that will keep Harris on the forefront of the semiconductor business.

The system and procedures define the processing of product being returned by the customer for analysis performed by Product Engineering, Reliability Failure Analysis and/or Quality Engineering. This system is designed for processing "sample" returns, not entire lot returns or lot replacements.

The philosophy is that each site analyzes its own product. This applies the local expertise to the solutions and helps toward the goal of quick turn time.

Goals: quick, accurate response, uniform deliverable (consistent quality) from each site, traceability.

The PFAST system is summarized in the following steps:

1) Customer calls the sales rep about the unit(s) to return.
2) Fill out PFAST Action Request - see the PFAST form in this section. This form is all that is required to process a Field Return of samples for failure analysis. This form contains essential information necessary to perform root cause analysis. (See Figure 2).
3) The units must be packaged in a manner that prevents physical damage and prevents ESD. Send the units and PFAST form to the appropriate PFAST controller. This location can be determined at the field sales office or rep using "look-up""tables in the PFAST document.
4) The PFAST controller will log the units and route them to ATE testing for data log.
5) Test results will be reviewed and compared to customer complaint and a decision will be made to route the failure to the appropriate analytical group.
6) The customer will be contacted with the ATE test results and interim findings on the analysis. This may relieve a line down situation or provide a rapid disposition of material. The customer contact is valuable in analytical process to insure root cause is found.
7) A report will be written and sent directly to the customer with copies to sales, rep, responsible individuals with corrective actions and to the PFAST controller so that the records will capture the closure of the cycle.
8) Each report will contain a feedback form (stamped and preaddressed) so that the PFAST team can assess their performance based on the customers assessment of quality and cycle time.
9) The PFAST team objectives are to have a report in the customers hands in 28 days, or 14 days based on agreements. Interim results are given real-time.

HARRIS SEMICONDUCTOR

Request # ________
Customer Analysis # ________

PFAST ACTION REQUEST

Date: ________

ORIGINATOR ________	CUSTOMER ________
LOCATION/PHONE NO. ________	LOCATION ________
DEVICE TYPE/PART NO. ________	PURCHASE ORDER NO. ________
NO. SAMPLES RETURNED ________	QUANTITY RECEIVED ________

THE COMPLETENESS AND TIMELY RESPONSE OF THE EVALUATION IS DIRECTLY RELATED TO THE COMPLETENESS OF THE DATA PROVIDED. PLEASE PROVIDE ALL PERTINENT DATA. ATTACH ADDITIONAL SHEETS IF NECESSARY.

TYPE OF PROBLEM

1. ☐ INCOMING INSPECTION
   - ☐ 100% SCREEN ☐ SAMPLE INSPECTION
   - NO. TESTED _____ NO. OF REJECTS _____
   - ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS? ☐ YES ☐ NO
   - ☐ BRIEF DESCRIPTION OF EVALUATION AND RESULTS ATTACHED
2. ☐ IN PROCESS/MANUFACTURING FAILURE
   - ☐ BOARD CHECKOUT ☐ SYSTEM CHECKOUT
   - ☐ FAILED ON TURN-ON
   - ☐ FAILED AFTER _____ HOURS OPERATION
   - WAS UNIT RETESTED UNDER INCOMING INSPECTION CONDITIONS? ☐ YES ☐ NO
   - ☐ BRIEF DESCRIPTION OF HOW FAILURE WAS ISOLATED TO COMPONENT ATTACHED
3. ☐ FIELD FAILURE
   - FAILED AFTER _____ HOURS OPERATION
   - ESTIMATED FAILURE RATE _____% PER 1000 HOURS
   - END USER ________ LOCATION ________
   - AMBIENT TEMPERATURE ________C
   - MIN. _____ C MAX. _____ C
   - REL. HUMIDITY ________%
   - ☐ END USER FAILURE CORRESPONDENCE ATTACHED

ACTION REQUESTED BY CUSTOMER

SPECIFIC ACTION REQUESTED ________

____

IMPACT OF FAILED UNITS ON CUSTOMER'S SITUATION: ________

____

____

CUSTOMER CONTACTS WITH SPECIFIC KNOWLEDGE OF REJECTS

NAME ________

POSITION ________ PHONE ________

DETAILS OF REJECT

(Where appropriate serialize units and specify for each)

TEST CONDITIONS RELATING TO FAILURE
- ☐ TESTER USED (MFGR/MODEL) ________
- ☐ TEST TEMPERATURE ________
- ☐ TEST TIME: ☐ CONTINUOUS TEST ☐ ONE SHOT (T = _____ SEC)
- ☐ DESCRIPTION OF ANY OBSERVED CONDITION TO WHICH FAILURE APPEARS SENSITIVE: ________

1. ☐ DC FAILURES
   - ☐ OPENS ☐ SHORTS ☐ LEAKAGE ☐ STRESS
   - ☐ POWER DRAIN ☐ INPUT LEVEL ☐ OUTPUT LEVEL
   - ☐ LIST OF FORCING CONDITIONS AND MEASURED RESULTS FOR EACH PIN IS ATTACHED
   - ☐ POWER SUPPLY SEQUENCING ATTACHED
2. ☐ AC FAILURES
   - LIST FAILING CHARACTERISTICS ________
   - ADDRESS OF FAILING LOCATION (IF APPLICABLE) ________
   - ATTACHED:
     - ☐ LIST OF POWER SUPPLY AND DRIVER LEVELS (Include pictures of waveforms).
     - ☐ LIST OF OUTPUT LEVELS AND LOADING CONDITIONS
     - ☐ INPUT AND OUTPUT TIMING DIAGRAMS
     - ☐ DESCRIPTION OF PATTERNS USED (If not standard patterns, give very complete description including address sequence).
3. ☐ PROM PROGRAMMING FAILURES
   - ADDRESS OF FAILURES ________
   - PROGRAMMER USED (MFG/MODEL/REV. NO.) ________
4. ☐ PHYSICAL/ASSEMBLY RELATED FAILURES
   - ☐ SEE COMMENTS BELOW ☐ SEE ATTACHED

Additional Comments:

FIGURE 2. PFAST ACTION REQUEST

INSTRUCTIONS FOR COMPLETING PFAST ACTION REQUEST FORM

The purpose of this form is to help us provide you with a more accurate, complete, and timely response to failures which may occur. Accurate and complete information is essential to ensure that the appropriate corrective action can be implemented. Due to this need for accurate and complete information, requests without a completed PFAST Action Request form will be returned.

Source of Problem:
This section requests the product flow leading to the failure. Mark an "X" in the appropriate boxes up to and including the step which detected the failure. Also mark an "X" in the appropriate box under ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS? to indicate whether this is a rare failure or a repeated problem.

Example 1. No incoming electrical test was performed, the units were installed onto boards, the boards functioned correctly for two hours and then 1 unit failed. The customer rarely has a failure due to this Harris device.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE ____________
2. INCOMING TEST ■ NOT PERFORMED
   ☐ 100% TESTED ☐ SAMPLE TESTED
   NO. TESTED _____ NO. OF REJECTS _____
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ■ BOARD TEST ☐ SYSTEM TEST
   HOW MANY UNITS FAILED? 1
   FAILED AFTER 2 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ■ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ■ NO
4. FIELD FAILURE
   FAILED AFTER _____ HOURS OPERATION
   ESTIMATED FAILURE RATE _____% PER _______
   END USER _________ LOCATION _________
   MIN. _____°C AVE. _____°C MAX. _____°C
5. OTHER ____________

Example 2. 100 out of the 500 units shipped were tested at incoming and all passed. The units were installed into boards and the boards passed. The boards were installed into the system and the system failed immediately when turned on. There were 3 system failures due to this part. The customer frequently has failures of this Harris device. The 3 units were not retested at incoming.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE ____________
2. INCOMING TEST ☐ NOT PERFORMED
   ☐ 100% TESTED ■ SAMPLE TESTED
   NO. TESTED 100 NO. OF REJECTS 0
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ■ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ■ BOARD TEST ■ SYSTEM TEST
   HOW MANY UNITS FAILED? 3
   FAILED AFTER 0 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ■ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ■ YES ☐ NO
4. FIELD FAILURE
   FAILED AFTER _____ HOURS OPERATION
   ESTIMATED FAILURE RATE _____% PER _______
   END USER _________ LOCATION _________
   MIN. _____°C AVE. _____°C MAX. _____°C
5. OTHER ____________

Action Requested by Customer:
This section should be completed with the customer's expectations. This information is essential for an appropriate response.

Reason for Electrical Reject:
This section should be completed if the type of failure could be identified. If this information is contained in attached customer correspondence there is no need to transpose onto the PFAST Action Request form.

PFAST REQUIREMENTS

The value of returning failing products is in the corrective actions that are generated. Failure to meet the following requirements can cause an erroneous conclusion and corrective action; therefore, failure to meet these requirements will result in the request being returned. Contact the local PFAST Coordinator if you have any questions.

Units with conformal coating should include the coating manufacturer and model. This is requested since the coating must be removed in order to perform electrical or hermeticity testing.

1) Units must be returned with proper ESD protection (ESD-safe shipping tubes within shielding box/bag or inserted into conductive foam within shielding box/bag). No tape, paper bags, or plastic bags should be used. This requirement ensures that the devices are not damaged during shipment back to Harris.

2) Units must be intact (lid not removed and at least part of each package lead present). This requirement is in place since the parts must be intact in order to perform electrical test. Also, opening the package can remove evidence of the cause for failure and lead to an incorrect conclusion.

3) Programmable parts (ROMs, PROMS, UVEPROMs, and EEPROMs) must include a master unit with the same pattern. This requirement is to provide the pattern so all failing locations can be identified. A master unit is required if a failure analysis is requested.

FIGURE 2. PFAST ACTION REQUEST (Continued)

Failure Analysis Laboratory

The Failure Analysis Laboratory's capabilities encompass the isolation and identification of all failure modes/failure mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. Research vital to understanding the basic physics of the failure is also undertaken.

Failure analysis is a method of enhancing product reliability and determining corrective action. It is the final and crucial step used to isolate potential reliability problems that may have occurred during reliability stressing. Accurate analysis results are imperative to assess effective corrective actions. To ensure the integrity of the analysis, correlation of the failure mechanism to the initial electrical failure is essential.

A general failure analysis procedure has been established in accordance with the current revision of MIL-STD-883, Section 5003. The analysis procedure was designed on the premise that each step should provide information on the failure without destroying information to be obtained from subsequent steps. The exact steps for an analysis are determined as the situation dictates. (See Figures 3 and 4). Records are maintained by laboratory personnel and contain data, the failure analyst's notes, and the formal Product Analysis Report.

Analytical Services Laboratory

Harris facilities, engineering, manufacturing, and product assurance are supported by the Analytical Services Laboratory. Organized into chemical or microbeam analysis methodology, staff and instrumentation from both labs cooperate in fully integrated approaches necessary to complete analytical studies. The capabilities of each area are shown below.

SPECTROSCOPIC METHODS: Colorimetry, Optical Emission, Ultraviolet Visible, Fourier Transform-Infrared, Flame Atomic Absorption, Furnace Organic Carbon Analyzer, Mass Spectrometer.

CHROMATOGRAPHIC METHODS: Gas Chromatography, Ion Chromatography.

THERMAL METHODS: Differential Scanning Colorimetry, Thermogravimetric Analysis, Thermomechanical Analysis.

PHYSICAL METHODS: Profilometry, Microhardness, Rheometry.

CHEMICAL METHODS: Volumetric, Gravimetric, Specific Ion Electrodes.

ELECTRON MICROSCOPE: Transmission Electron Microscopy, Scanning Electron Microscope.

X-RAY METHODS: Energy Dispersive X-ray Analysis (SEM), Wavelength Dispersive X-ray Analysis (SEM), X-ray Fluorescence Spectrometry, X-ray Diffraction Spectrometry.

SURFACE ANALYSIS METHODS: Scanning Auger Microprobe, Electron Spectroscopy/Chemical Analysis, Secondary Ion Mass Spectrometry, Ion Scattering Spectrometry, Ion Microprobe.

The department also maintains ongoing working arrangements with commercial, university, and equipment manufacturers' technical service laboratories, and can obtain any materials analysis in cases where instrumental capabilities are not available in our own facility.

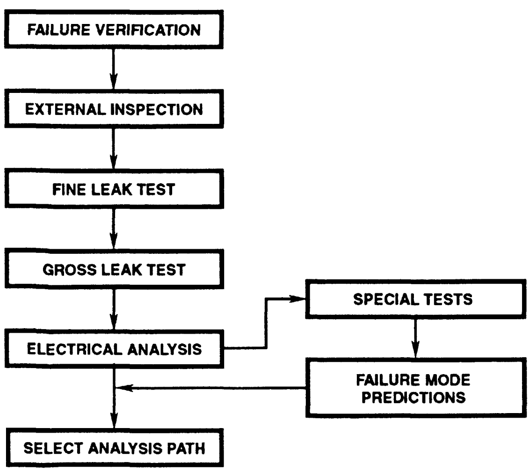


FIGURE 3. NON-DESTRUCTIVE

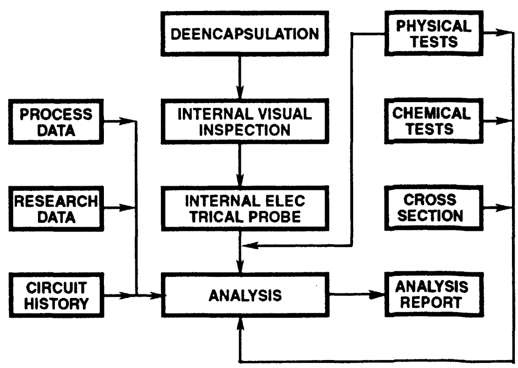


FIGURE 4. DESTRUCTIVE

Reliability Fundamentals and Calculation of Failure Rate

Table 8 below defines some of the more important terminology used in describing the lifetime of integrated circuits.

Of prime importance is the concept of "failure rate" and the calculation thereof.

Failure Rate Calculations

Reliability data may be composed of several different failure mechanisms and the combining of potentially diverse failure rates into one comprehensive failure rate is desired. The failure rate calculation is complicated because the failure mechanisms are thermally activated at differing rates. Additionally, this data is usually obtained on a number of life tests performed at unique stress temperatures. The equation below accounts for these considerations along with a statistical factor to obtain the upper confidence level (UCL) for the resulting failure rate.

$$\lambda = \left[\sum_{i=1}^{\beta} \frac{x_i}{\sum_{j=1}^{k} TDH_j \, AF_{ij}} \right] \bullet \frac{M \times 10^9}{\sum_{i=1}^{\beta} x_i}$$

where,

λ = failure rate in FITs (Number fails in 10^9 device hours)

β = # of distinct possible failure mechanisms

k = # of life tests being combined

x_i = # of failures for a given failure mechanism $i = 1, 2, \ldots \beta$

TDH_j = Total device hours of test time (unaccelerated) for Life Test j, $j = 1, 2, 3, \ldots k$

AF_{ij} = Acceleration factor for appropriate failure mechanism $i = 1, 2, \ldots k$

$$M = \frac{X^2(\alpha, 2r+2)}{2}$$

where,

X^2 = chi square factor for 2r + 2 degrees of freedom

r = total number of failures (Σx_i)

α = risk associated with UCL;
i.e. α = (100-UCL(%))/100

In the failure rate calculation, Acceleration Factors (AFij) are used to derate the failure rate from the thermally accelerated life test conditions to a failure rate indicative of actual use temperature. Although no standard exists, a temperature of +55°C has been popular. Harris Semiconductor Reliability Reports will derate to +55°C and will express failure rates at 60% UCL. Other derating temperatures and UCLs are available upon request.

TABLE 8. FAILURE RATE PRIMER

TERMS	DEFINITIONS/DESCRIPTION
Failure Rate λ	Measure of failure per unit of time. The failure rate typically decreases slightly over early life, and then becomes relatively constant over time. The on set of wearout will show an increasing failure rate, which should occur well beyond useful life. The useful life failure rate is based on the exponential life distribution
FIT (Failure In Time)	Measure of failure rate in 10^9 device hours; e.g., 1 FIT = 1 failure in 10^9 device hours, 100 FITS = 100 failure in 10^9 device hours, etc.
Device Hours	The summation of the number of units in operation multiplied by the time of operation.
MTTF (Mean Time To Failure)	Mean of the life distribution for the population of devices under operation or expected lifetime of an individual, MTTF = $1/\lambda$, which is the time where 63.2% of the population has failed. Exampled: For λ = 10 FITS (or 10 E-9/Hr.), MTTF = $1/\lambda$ = 100 million hours.
Confidence Level (or Limit)	Probability level at which population failure rate estimates are derived from sample life test: 10 FITs at 95% UCL means that the population failure rate is estimated to be no more than 10 FITs with 95% certainty. The upper limit of the confidence interval is used.
Acceleration Factor (AF)	A constant derived from experimental data which relates the times to failure at two different stresses. The AF allows extrapolation of failure rates from accelerated test conditions to use conditions.

Acceleration Factors

Acceleration factor is determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and has been found to be an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP\left[\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)\right]$$

where,

AF = Acceleration Factor

E_a = Thermal Activation Energy (See Table 9)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

Both T_{use} and T_{stress} (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature.

Activation Energy

The Activation Energy (E_a) of a failure mechanism is determined by performing at least two tests at different levels of stress (temperature and/or voltage). The stresses will provide the time to failure (t_f) for the two (or more) populations thus allowing the simultaneous solution for the activation energy as follows:

$$\ln(t_{f1}) = C + \frac{E_a}{kT_1} \qquad \ln(t_{f2}) = C + \frac{E_a}{kT_2}$$

By subtracting the two equations, and solving for the activation energy, the following equation is obtained:

$$E_a = \frac{k\,[\ln(t_{f1}) - \ln(t_{f2})]}{(1/T1 - 1/T2)}$$

where,

E_a = Thermal Activation Energy (See Table 9)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

T_1, T_2 = Life test temperatures in degrees Kelvin

TABLE 9. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3 - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3 - 0.5eV	HTOL & voltage stress screens.	Vendor statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress testing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5 - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistical Process Control of assembly processes, proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles, Statistical Process Control of photoresist/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test and HTOL.	Statistical Process Control of C-V data, oxide/interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL & oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

ELECTROSTATIC DISCHARGE CONTROL A GUIDE TO HANDLING INTEGRATED CIRCUITS

This paper discusses methods and materials recommended for protection of ICs against ESD damage or degradation during manufacturing operations vulnerable to ESD exposure. Areas of concern include dice prep and handling, dice and package inspection, packing, shipping, receiving, testing, assembly and all operations where ICs are involved.

All integrated circuits are sensitive to electrostatic discharge (ESD) to some degree. Since the introduction of integrated circuits with MOS structures and high quality junctions, safe and effective means of handling these devices have been of primary importance.

If static discharge occurs at a sufficient magnitude, 2kV or greater, some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10kV in a low humidity environment; thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. Avoiding any damage or degradation by ESD when handling devices during the manufacturing flow is therefore essential.

ESD Protection and Prevention Measures

One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existence in the industry.

In areas where ICs are being handled, certain equipment should be utilized to reduce the damaging effects of ESD. Typically, equipment such as grounded work stations, conductive wrist straps, conductive floor mats, ionized air blowers and conductive packaging materials are included in the IC handling environment. Any time an individual intends to handle an IC, in any way, they must insure they have been grounded to eliminate circuit damage.

Grounding personnel can, practically, be performed by two methods. First, grounded wrist straps which are usually made of a conductive material, such as Velostat or metal. A resistor value of 1 megohm (1/2 watt) in series with the strap to ground completes a discharge path for ESD when the operator wears the strap in contact with the skin. Another method is to insure direct physical contact with a grounded, conductive work surface.

This consists of a conductive surface like Velostat, covering the work area. The surface is connected to a 1 megohm (1/2 watt) resistor in series with ground.

In addition to personnel grounding, areas where work is being performed with ICs, should be equipped with an ionized air blower. Ionized air blowers force positive and negative ions simultaneously over the work area so that any nonconductors that are near the work surface would have their static charge neutralized before it would cause device damage or degradation.

Relative humidity in the work area should be maintained as high as practical. When the work environment is less than 40% RH, a static build-up condition can exist on nonconductors allowing stored charges to remain near the ICs causing possible static electricity discharge to ICs.

Integrated circuits that are being shipped or transported require special handling and packaging materials to eliminate ESD damage. Dice or packaged devices should be in conductive carriers during all phases of transport and handling. Leads of packaged devices can be shorted by tubular metalic carriers, conductive foam or foil.

Do's and Don'ts for Integrated Circuit Handling

Do's

Do keep paper, nonconductive plastic, plastic foams and films or cardboard off the static controlled conductive bench top. Placing devices, loaded sticks or loaded burn-in boards on top of any of these materials effectively insulates them from ground and defeats the purpose of the static controlled conductive surface.

Do keep hand creams and food away from static controlled conductive work surfaces. If spilled on the bench top, these materials will contaminate and increase the resistivity of the work area.

Do be especially careful when using soldering guns around conductive work surfaces. Solder spills and heat from the gun may melt and damage the conductive mat.

Do check the grounded wrist strap connections daily. Make certain they are snugly fitted before starting work with the product.

Do put on grounded wrist strap before touching any devices. This drains off any static build-up from the operator.

Do know the ESD caution symbols.

Do remove devices or loaded sticks from shielding bags only when grounded via wrist strap at grounded work station. This also applies when loading or removing devices from the antistatic sticks or the loading on or removing from the burn-in boards.

Do wear grounded wrist straps in direct contact with the bare skin never over clothing.

Do use the same ESD control with empty burn-in boards as with loaded boards if boards contain permanently mounted ICs as part of driver circuits.

Do insure electrical test equipment and solder irons at an ESD control station are grounded and only uninsulated metal hand tools be used. Ordinary plastic solder suckers and other plastic assembly aids shall not be used.

Do use ionizing air blowers in static controlled areas when the use of plastic (nonconductive) materials cannot be avoided.

Don'ts

Don't allow anyone not grounded to touch devices, loaded sticks or loaded burn-in boards. To be grounded they must be standing on a conductive floor mat with conductive heel straps attached to footwear or must wear a grounded wrist strap.

Don't touch the devices by the pins or leads unless grounded since most ESD damage is done at these points.

Don't handle devices or loaded sticks during transport from work station to work station unless protected by shielding bags. These items must never be directly handled by anyone not grounded.

Don't use freon or chlorinated cleaners at a grounded work area.

Don't wax grounded static controlled conductive floor and bench top mats. This would allow build-up of an insulating layer and thus defeating the purpose of a conductive work surface.

Don't touch devices or loaded sticks or loaded burn-in boards with clothing or textiles even though grounded wrist strap is worn. This does not apply if conductive coats are worn.

Don't allow personnel to be attached to hard ground. There must always be 1 megohm series resistance (1/2 watt between the person and the ground).

Don't touch edge connectors of loaded burn-in boards or empty burn-in boards containing permanently mounted driver circuits when not grounded. This also applies to burn-in programming cards containing ICs.

Don't unload stick on a metal bench top allowing rapid discharge of charged devices.

Don't touch leads. Handle devices by their package even though grounded.

Don't allow plastic "snow or peanut" polystyrene foam or other high dielectric materials to come in contact with devices or loaded sticks or loaded burn-in boards.

Don't allow rubber/plastic floor mats in front of static controlled work benches.

Don't solvent-clean devices when loaded in antistatic sticks since this will remove antistatic inner coating from sticks.

Don't use antistatic sticks for more than one throughput process. Used sticks should not be reused unless recoated.

Recommended Maintenance Procedures

Daily:

Perform visual inspection of ground wires and terminals on floor mats, bench tops, and grounding receptacles to ensure that proper electrical connections via 1 megohm resistor (1/2 watt) exist.

Clean bench top mats with a soft cloth or paper towel dampened with a mild solution of detergent and water.

Weekly:

Damp mop conductive floor mats to remove any accumulated dirt layer which causes high resistivity.

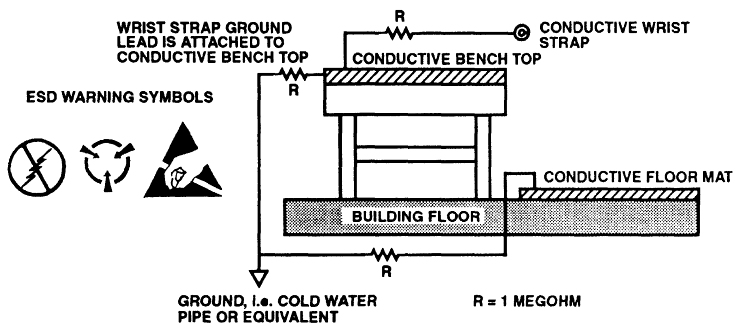
Annually:

Replace nuclear elements for ionized air blowers.

Review ESD protection procedures and equipment for updating and adequacy.

Static Controlled Work Station

The figure below shows an example of a work bench properly equipped to control electro-static discharge. Note that the wrist strap is connected to a 1 megohm resistor. This resistor can be omitted in the setup if the wrist strap has a 1 megohm assembled on the cable attached.



DSP 11

PACKAGING INFORMATION

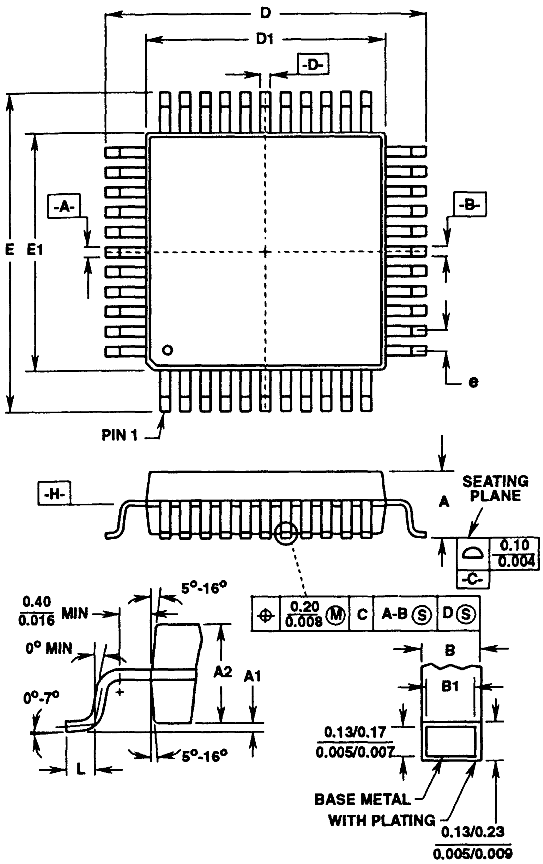
DSP Package Selection Guide

Using the Selection Guide:

The first character of each entry indicates the package type, while the number preceding the decimal point details the package lead count. Except for CPGA and TAB packages, the decimal point and succeeding numbers relate to the package body dimensions (e.g. .14 x 20 = 14mm x 20mm; .95 = 950 mil sq.; .3 = 300 mils. The entire entry indicates the table containing the appropriate package dimensions (e.g. 24 lead PDIP dimension are detailed in Table E24.3). The index on page 11-1 lists page numbers for MQFP, PLCC, SOIC, PDIP, CPGA and TAB tables.

PART NUMBER	MQFP	PLCC	SOIC	PDIP	CPGA	TAB
HMA510		N68.95			G68.A	
HMA510/883					G68.A	
HMU16		N68.95			G68.A	
HMU16/883					G68.A	
HMU17		N68.95			G68.A	
HMU17/883					G68.A	
HSP43124			M28.3	E28.6		
HSP43168	Q100.14x20	N84.1.15			G84.A	
HSP43168/883					G84.A	
HSP43216		N84.1.15			G85.A	
HSP43220	Q100.14x20	N84.1.15			G84.A	S84.A
HSP43220/883					G84.A	
HSP43481		N68.95			G68.A	
HSP43481/883					G68.A	
HSP43881		N84.1.15			G85.A	
HSP43881/883					G85.A	
HSP43891	Q100.14x20	N84.1.15			G85.A	
HSP43891/883					G85.A	
HSP45102			M28.3	E28.6		
HSP45106		N84.1.15			G85.A	
HSP45106/883		N84.1.15			G85.A	
HSP45116	Q160.28x28				G145.A	S156.A
HSP45116A	Q160.28x28					
HSP45116/883					G145.A	
HSP45240		N68.95			G68.A	
HSP45240/883					G68.A	
HSP45256		N84.1.15			G85.A	
HSP45256/883					G85.A	
HSP48212	Q64.14x14	N68.95				
HSP48410		N84.1.15			G84.A	
HSP48410/883		N84.1.15			G84.A	
HSP48901		N68.95			G68.A	
HSP48908	Q100.14x20	N84.1.15			G84.A	
HSP48908/883					G84.A	
HSP50016		N44.65			G48.A	
HSP9501		N44.65				
HSP9520			M24.3	E24.3		
HSP9521			M24.3	E24.3		

Metric Plastic Quad Flatpack (MQFP) Packages



Q64.14x14 (JEDEC MO-108BD-2 ISSUE A)
64 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

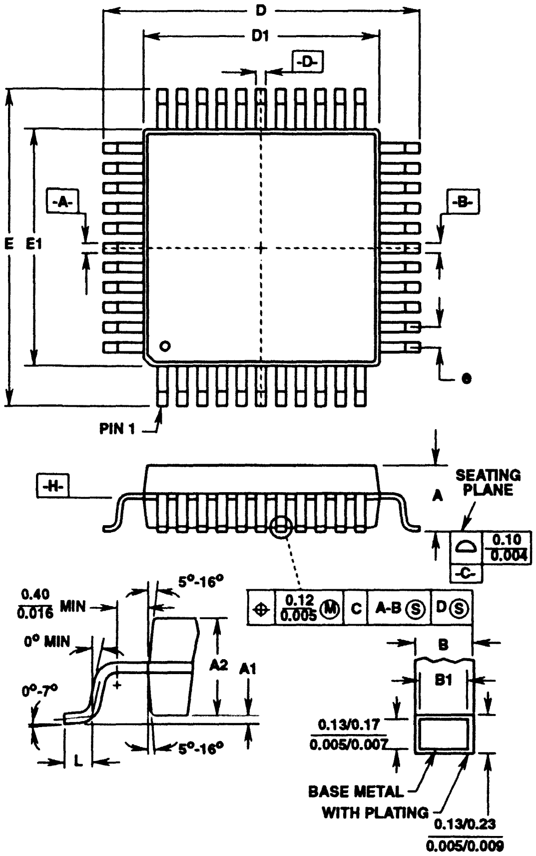
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.130	-	3.30	-
A1	0.004	0.010	0.10	0.25	-
A2	0.100	0.120	2.55	3.05	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.667	0.687	16.95	17.45	3
D1	0.547	0.555	13.90	14.10	4, 5
E	0.667	0.687	16.95	17.45	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	64		64		7
e	0.032 BSC		0.80 BSC		-

Rev. 0 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack (MQFP) Packages (Continued)



Q100.14x20 (JEDEC MO-108CC-1 ISSUE A)
100 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.134	-	3.40	-
A1	0.010	-	0.25	-	-
A2	0.100	0.120	2.55	3.05	-
B	0.009	0.015	0.22	0.38	6
B1	0.009	0.013	0.22	0.33	-
D	0.904	0.923	22.95	23.45	3
D1	0.783	0.791	19.90	20.10	4, 5
E	0.667	0.687	16.95	17.45	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	100		100		7
e	0.026 BSC		0.65 BSC		-
ND	30		30		-
NE	20		20		-

Rev. 0 1/94

Q160.28x28 (JEDEC MO-108DD-1 ISSUE A)
160 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

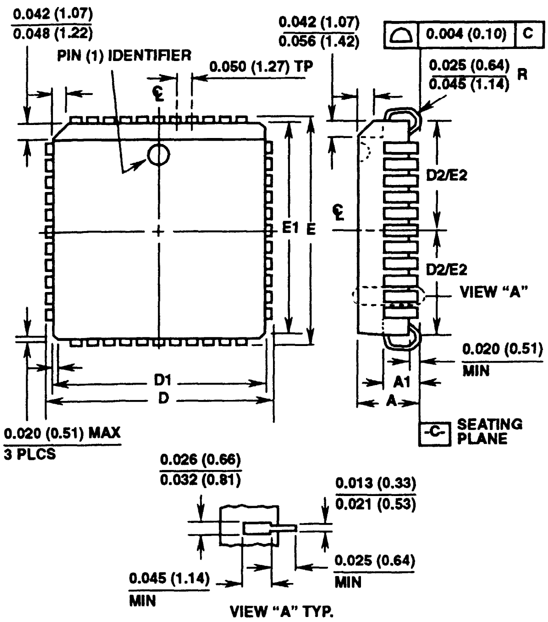
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.160	-	4.07	-
A1	0.010	-	0.25	-	-
A2	0.125	0.144	3.17	3.67	-
B	0.009	0.015	0.22	0.38	6
B1	0.009	0.013	0.22	0.33	-
D	1.219	1.238	30.95	31.45	3
D1	1.098	1.106	27.90	28.10	4, 5
E	1.219	1.238	30.95	31.45	3
E1	1.098	1.106	27.90	28.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	160		160		7
e	0.026 BSC		0.65 BSC		-

Rev. 0 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

Plastic Leaded Chip Carrier (PLCC) Packages



NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

N44.65 (JEDEC MS-018 ISSUE A)
44 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.685	0.695	17.40	17.65	-
D1	0.650	0.656	16.51	16.66	3
D2	0.291	0.319	7.40	8.10	4, 5
E	0.685	0.695	17.40	17.65	-
E1	0.650	0.656	16.51	16.66	3
E2	0.291	0.319	7.40	8.10	4, 5
N	44		44		6

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N68.95 (JEDEC MS-018 ISSUE A)
68 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.985	0.995	25.02	25.27	-
D1	0.950	0.958	24.13	24.33	3
D2	0.441	0.469	11.21	11.91	4, 5
E	0.985	0.995	25.02	25.27	-
E1	0.950	0.958	24.13	24.33	3
E2	0.441	0.469	11.21	11.91	4, 5
N	68		68		6

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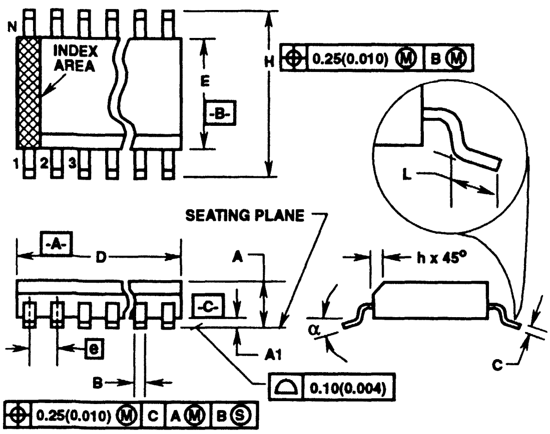
N84.1.15 (JEDEC MS-018 ISSUE A)
84 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	1.185	1.195	30.10	30.35	-
D1	1.150	1.158	29.21	29.41	3
D2	0.541	0.569	13.75	14.45	4, 5
E	1.185	1.195	30.10	30.35	-
E1	1.150	1.158	29.21	29.41	3
E2	0.541	0.569	13.75	14.45	4, 5
N	84		84		6

Rev. 0 12/93

Small Outline Plastic (SOIC) Packages



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

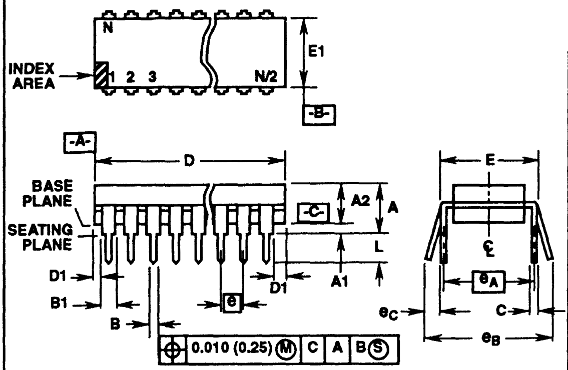
Rev. 0 12/93

M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

Dual-In-Line Plastic (PDIP) Packages



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E24.3 **(JEDEC MS-001-AF ISSUE D)**
24 LEAD NARROW BODY DUAL-IN-LINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	1.230	1.280	31.24	32.51	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	24		24		9

Rev. 0 12/93

E28.6 **(JEDEC MS-011-AB ISSUE B)**
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

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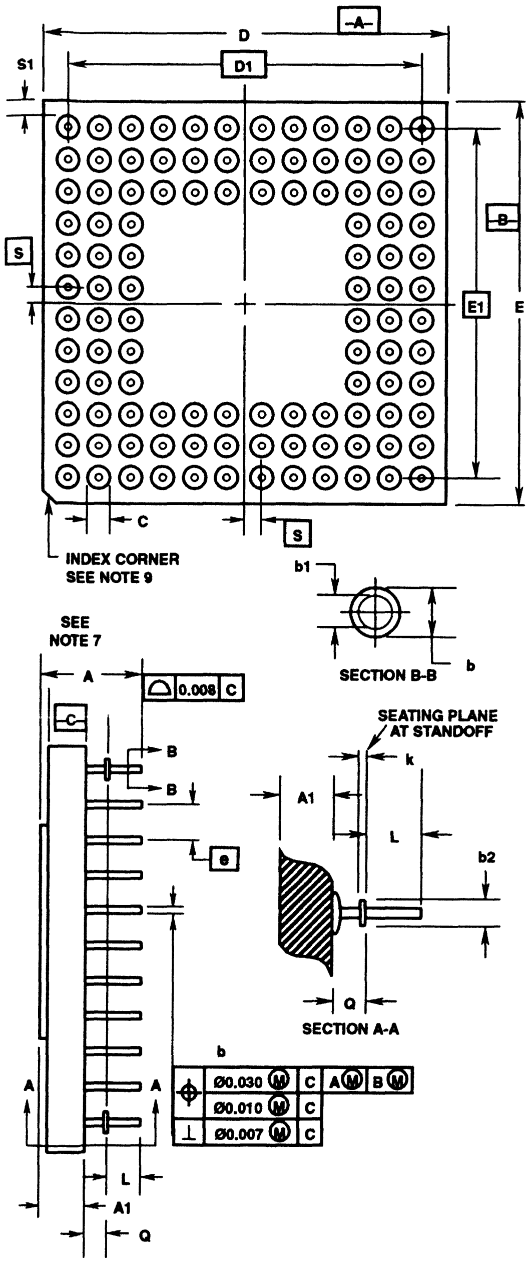
Ceramic Pin Grid Array (CPGA) Packages



G48.A

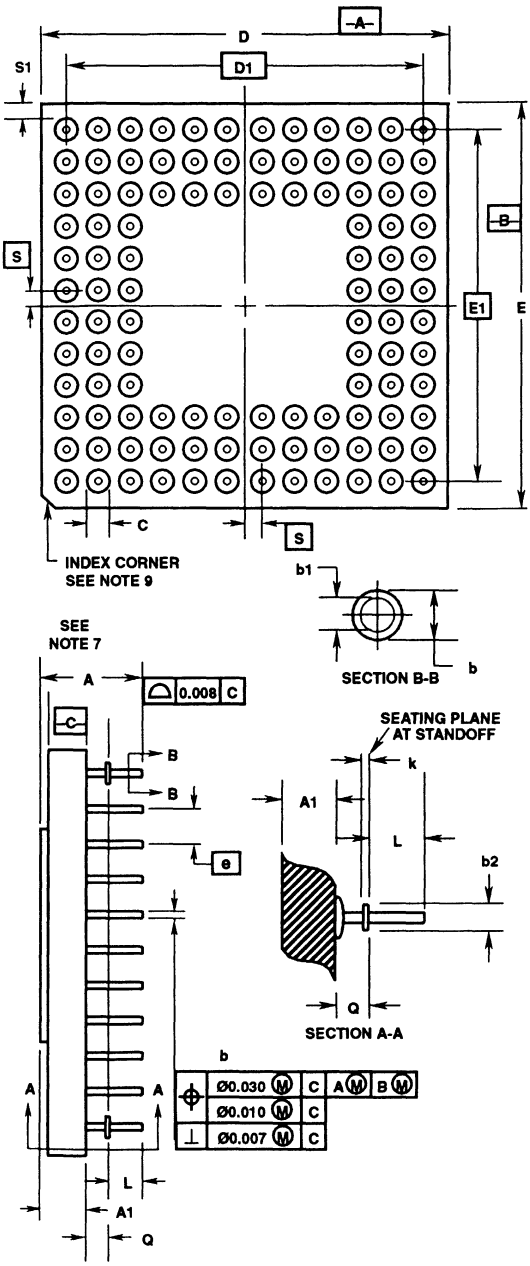
48 LEAD CERAMIC PIN GRID ARRAY PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	-	-	-	-
A1	0.080	0.120	2.03	3.05	3
b	0.016	0.0215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.040	0.060	1.02	1.52	4
C	-	0.80	-	2.03	-
D	0.790	0.810	20.07	20.57	-
D1	0.700 BSC		17.78 BSC		-
E	0.790	0.810	20.07	20.57	-
E1	0.700 BSC		17.78 BSC		-
e	0.100 BSC		2.54 BSC		6
k	-	-	-	-	-
L	0.090	0.110	2.29	2.79	-
Q	0.40	0.060	1.02	1.52	5
S	0.050 BSC		1.27 BSC		10
S1	-	-	-	-	
M	8		8		1
N	-	64	-	64	2

NOTES:

1. "M" represents the maximum pin matrix size.
2. "N" represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension "A1" includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity up. Dimension does not include heatsinks or other attached features.
4. Standoffs are intrinsic and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimensions Q.
5. Dimension "Q" applies to cavity-up configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension "S" is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling Dimensions: Inch.
13. Lead Finish: Type C.
14. Materials: Compliant to MIL-I-38535.

Ceramic Pin Grid Array (CPGA) Packages (Continued)



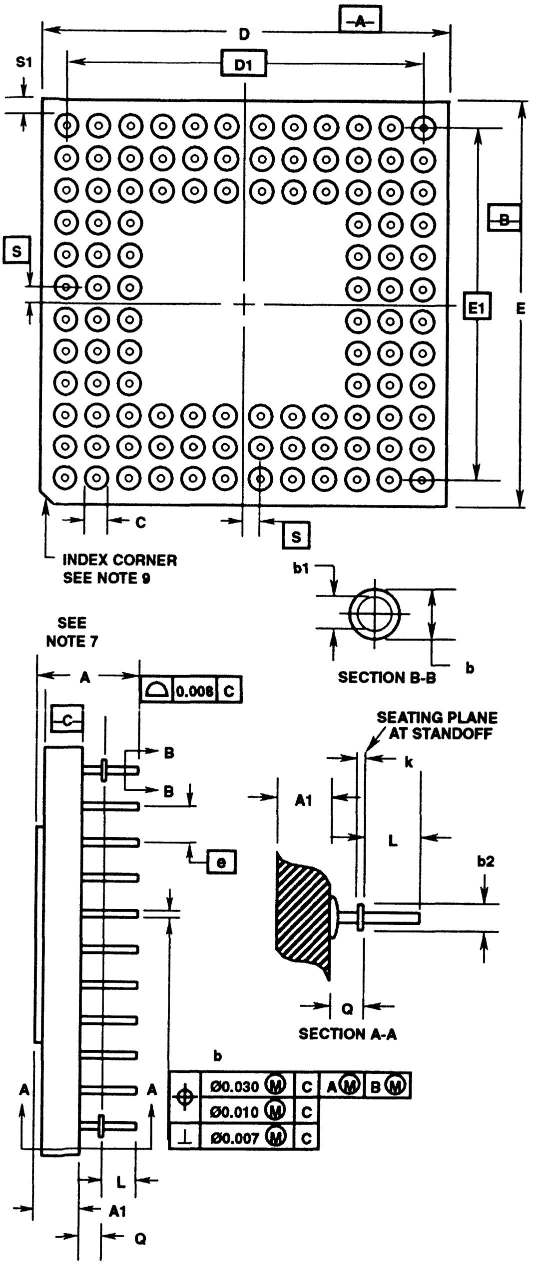
G68.A MIL-STD-1835 CMGA3-PN (P-AC)
68 LEAD CERAMIC PIN GRID ARRAY PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.215	0.345	5.46	8.76	-
A1	0.070	0.145	1.78	3.68	3
b	0.016	0.0215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.042	0.058	1.07	1.47	4
C	-	0.080	-	2.03	-
D	1.140	1.180	28.96	29.97	-
D1	1.000 BSC		25.4 BSC		-
E	1.140	1.180	28.96	29.97	-
E1	1.000 BSC		25.4 BSC		-
e	0.100 BSC		2.54 BSC		6
k	0.008 REF		0.20 REF		-
L	0.120	0.140	3.05	3.56	-
Q	0.040	0.060	1.02	1.52	5
S	0.000 BSC		0.00 BSC		10
S1	0.003	-	0.08	-	-
M	11		11		1
N	-	121	-	121	2

NOTES:

1. "M" represents the maximum pin matrix size.
2. "N" represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension "A1" includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity up. Dimension does not include heatsinks or other attached features.
4. Standoffs are intrinsic and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimensions Q.
5. Dimension "Q" applies to cavity-up configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension "S" is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling Dimensions: Inch.
13. Lead Finish: Type C.
14. Materials: Compliant to MIL-I-38535.

Ceramic Pin Grid Array (CPGA) Packages (Continued)



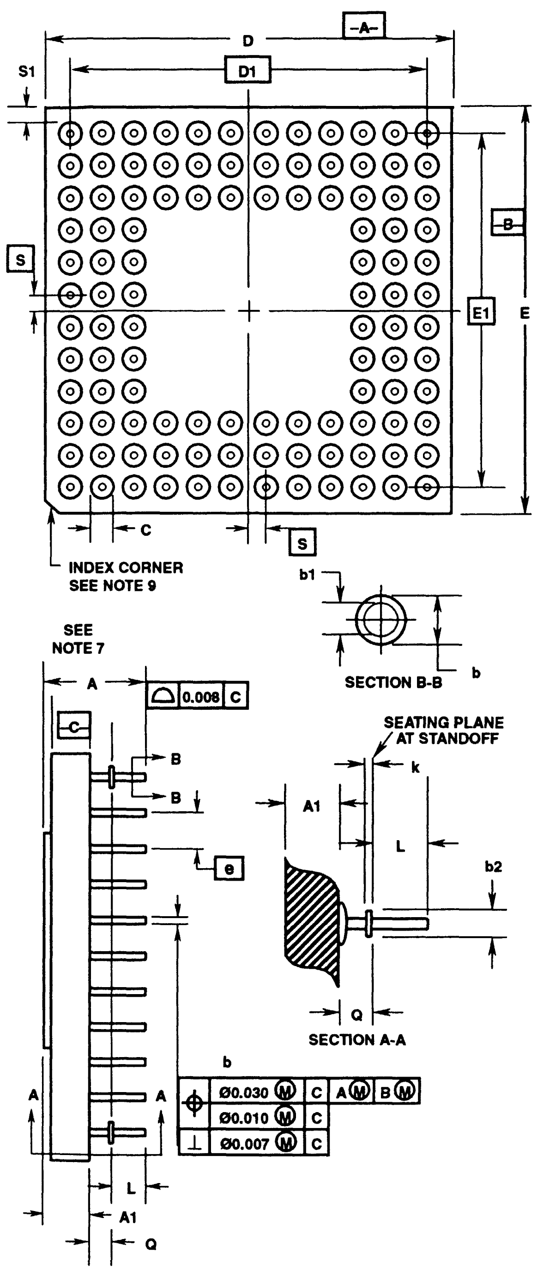
G84.A MIL-STD-1835 CMGA3-PN (P-AC)
84 LEAD CERAMIC PIN GRID ARRAY PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.215	0.345	5.46	8.76	-
A1	0.070	0.145	1.78	3.68	3
b	0.016	0.0215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.042	0.058	1.07	1.47	4
C	-	0.080	-	2.03	-
D	1.140	1.180	28.96	29.97	-
D1	1.000 BSC		25.4 BSC		-
E	1.140	1.180	28.96	29.97	-
E1	1.000 BSC		25.4 BSC		-
e	0.100 BSC		2.54 BSC		6
k	0.008 REF		0.20 REF		-
L	0.120	0.140	3.05	3.56	-
Q	0.040	0.060	1.02	1.52	5
S	0.000 BSC		0.00 BSC		10
S1	0.003	-	0.08	-	-
M	11		11		1
N	-	121	-	121	2

NOTES:

1. "M" represents the maximum pin matrix size.
2. "N" represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension "A1" includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity up. Dimension does not include heatsinks or other attached features.
4. Standoffs are intrinsic and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimensions Q.
5. Dimension "Q" applies to cavity-up configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension "S" is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling Dimensions: Inch.
13. Lead Finish: Type C.
14. Materials: Compliant to MIL-I-38535.

Ceramic Pin Grid Array (CPGA) Packages (Continued)



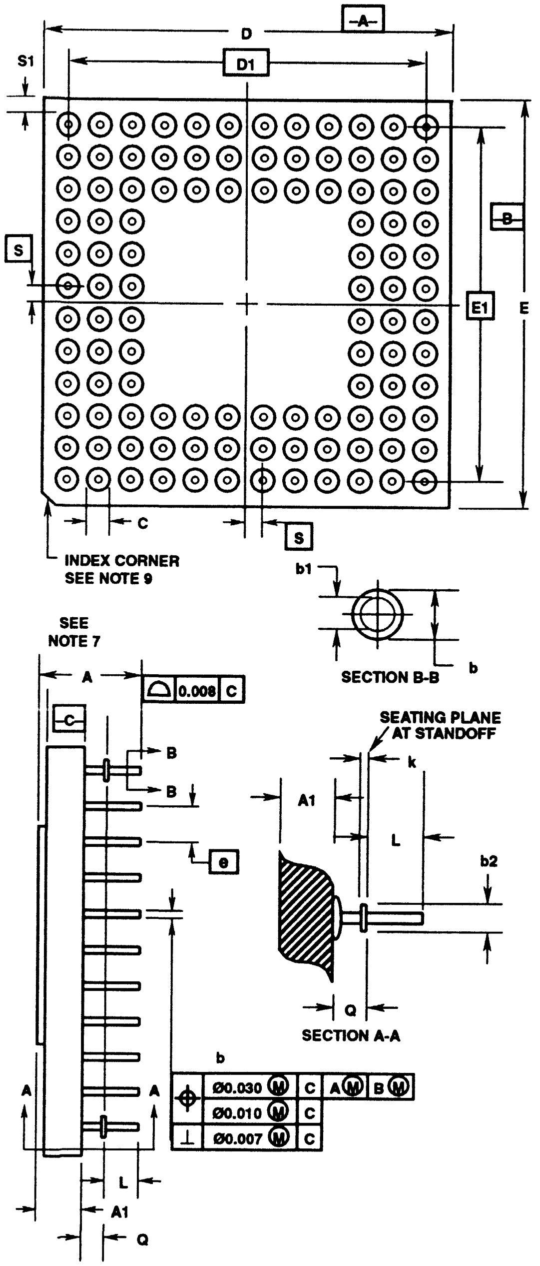
G85.A MIL-STD-1835 CMGA3-PN (P-AC)
85 LEAD CERAMIC PIN GRID ARRAY PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.215	0.345	5.46	8.76	-
A1	0.070	0.145	1.78	3.68	3
b	0.016	0.215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.042	0.058	1.07	1.47	4
C	-	0.080	-	2.03	-
D	1.140	1.180	28.96	29.97	-
D1	1.000 BSC		25.4 BSC		-
E	1.140	1.180	28.96	29.97	-
E1	1.000 BSC		25.4 BSC		-
e	0.100 BSC		2.54 BSC		6
k	0.008 REF		0.20 REF		-
L	0.120	0.140	3.05	3.56	-
Q	0.040	0.060	1.02	1.52	5
S	0.000 BSC		0.00 BSC		10
S1	0.003	-	0.08	-	-
M	11		11		1
N	-	121	-	121	2

NOTES:

1. "M" represents the maximum pin matrix size.
2. "N" represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension "A1" includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity up. Dimension does not include heatsinks or other attached features.
4. Standoffs are intrinsic and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimensions Q.
5. Dimension "Q" applies to cavity-up configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension "S" is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling Dimensions: Inch.
13. Lead Finish: Type C.
14. Materials: Compliant to MIL-I-38535.

Ceramic Pin Grid Array (CPGA) Packages (Continued)



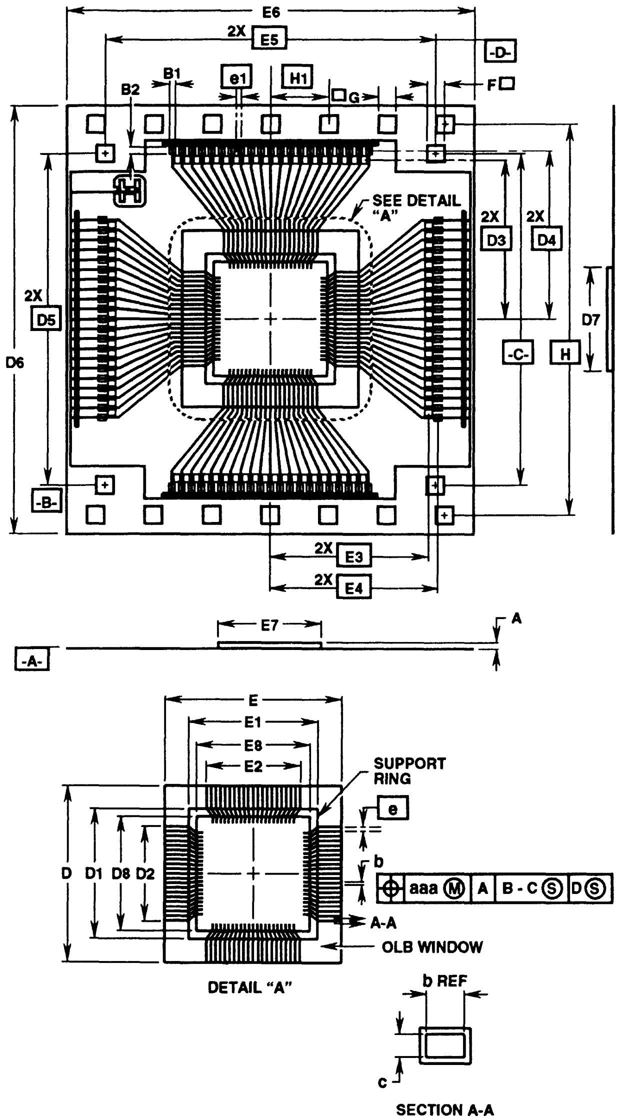
G145.A MIL-STD-1835 CMGA7-PN (P-AG)
145 LEAD CERAMIC PIN GRID ARRAY PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.215	0.345	5.46	8.76	-
A1	0.070	0.145	1.78	3.68	3
b	0.016	0.0215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.042	0.058	1.07	1.47	4
C	-	0.080	-	2.03	-
D	1.540	1.590	39.12	40.38	-
D1	1.400 BSC		35.56 BSC		-
E	1.540	1.590	39.12	40.38	-
E1	1.400 BSC		35.56 BSC		-
e	0.100 BSC		2.54 BSC		6
k	0.008 REF		0.20 REF		-
L	0.120	0.140	3.05	3.56	-
Q	0.040	0.060	1.02	1.52	5
S	0.000 BSC		0.00 BSC		10
S1	0.003	-	0.08	-	-
M	15		15		1
N	-	225	-	225	2

NOTES:

1. "M" represents the maximum pin matrix size.
2. "N" represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension "A1" includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity up. Dimension does not include heatsinks or other attached features.
4. Standoffs are intrinsic and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimensions Q.
5. Dimension "Q" applies to cavity-up configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension "S" is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling Dimensions: Inch.
13. Lead Finish: Type C.
14. Materials: Compliant to MIL-I-38535.

Tape Automated Bonding (TAB) Packages



S84.A

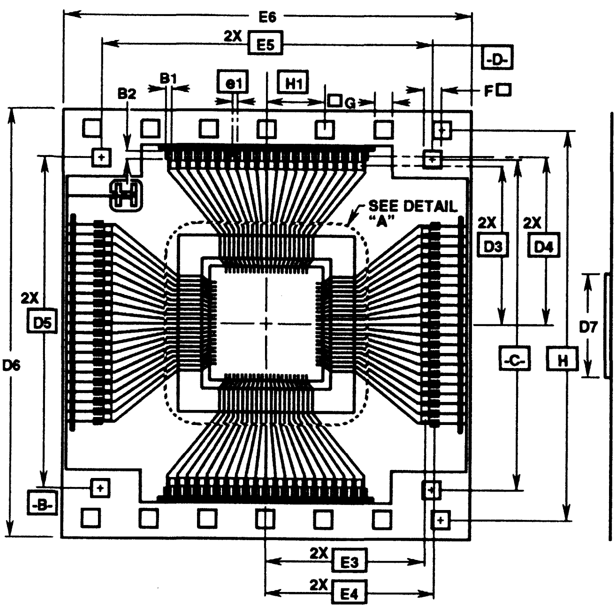
84 LEAD TAPE AUTOMATED BONDING PACKAGE

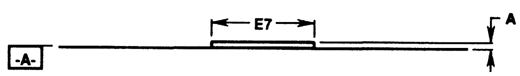
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.034	-	0.86	-
b	0.002	0.004	0.05	0.10	2, 7
c	0.0010	0.0018	0.025	0.046	2, 7
B1	0.019	0.021	0.47	0.53	5
B2	0.023	0.028	0.60	0.70	5
D	0.559	0.569	14.20	14.45	-
E	0.562	0.572	14.27	14.53	-
D1	0.410	0.420	10.41	10.67	3
E1	0.409	0.419	10.39	10.64	3
D2	0.300	0.310	7.62	7.87	4
E2	0.300	0.310	7.62	7.87	4
D3/E3	0.500 BSC		12.70 BSC		-
D4/E4	0.531 BSC		13.475 BSC		-
D5/E5	1.061 BSC		26.95 BSC		-
D6	1.372	1.382	34.85	35.10	-
E6	1.244	1.314	31.62	33.37	-
D7	0.345	0.351	8.77	8.92	-
E7	0.344	0.350	8.74	8.89	-
D8	0.360	0.370	9.14	9.40	-
E8	0.358	0.368	9.09	9.35	-
e	0.015 BSC		0.38 BSC		2
e1	0.016 BSC		0.40 BSC		5
F	0.054	0.057	1.39	1.45	-
G	0.055	0.057	1.40	1.45	-
H	1.253 BSC		31.83 BSC		-
H1	0.187 BSC		4.75 BSC		-
aaa	0.003		0.08		-

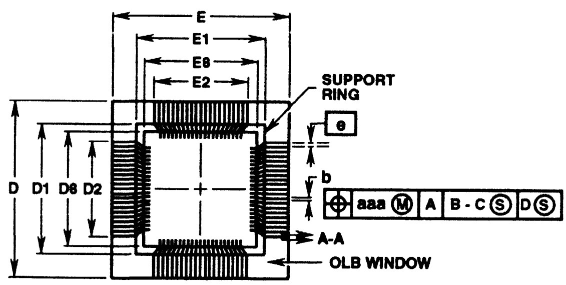
NOTES:

1. All dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Controlling dimension is MILLIMETERS except for dimensions b, c and e which are in INCHES.
3. Dimensions D1/E1 define the package "body size".
4. Dimensions D2/E2 define the maximum allowable dimension between the outside edges of the outermost leads. This dimension provides necessary clearance from the OLB window corners for excise operations.
5. This dimension applies to all test pads.
6. All lead and test pad arrays shall be arranged in a symmetric configuration with respect to datums D or B-C.
7. Dimensions b and c apply to base material only.
8. Lead Material: Copper
   Lead Finish: Gold over nickel underplate
9. Film format and test pads per JEDEC US-001, Ax - 2x.
10. TAB packages shipped in slide carriers per JEDEC CS-006 with the leads unformed (flat).

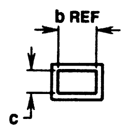
Tape Automated Bonding (TAB) Packages (Continued)







DETAIL "A"



SECTION A-A

S156.A

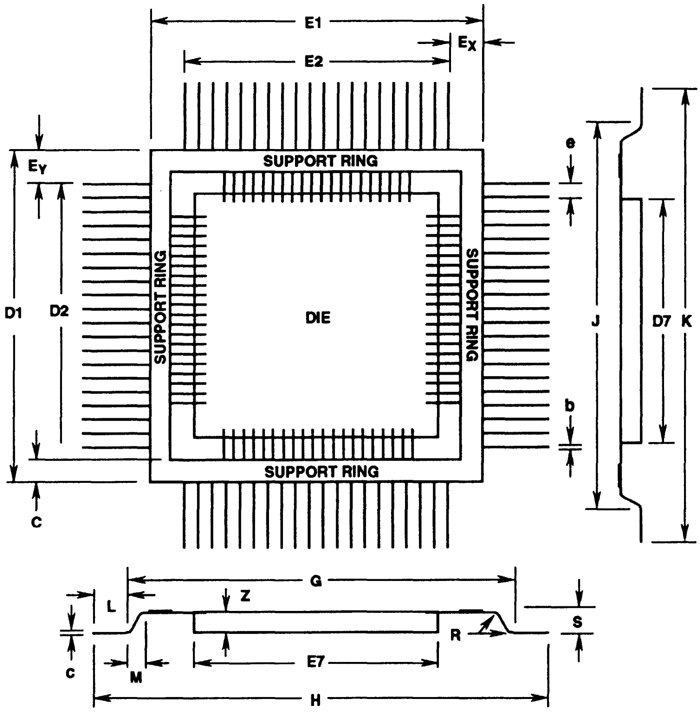
156 LEAD TAPE AUTOMATED BONDING PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.034	-	0.86	-
b	0.002	0.004	0.05	0.10	2
c	0.0010	0.0018	0.025	0.046	2, 7
B1	0.019	0.021	0.47	0.53	5
B2	0.023	0.028	0.60	0.70	5
D	0.559	0.569	14.20	14.45	-
E	0.562	0.572	14.27	14.53	-
D1	0.429	0.439	10.90	11.15	3
E1	0.431	0.441	10.95	11.20	3
D2	0.380	0.390	9.65	9.90	4
E2	0.380	0.390	9.65	9.90	4
D3/E3	0.500 BSC		12.70 BSC		-
D4/E4	0.531 BSC		13.475 BSC		-
D5/E5	1.061 BSC		26.95 BSC		-
D6	1.372	1.382	34.85	35.10	-
E6	1.244	1.314	31.62	33.37	-
D7	0.349	0.355	8.87	9.02	-
E7	0.346	0.352	8.79	8.94	-
D8	0.360	0.370	9.14	9.40	-
E8	0.367	0.377	9.32	9.57	-
e	0.010 BSC		0.254 BSC		2
e1	0.016 BSC		0.40 BSC		5
F	0.054	0.057	1.39	1.45	-
G	0.055	0.057	1.40	1.45	-
H	1.253 BSC		31.83 BSC		-
H1	0.187 BSC		4.75 BSC		-
aaa	0.002		0.05		-

NOTES:

1. All dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Controlling dimension is MILLIMETERS except for dimensions b, c and e which are in INCHES.
3. Dimensions D1/E1 define the package "body size".
4. Dimensions D2/E2 define the maximum allowable dimension between the outside edges of the outermost leads. This dimension provides necessary clearance from the OLB window corners for excise operations.
5. This dimension applies to all test pads.
6. All lead and test pad arrays shall be arranged in a symmetric configuration with respect to datums D or B-C.
7. Dimensions b and c apply to base material only.
8. Lead Material: Copper
   Lead Finish: Gold over nickel underplate
9. Film format and test pads per JEDEC US-001, Ax - 2x.
10. TAB packages shipped in slide carriers per JEDEC CS-006 with the leads unformed (flat).

Tape Automated Bonding (TAB) Suggested Lead Form Dimensions



CONSTANT DIMENSIONS									
b	G	H	J	K	L	M	c	R	S
0.003	0.475	0.515	0.472	0.512	0.020	0.0114	0.0014	0.0057	0.0224

DEVICE DEPENDENT DIMENSIONS												
DEVICE	LEADS	E1	D1	E2	D2	C	e	E_X	E_Y	E7	D7	Z
HSP43220	84	0.414	0.415	0.305	0.305	0.025	0.015	0.0545	0.0550	0.348	0.349	0.019
HSP45116	156	0.436	0.434	0.385	0.385	0.032	0.010	0.0256	0.0245	0.350	0.353	0.019

DSP 12

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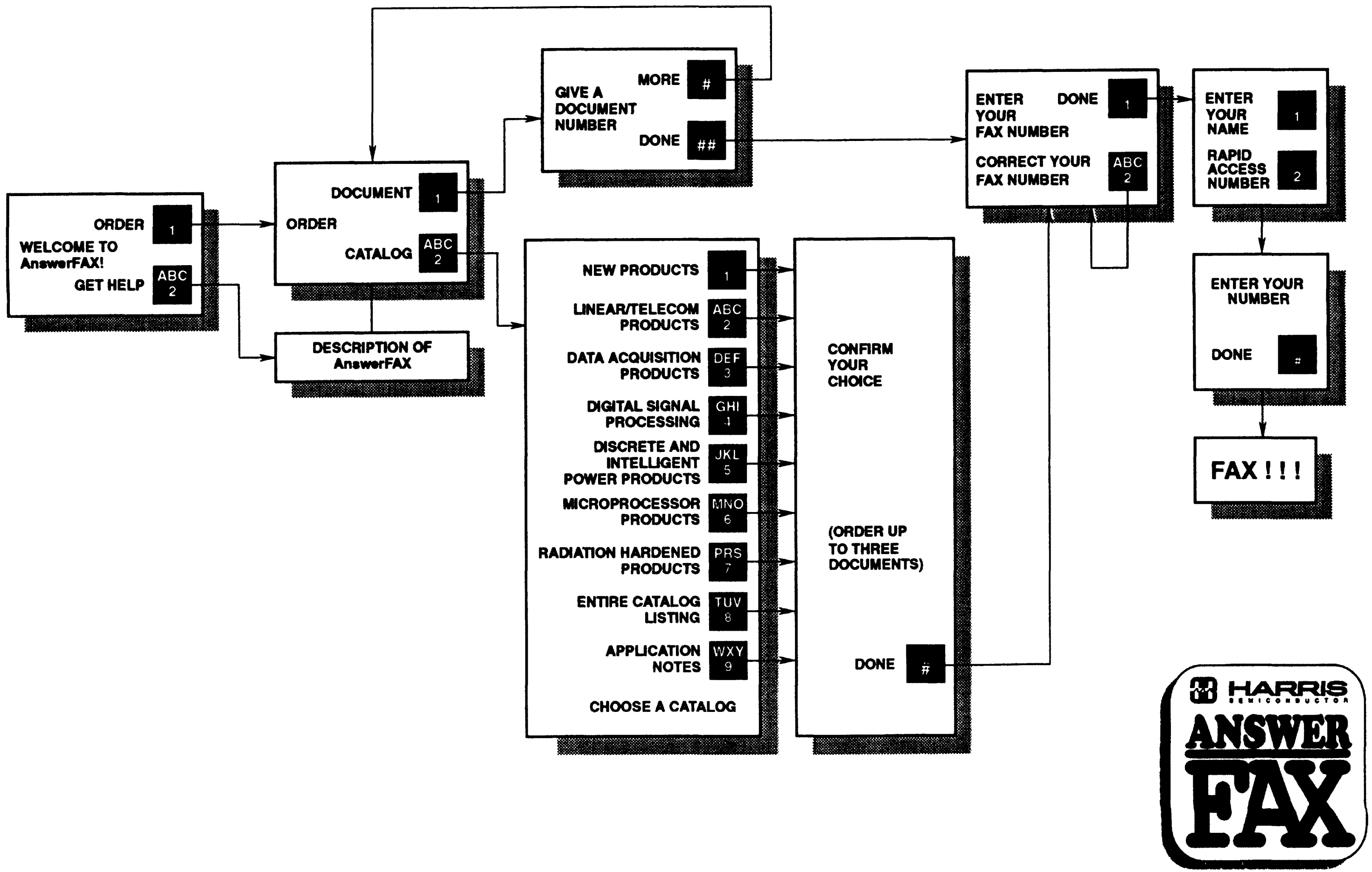

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DB500B	**LINEAR AND TELECOM ICs** (1993: 1,312pp) Product specifications for: op amps, comparators, S/H amps, differential amps, arrays, special analog circuits, telecom ICs, and power processing circuits.
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DB302A	**DIGITAL SIGNAL PROCESSING** (1993: 380pp) This new edition includes specifications on one- and two-dimensional filters, signal synthesizers, multipliers, special function devices (such as address sequencers, binary correlators, histogrammer). Includes sections on development tools, application notes and Quality/Reliability.
DB304	**INTELLIGENT POWER ICs** (1992: 512pp) Product specifications for low- and high-side switches, half bridges, AC-DC converters, full bridges, regulators & power supplies, protection circuits, and special function ICs. Includes application notes and Quality/Reliability sections.
DB450C	**TRANSIENT VOLTAGE SUPPRESSION DEVICES** (1994: 400pp) Product specifications of Harris varistors and surgectors. Also, general informational chapters such as: "Voltage Transients - An Overview," "Transient Suppression - Devices and Principles," "Suppression - Automotive Transients."
DB223.2	**POWER MOSFETs** (1992: 1,504pp) Product specifications on MOSFETs (N- and P-channel, logic level, military and radiation-hardened); IGBTs; Intelligent discretes; power drivers and switches; and ultra-fast rectifiers. Includes industry replacement guide and application notes.
DB220.1	**BIPOLAR POWER TRANSISTORS** (1992: 592pp) Technical information on over 750 power transistors for use in a wide range of consumer, industrial and military applications. Indexing and packaging included.
DB303	**MICROPROCESSOR PRODUCTS** (1992: 1,156pp) For commercial and military applications. Product specifications on CMOS microprocessors, peripherals, data communications, and memory ICs. Includes application notes and Quality/Reliability chapters.
DB309	**MCT/IGBT/DIODES** (1994: 528pp) This databook fully describes Harris Semiconductor's line of MOS Controlled Thyristors, Insulated Gate Bipolar Transistors (IGBTs) and Power Diodes/Rectifiers. It includes a complete set of datasheets for product specifications, application notes with design details for specific applications of Harris products, and a description of the Harris Quality and Reliability program.
Analog Military	**ANALOG MILITARY** (1989: 1,264pp) This databook describes Harris' military line of Linear, Data Acquisition, and Telecommunications circuits.
Digital Military	**DIGITAL MILITARY** (1989: 680pp) Harris CMOS digital ICs -- microprocessors, peripherals, data communications and memory -- are included in this databook.

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AnswerFAX Technical Support Application Note Listing

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9002	AN002	Principles of Data Acquisition and Conversion (20 pages)
9004	AN004	The IH5009 Analog Switch Series (9 pages)
9007	AN007	Using the 8048/8049 Log/Antilog Amplifier (6 pages)
9009	AN009	Pick Sample-Holds by Accuracy and Speed and Keep Hold Capacitors in Mind (7 pages)
9012	AN012	Switching Signals with Semiconductors (4 pages)
9013	AN013	Everything You Always Wanted to Know About the ICL8038 (4 pages)
9016	AN016	Selecting A/D Converters (7 pages)
9017	AN017	The Integrating A/D Converter (5 pages)
9018	AN018	Do's and Don'ts of Applying A/D Converters (4 pages)
9020	AN020	A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing (23 pages)
9023	AN023	Low Cost Digital Panel Meter Designs (5 pages)
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9053	AN053	The ICL7650 A New Era in Glitch-Free Chopper Stabilized Amplifiers (19 pages)
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